

# Alex Tomala

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## Employment History

### Massachusetts Institute of Technology

May 2016 - Current

*Visiting Student*

- Investigating new methods to classify scientific papers using Machine learning methods
- Maintaining the group servers and previously developed code on them

### University of Toronto Institute for Aerospace Studies

April 2015 - August 2015

*Research Intern*

- Developed error correction systems (using C++ and ROS) for an autonomous wheelchair
- Developed a web app (using React.js) to manage the wheelchair using a touchscreen tablet

### Science Expo

October 2014 - February 2015

*IT Manager*

- Managed the Science Expo webserver while also designing websites for various Science Expo events
- Overhauled the Science Expo website to have a modern look and defined sub-domains for province specific websites

## Skills

#### Programming Languages

- Python, C, C++, C#, Objective-C, Java, Racket
- MIPS/x86 assembly
- VHDL

#### Web Design

- D3.js
- React.js/Ember.js
- Bootstrap/Materialize
- JQuery, HammerJS

#### Other

- Machine Learning
- ROS
- Computer Networking
- $\text{\LaTeX}$

## Education

### University of Waterloo

September 2015 - Current

*Candidate for Bachelor of Computer Science*

- Expected to Graduate in 2020
- 91% cumulative average while taking all the advanced Math/CS courses

## Notable Awards

### CWSF Senior Informatics Award

May 2014

- Awarded to the best Grade 11-12 computing related project at the Canada Wide Science Fair (largest national science fair).

### Intel Excellence Award - Computer Science

May 2014, May 2013

- Awarded to the best computing related project at the Bay Area Science and Engineering Fair, one of the largest science fairs in Canada.

## Projects

### An Innovative Approach to Multi-Core Interconnection Networks

July 2013 - April 2014

- Modified an innovative tree-based memory subsystem
- Implemented it onto a FPGA and a software simulator (GEM5)

### MIPE: Microprocessor with Integrated Programmable Execution Units

July 2012 - April 2013

- Created a 5-stage RISC microprocessor based on the MIPS32 ISA
- Designed the architecture so the instruction set can be reconfigured to suit different tasks
- Worked on an Assembler to make programming easier