Final Project	
Course Code: CPE 016	**Program: BSCPE**
Course Title: Introduction to HDL	**Date Performed: 9/12/23**
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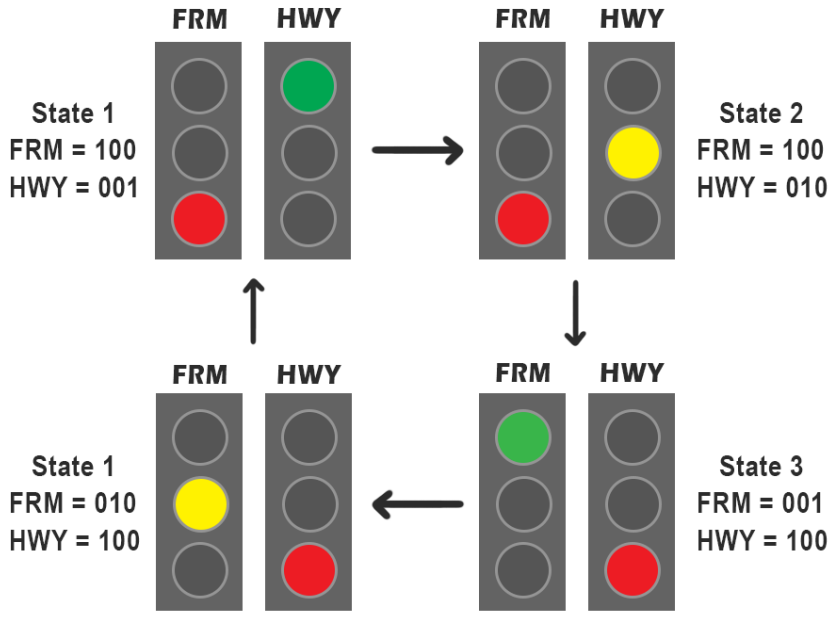
1. Discussion

The traffic light controller in VHDL is used for an intersection between highway and farm way. There is a sensor in the farm way side to detect if there is any vehicle on the farm way. If vehicles are detected on the farm way, traffic lights on the highway turn to YELLOW, then RED so that the vehicles from the farm way can cross the highway. Otherwise, the traffic light on the highway is always GREEN and traffic lights on the farm way are always RED. The time period is 3 seconds for the YELLOW light and 10 seconds for the RED light.

2. Finite state machine design



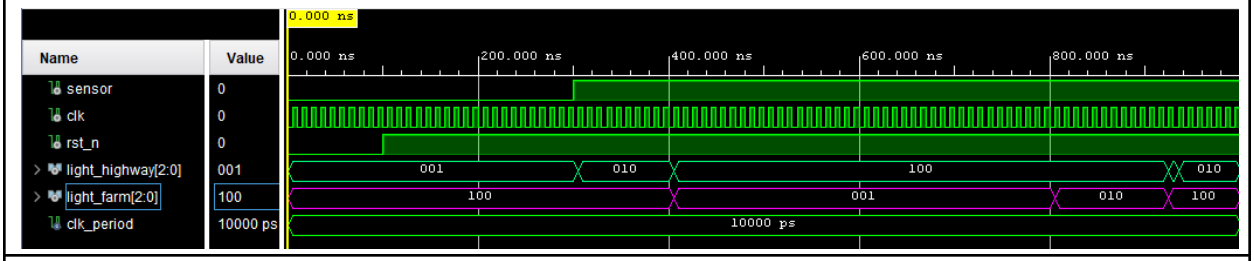
3. VHDL Code

```
3   library IEEE;
4   use IEEE.STD_LOGIC_1164.ALL;
5   use IEEE.STD_LOGIC_UNSIGNED.ALL;
6   -- Traffic ligh system for a intersection between highway and farm way
7   -- There is a sensor on the farm way side, when there are vehicles,
8   -- Traffic light turns to YELLOW, then GREEN to let the vehicles cross the highway
9   -- Otherwise, always green light on Highway and Red light on farm way
10  entity traffic_light_controller is
11   port ( sensor  : in STD_LOGIC; -- Sensor
12          clk  : in STD_LOGIC; -- clock
13          rst_n: in STD_LOGIC; -- reset active low
14          light_highway  : out STD_LOGIC_VECTOR(2 downto 0); -- light outputs of high way
15           light_farm:    out STD_LOGIC_VECTOR(2 downto 0)-- light outputs of farm way
16       --RED_YELLOW_GREEN
17     );
18  end traffic_light_controller;
19  architecture traffic_light of traffic_light_controller is
20  signal counter_1s: std_logic_vector(27 downto 0):= x"0000000";
21  signal delay_count:std_logic_vector(3 downto 0):= x"0";
22  signal delay_10s, delay_3s_F,delay_3s_H, RED_LIGHT_ENABLE, YELLOW_LIGHT1_ENABLE,YELLOW_LIGHT2_ENABLE: std_logic:='0';
23  signal clk_1s_enable: std_logic; -- 1s clock enable
24  type FSM_States is (HGRE_FRED, HYEL_FRED, HRED_FGRE, HRED_FYEL);
25  -- HGRE_FRED : Highway green and farm red
26  -- HYEL_FRED : Highway yellow and farm red
27  -- HRED_FGRE : Highway red and farm green
28  -- HRED_FYEL : Highway red and farm yellow
29  signal current_state, next_state: FSM_States;
30  begin
31  -- next state FSM sequential logic
32  process(clk,rst_n)
33      begin
34      if(rst_n='0') then
35       current_state <= HGRE_FRED;
36      elsif(rising_edge(clk)) then
37       current_state <= next_state;
38      end if;
39      end process;
40      -- FSM combinational logic
41      process(current_state,sensor,delay_3s_F,delay_3s_H,delay_10s)
42      begin
43      case current_state is
44      when HGRE_FRED => -- When Green light on Highway and Red light on Farm way
45       RED_LIGHT_ENABLE <= '0';-- disable RED light delay counting
46       YELLOW_LIGHT1_ENABLE <= '0';-- disable YELLOW light Highway delay counting
47       YELLOW_LIGHT2_ENABLE <= '0';-- disable YELLOW light Farmway delay counting
48       light_highway <= "001"; -- Green light on Highway
49       light_farm <= "100"; -- Red light on Farm way
50       if(sensor = '1') then -- if vehicle is detected on farm way by sensors
51        next_state <= HYEL_FRED;
52        -- High way turns to Yellow light
53       else
54        next_state <= HGRE_FRED;
55        -- Otherwise, remains GREEN ON highway and RED on Farm way
56       end if;
57      when HYEL_FRED => -- When Yellow light on Highway and Red light on Farm way
58       light_highway <= "010";-- Yellow light on Highway
59       light_farm <= "100";-- Red light on Farm way
60       RED_LIGHT_ENABLE <= '0';-- disable RED light delay counting
61       YELLOW_LIGHT1_ENABLE <= '1';-- enable YELLOW light Highway delay counting
62       YELLOW_LIGHT2_ENABLE <= '0';-- disable YELLOW light Farmway delay counting
63       if(delay_3s_H='1') then
64       -- if Yellow light delay counts to 3s,
65       -- turn Highway to RED,
66       -- Farm way to green light
```

```
67          next_state <= HRED_FGRE;
68        else
69          next_state <= HYEL_FRED;
70          -- Remains Yellow on highway and Red on Farm way
71          -- if Yellow light not yet in 3s
72        end if;
73      when HRED_FGRE =>
74        light_highway <= "100";-- RED light on Highway
75        light_farm <= "001";-- GREEN light on Farm way
76        RED_LIGHT_ENABLE <= '1';-- enable RED light delay counting
77        YELLOW_LIGHT1_ENABLE <= '0';-- disable YELLOW light Highway delay counting
78        YELLOW_LIGHT2_ENABLE <= '0';-- disable YELLOW light Farmway delay counting
79        if(delay_10s='1') then
80        -- if RED light on highway is 10s, Farm way turns to Yellow
81          next_state <= HRED_FYEL;
82        else
83          next_state <= HRED_FGRE;
84          -- Remains if delay counts for RED light on highway not enough 10s
85        end if;
86      when HRED_FYEL =>
87        light_highway <= "100";-- RED light on Highway
88        light_farm <= "010";-- Yellow light on Farm way
89        RED_LIGHT_ENABLE <= '0'; -- disable RED light delay counting
90        YELLOW_LIGHT1_ENABLE <= '0';-- disable YELLOW light Highway delay counting
91        YELLOW_LIGHT2_ENABLE <= '1';-- enable YELLOW light Farmway delay counting
92        if(delay_3s_F='1') then
93        -- if delay for Yellow light is 3s,
94        -- turn highway to GREEN light
95        -- Farm way to RED Light
96        next_state <= HGRE_FRED;
97        else
98        next_state <= HRED_FYEL;
99        -- if not enough 3s, remain the same state
100       end if;
101     when others => next_state <= HGRE_FRED; -- Green on highway, red on farm way
```

```
102     end case;
103     end process;
104     -- Delay counts for Yellow and RED light
105     process(clk)
106     begin
107     if(rising_edge(clk)) then
108     if(clk_1s_enable='1') then
109      if(RED_LIGHT_ENABLE='1' or YELLOW_LIGHT1_ENABLE='1' or YELLOW_LIGHT2_ENABLE='1') then
110       delay_count <= delay_count + x"1";
111       if((delay_count = x"9") and RED_LIGHT_ENABLE ='1') then
112        delay_10s <= '1';
113        delay_3s_H <= '0';
114        delay_3s_F <= '0';
115        delay_count <= x"0";
116       elsif((delay_count = x"2") and YELLOW_LIGHT1_ENABLE= '1') then
117        delay_10s <= '0';
118        delay_3s_H <= '1';
119        delay_3s_F <= '0';
120        delay_count <= x"0";
121       elsif((delay_count = x"2") and YELLOW_LIGHT2_ENABLE= '1') then
122        delay_10s <= '0';
123        delay_3s_H <= '0';
124        delay_3s_F <= '1';
125        delay_count <= x"0";
126       else
127        delay_10s <= '0';
128        delay_3s_H <= '0';
129        delay_3s_F <= '0';
130       end if;
131      end if;
132      end if;
133     end if;
134     end process;
135     -- create delay 1s
136     process(clk)
137     begin
138     if(rising_edge(clk)) then
139      counter_1s <= counter_1s + x"0000001";
140      if(counter_1s >= x"0000003") then -- x"0004" is for simulation
141       -- change to x"2FAF080" for 50 MHz clock running real FPGA
142        counter_1s <= x"0000000";
143       end if;
144     end if;
145     end process;
146     clk_1s_enable <= '1' when counter_1s = x"0003" else '0'; -- x"0002" is for simulation
147     -- x"2FAF080" for 50Mhz clock on FPGA
148     end traffic_light;
```

4. Waveform



5. **Video Link:**
   https://drive.google.com/file/d/1HK_-19fCCopY7e53mXOMFA_MGUpmFJqC/view?fbclid=IwAR34dmYAz3fitnI9Ci1eo5kvByQaqQ_B0-I3Yk5HHZrDZBMRzJ5YGxrLNDU

6. **Conclusion**

The traffic light controller in VHDL manages a highway and farm way intersection by detecting vehicles on the farm way. The system operates by keeping the highway green for uninterrupted flow, while the farm way light remains red for 10 seconds. The system prioritizes safety by ensuring a clear path for vehicles entering the highway from the farm way, minimizing waiting times, and ensuring predictability and consistency in traffic flow. VHDL's ability to handle finite state machines makes it ideal for modeling the traffic light controller's behavior. The sensor input triggers a state transition in the VHDL code, initiating the yellow and red light sequence for the highway. Timers manage the duration of each light state, and output signals control the traffic lights connected to the FPGA hardware. The VHDL code can be customized to accommodate different timing requirements or sensor configurations, and integration with additional sensors or traffic management systems is possible for further functionality.