

# MX6SL & MX508-EVK Based E-Book add-on Board 3

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## Revision History

REV	DATE	CHANGES	ENTERED BY
X1	03/09/12	First schematic review.	NI
A	03/30/12	Release to Prototype Phase	NI

# SCH-27468

## IMXEBOOKDC3-E

## Important Notes

- Unless Otherwise Specified:
  - All resistors are in ohms, 5%, 1/8 Watt
  - All voltages are DC
  - All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
  - \_B Denotes - Active-Low Signal
  - <> or [] Denotes - Vectored Signals
- All connector are identified with references "J\*" and the part number is explicit near the drawing for each one.
- Labels in bold green are used to:
  - Additional notes to be considered in the layout.
  - Relevant information of this schematic.
  - Extra identification for components in this schematic.
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.


## Usage Note: For use with LB060S04 Display

To use this board with the LG Display LB060S04 panel, make the folowing changes to a production board:

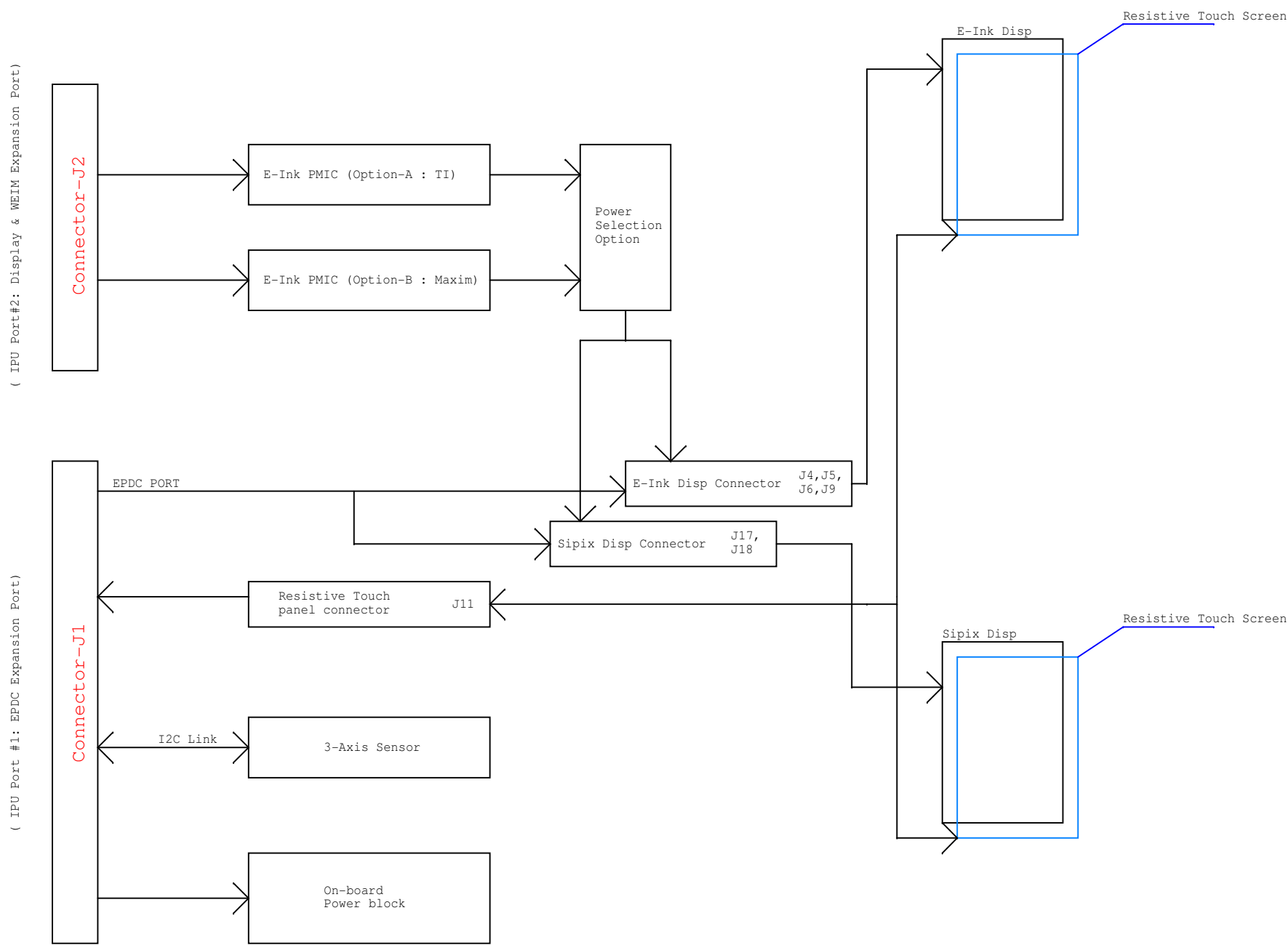
- Cut the following shorting traces: SH7, SH13, SH24, SH25, SH26, SH27, SH28.
- Depopulate the following resistors: R94, R101, R102, R103, R104.
- Populate the following resistors: R16, R58, R174, R175, R176.
- Populate the 1.2V regulator and associated components: U10, C64, C65, R177, R178.

When using the LG Display panel, the KEY\_PAD\_LOCK and the TOUCH\_RESET\_B traces will be disconnected from the EVK.

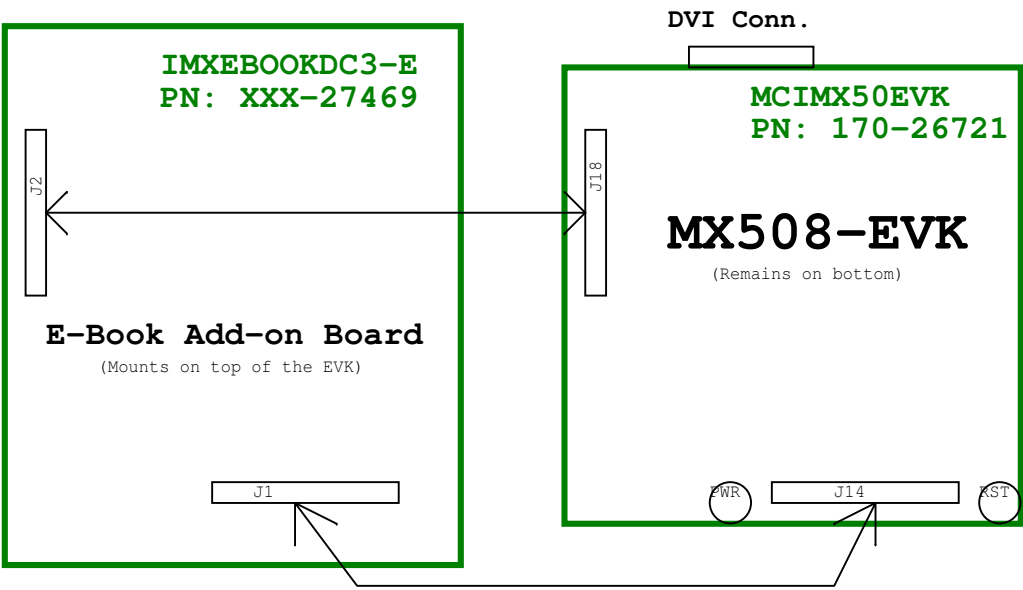
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		ICAP Classification:		FCP:	FIUO:	PUBI:	X
Designer: Nicolas Izquierdo		Drawing Title: <b>IMXEBOOKDC3-E</b>					
Drawn by: Nicolas Izquierdo		Page Title: <b>COVER</b>					
Approved:		Size C	Document Number SCH-27468				Rev A
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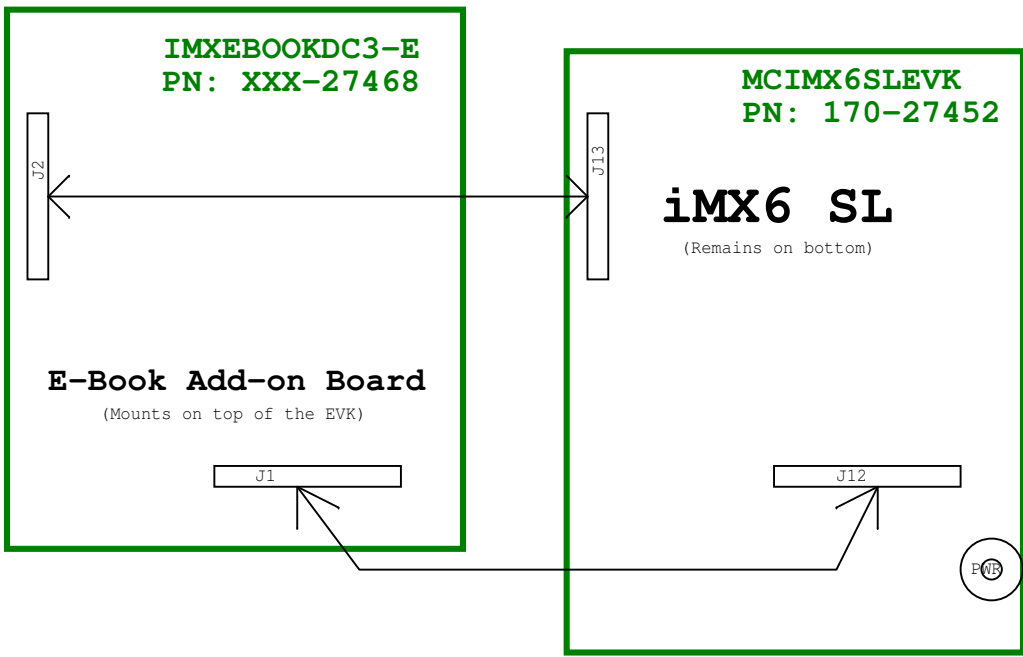
System Block Diagram



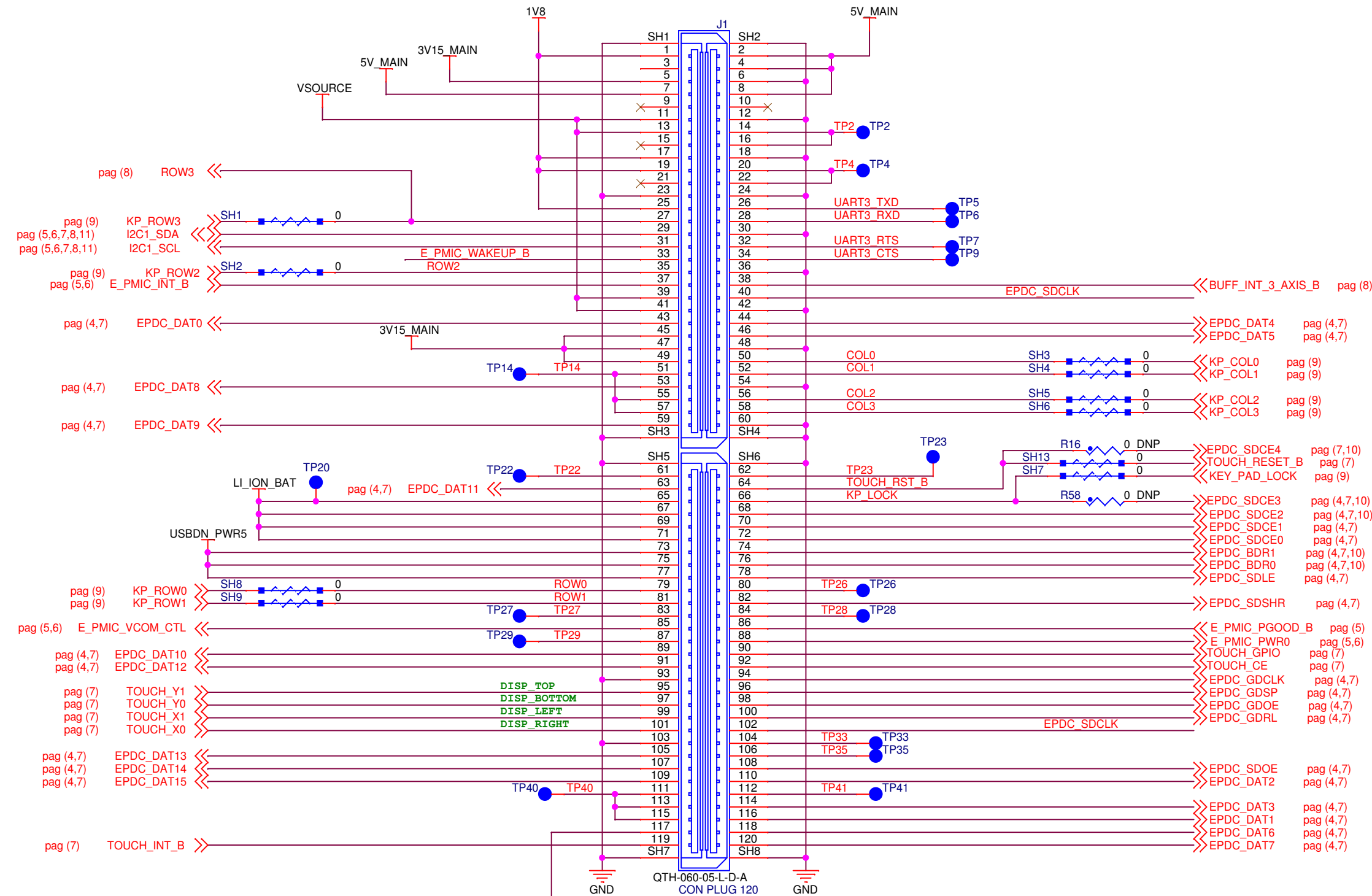
Docking Scheme



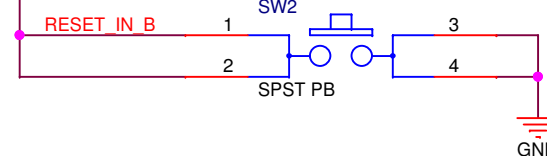
Docking Scheme



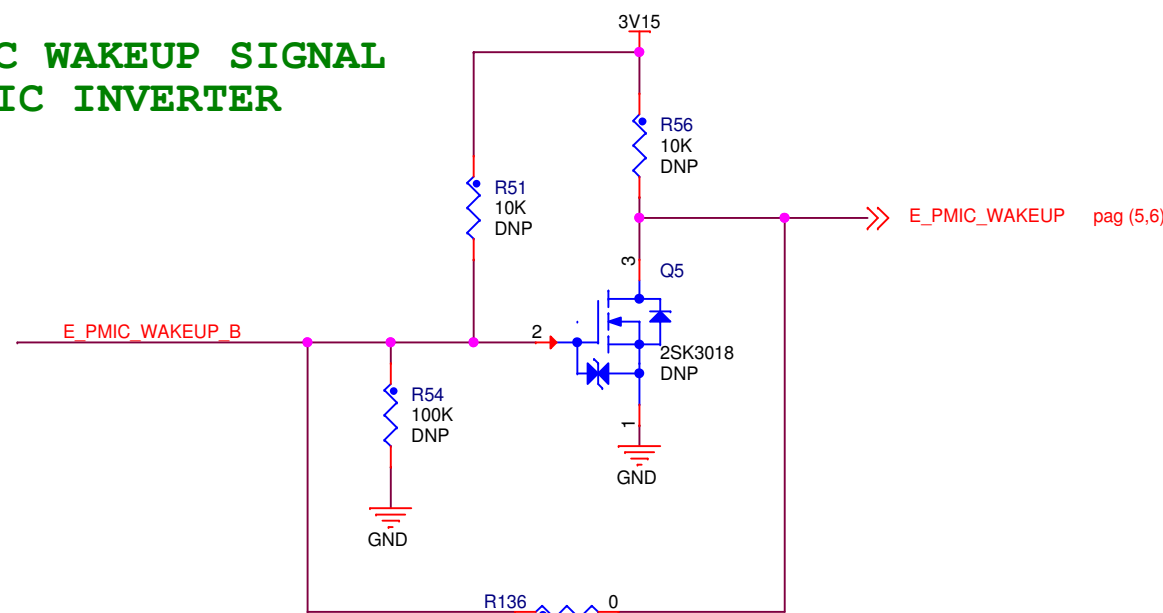
# EPDC Expansion Port



**"RESET"**

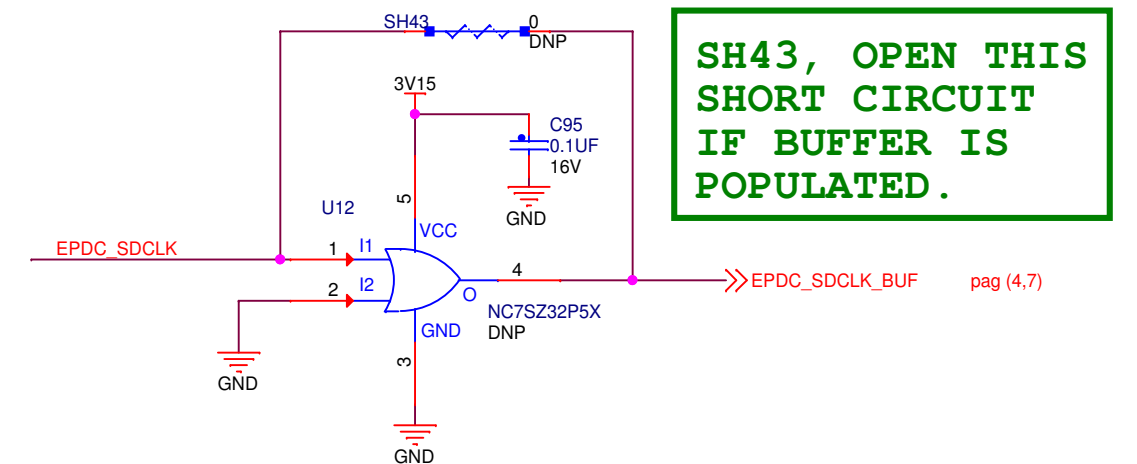
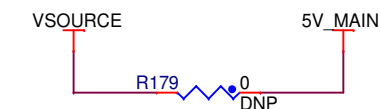
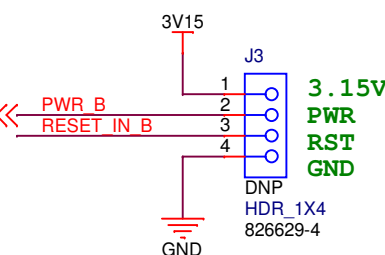


## PMIC WAKEUP SIGNAL LOGIC INVERTER



NOTE: Active low signal is currently inverted by software. DNP components provided if SW is changed to make signal active low again.

"J3" ADDITIONAL TESTPOINTS AVAILABLE FOR DEBUGGING. THE CONNECTOR IS DNP



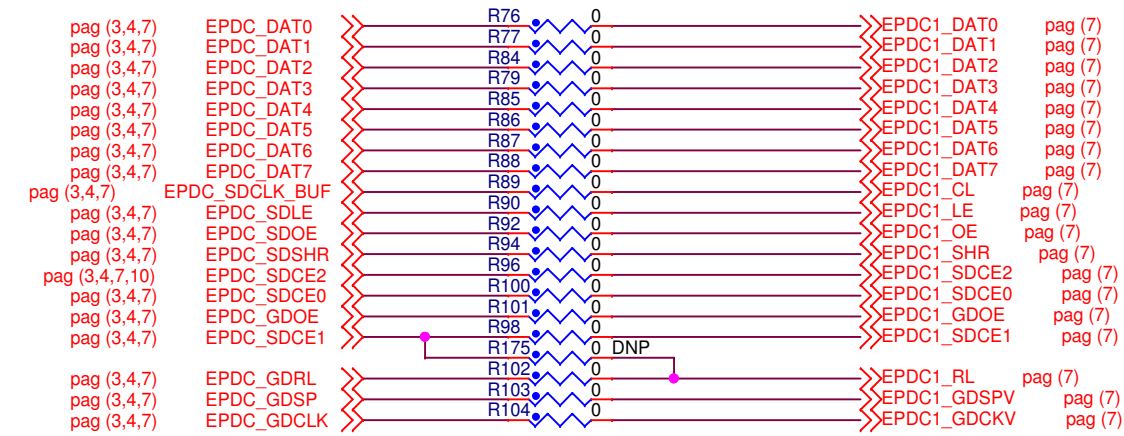
SH43, OPEN THIS SHORT CIRCUIT IF BUFFER IS POPULATED.

LAYOUT CONSTRAINTS  
KEEP THE NET EPDC\_SDCLK AS SHORT AS POSSIBLE  
LENGTH NET < 1000 mils.

ICAP Classification: FCP: FIUO: PUBI: X			
Drawing Title: IMXEBOOKDC3-E			
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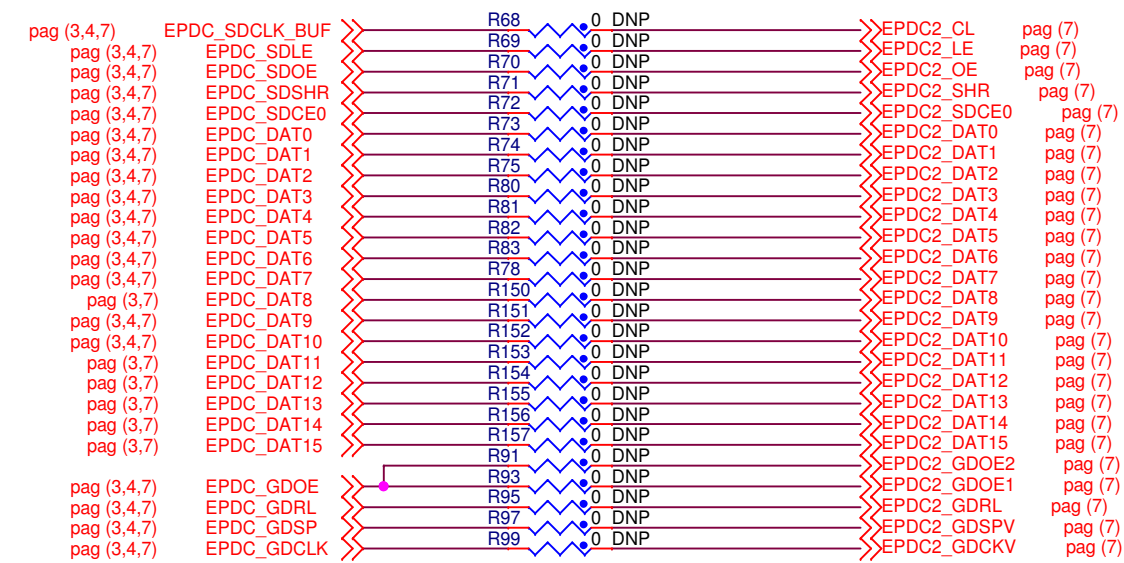
Connector Output Selectors

EPDC PORT FROM J1



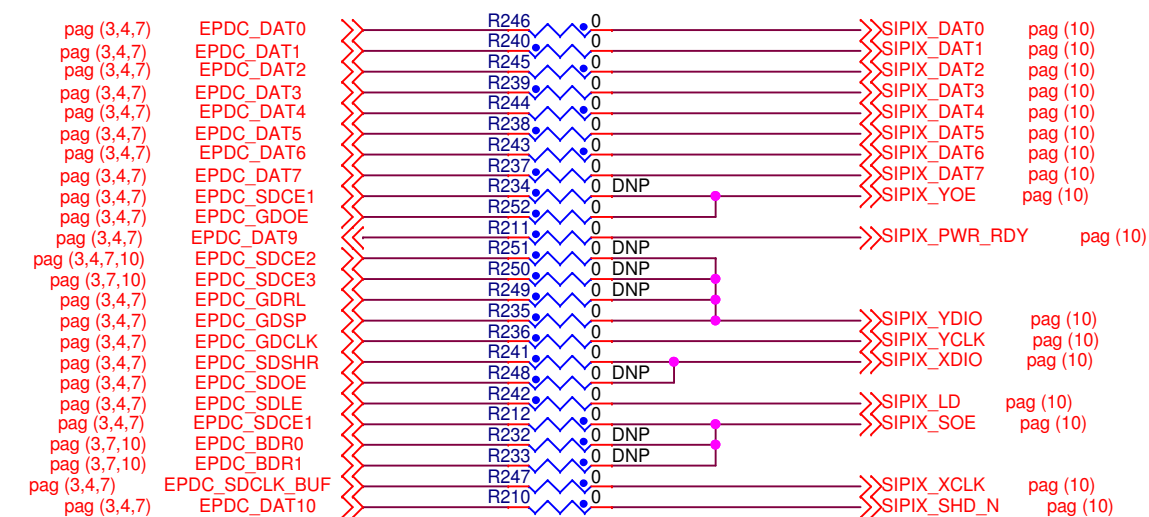
E-Ink  
J4 & J6

ED060SCM,  
ED060SCC,  
ED060SC7  
ED060SC4,  
ED060SC8,  
ED060SCD,  
LB060X01



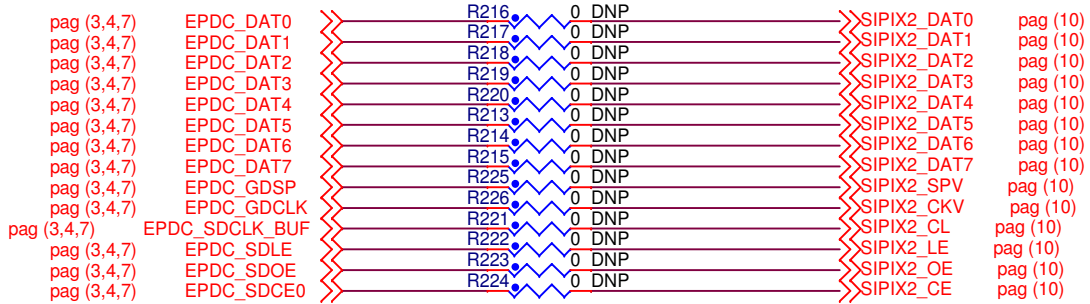
E-Ink  
J5 & J9

ED097OC1,  
ED097OC2 &  
ED097OC4  
EC097SC1,  
ED097OC5 &  
ED097OC6



Sipix  
J17

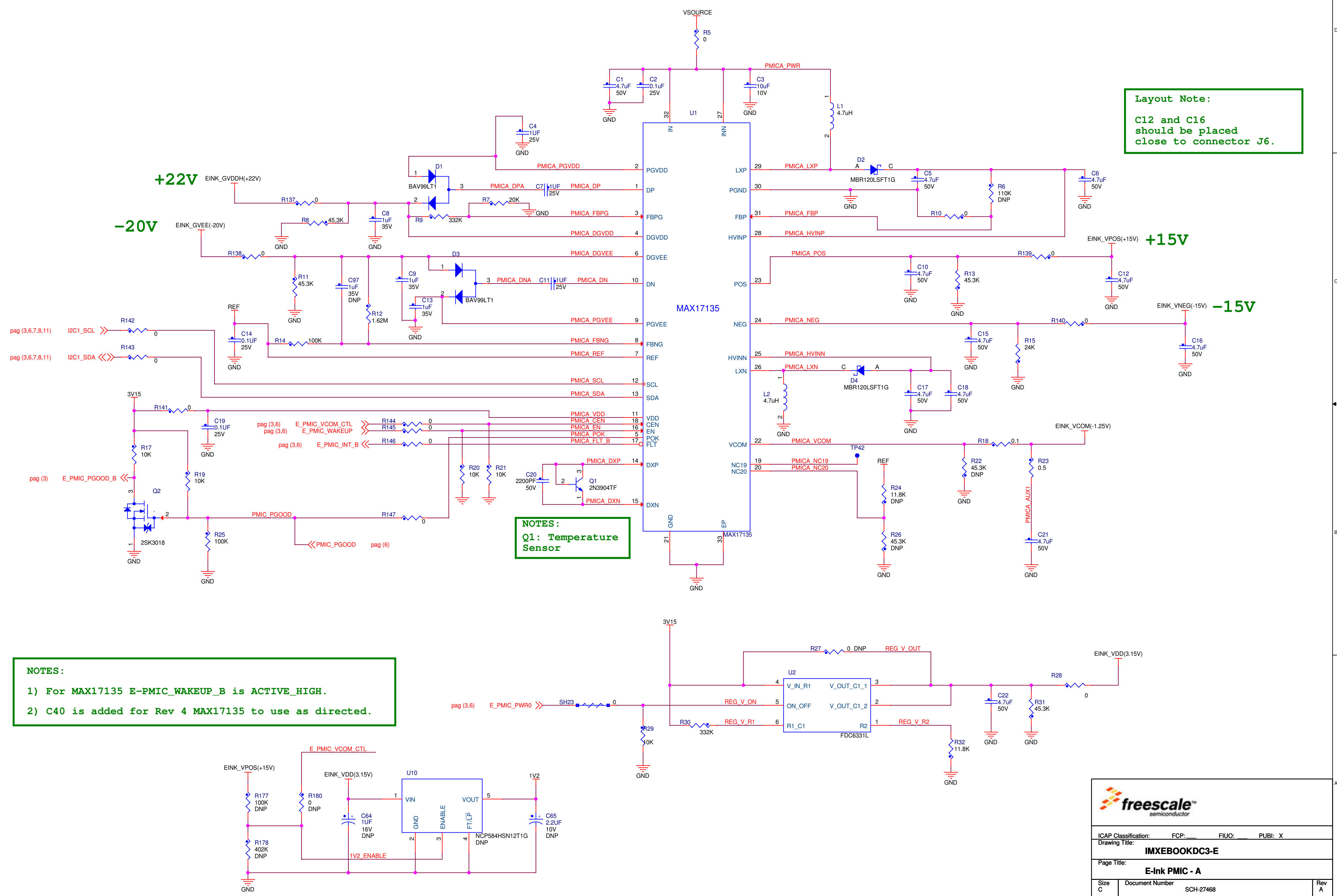
AUO  
A060SE03 &  
A060SE01



Sipix  
J18

LG LB060X03





**Layout Note:**  
C12 and C16  
should be placed  
close to connector J6.

**NOTES:**  
Q1: Temperature  
Sensor

**NOTES:**  
1) For MAX17135 E-PMIC\_WAKEUP\_B is ACTIVE\_HIGH.  
2) C40 is added for Rev 4 MAX17135 to use as directed.

```
NOTE: In order to use the TI PMIC:
Populate the following parts -
R33, R35, R36, R39, R40, R41, R49, R50,
R55, R59, R60, R63, R66, R67, RT1, U3
Depopulate the following parts -
R5, R18, R137, R138, R139, R140, R141,
R142, R143, R144, R145, R146, R147
```

pag (3,5) E\_PMIC\_VCOM\_CTL >> R55 0 DNP PMICB\_VCOM\_CTRL

R57 10K

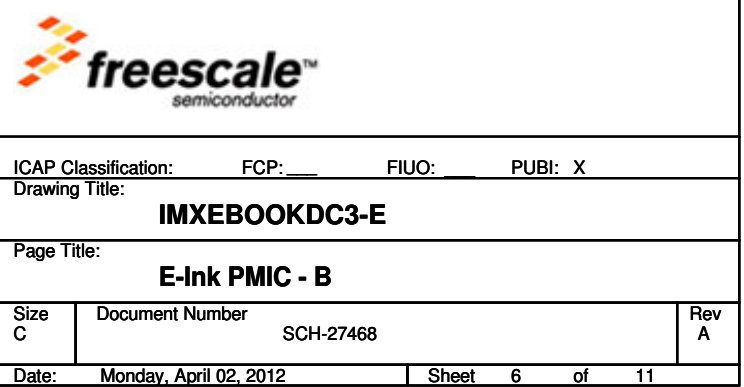
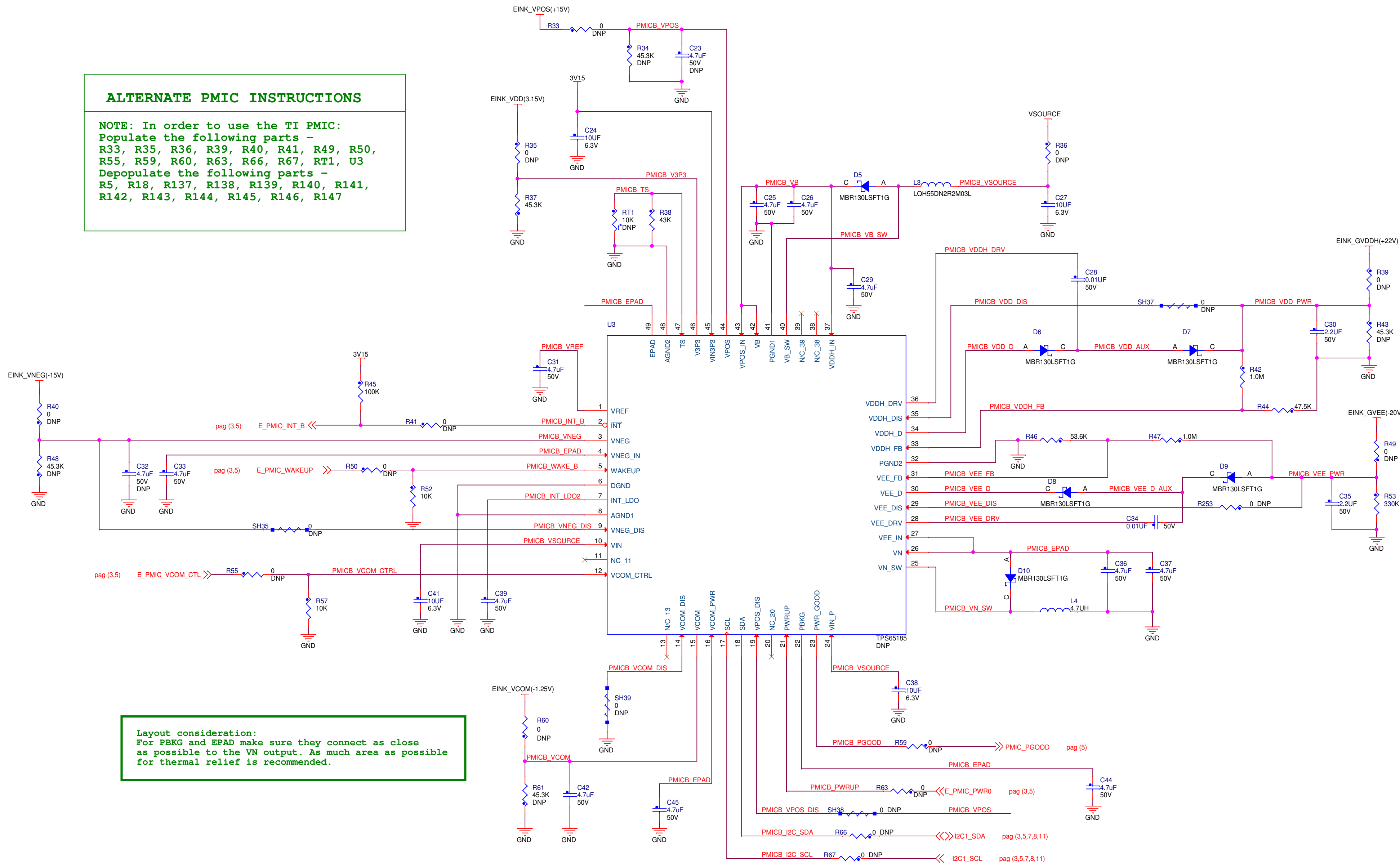
GND

C41 10UF 6.3V

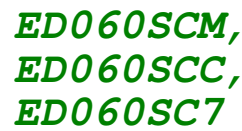
GND

GND

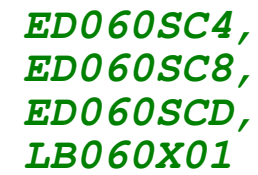
**Layout consideration:**  
For PBKG and EPAD make sure they connect as close as possible to the VN output. As much area as possible for thermal relief is recommended.



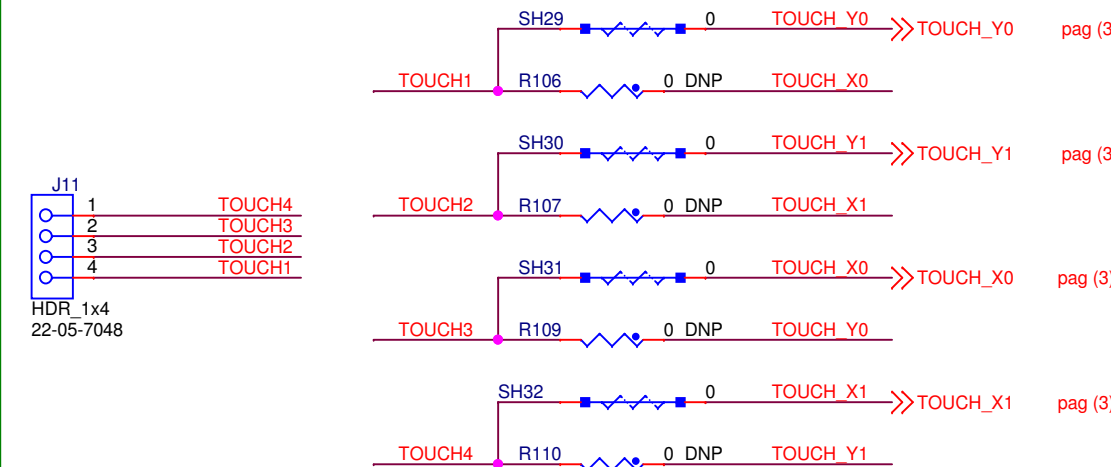
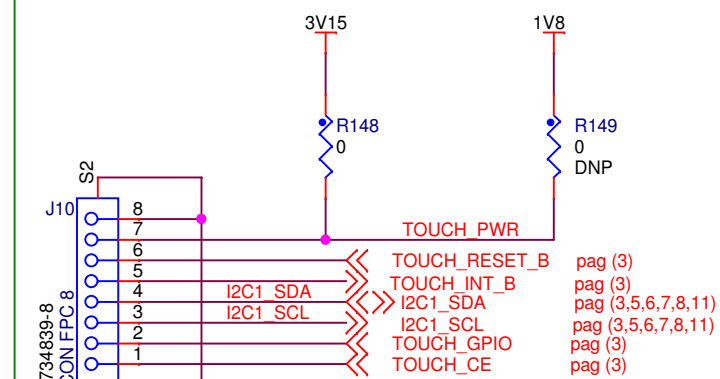
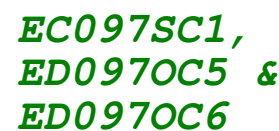
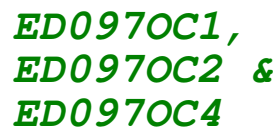
## 6.0" Connector



## 6.0" Connector



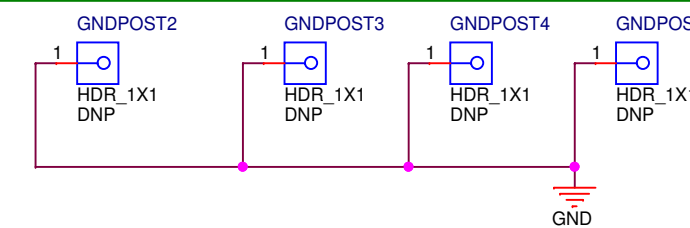
## 9.7" Connector



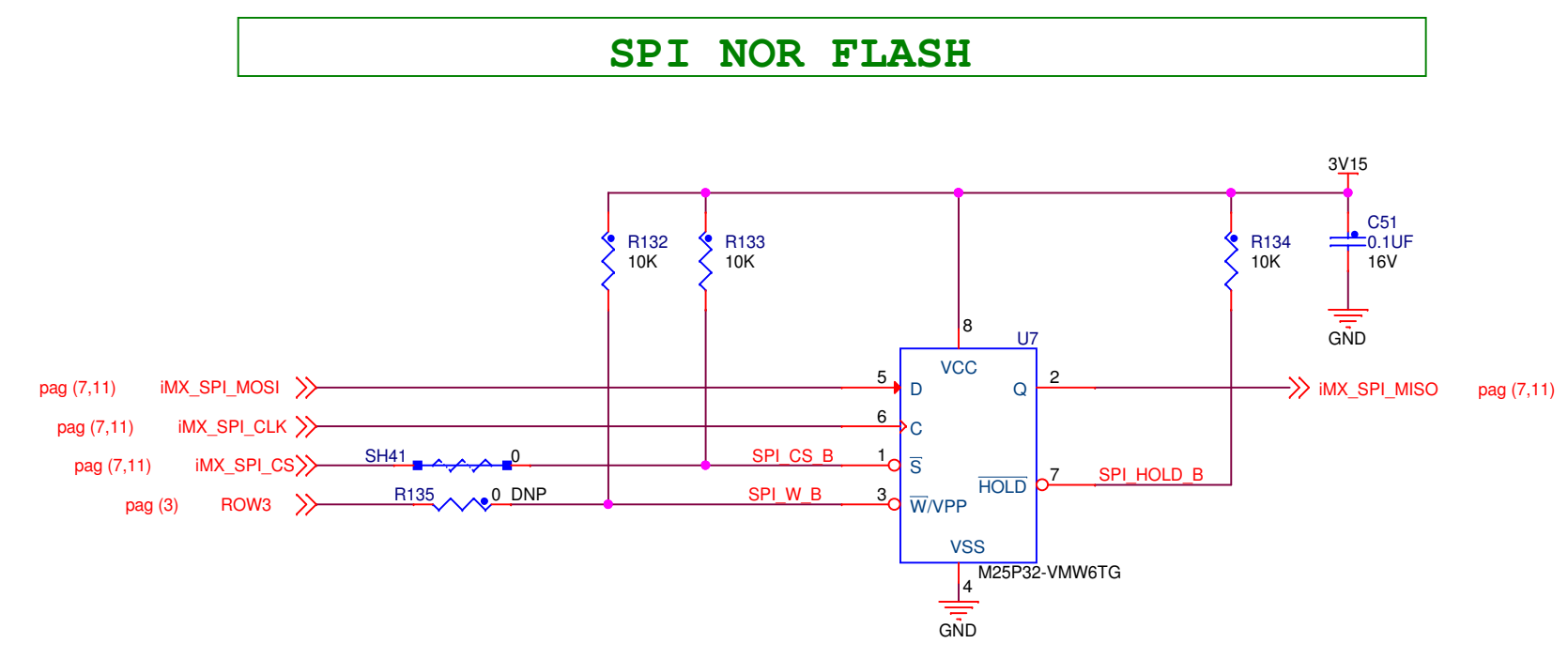
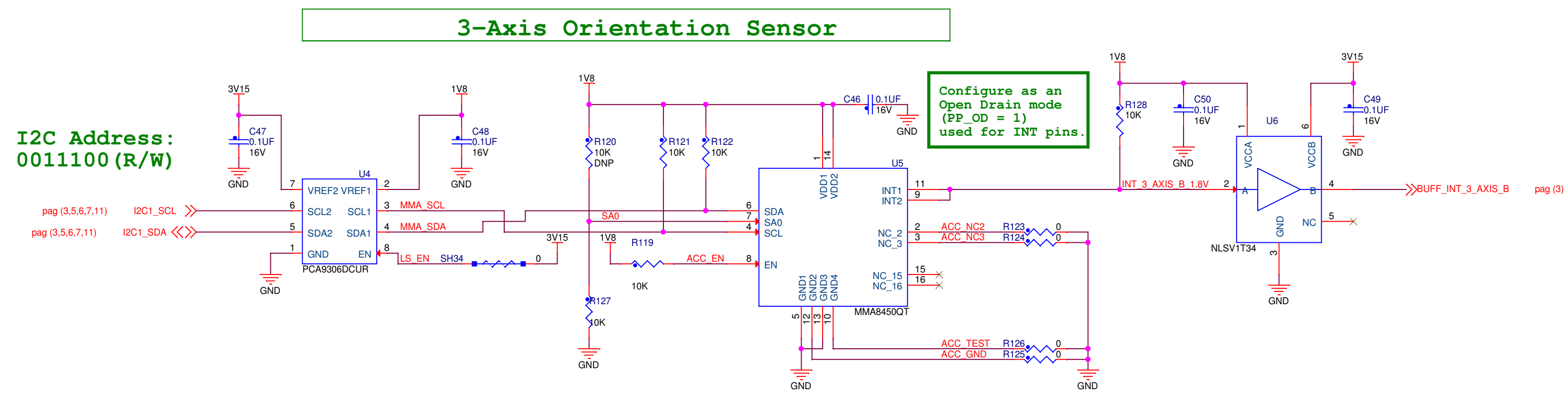
The schematic diagram illustrates the electrical connections for the EPDC module. It features two main connectors: J12 (TSW-120-07-S-D) and J14 (TSW-109-07-S-D). The EPDC module is connected to J12 via a ribbon cable, with pins 1 through 40 labeled. The TOUCH module is connected to J14 via a ribbon cable, with pins 1 through 18 labeled. The IMX SPI module is connected to the EPDC module via a ribbon cable, with pins 1 through 18 labeled. The diagram also shows various power and ground connections, including 5V\_MAIN, 3V15, and EINK\_VDD(+3.15V). The EPDC module is connected to the IMX SPI module via a ribbon cable, with pins 1 through 18 labeled. The diagram also shows various power and ground connections, including 5V\_MAIN, 3V15, and EINK\_VDD(+3.15V).

**Additional J14 connector for Power & Serial communication signals.**

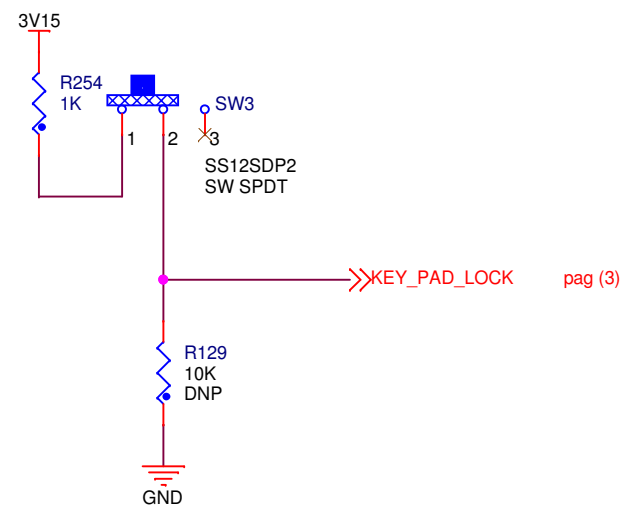
## GND Posts



ICAP Classification:		FCP: _____	FIUO: _____	PUBI: X
Drawing Title:				
<b>IMXEBOOKDC3-E</b>				
Page Title:				
<b>Level Shifters and E-Ink Display</b>				
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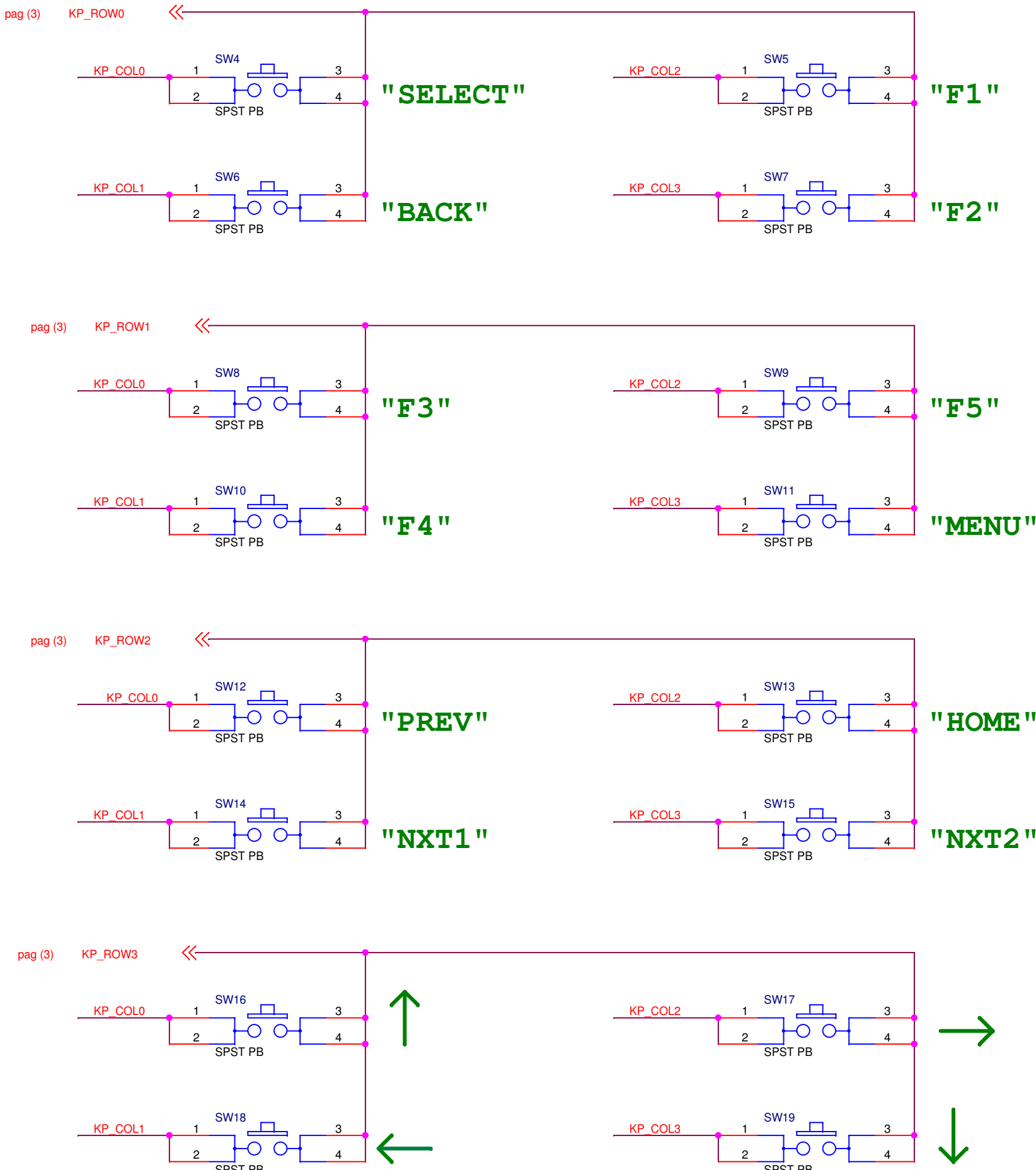
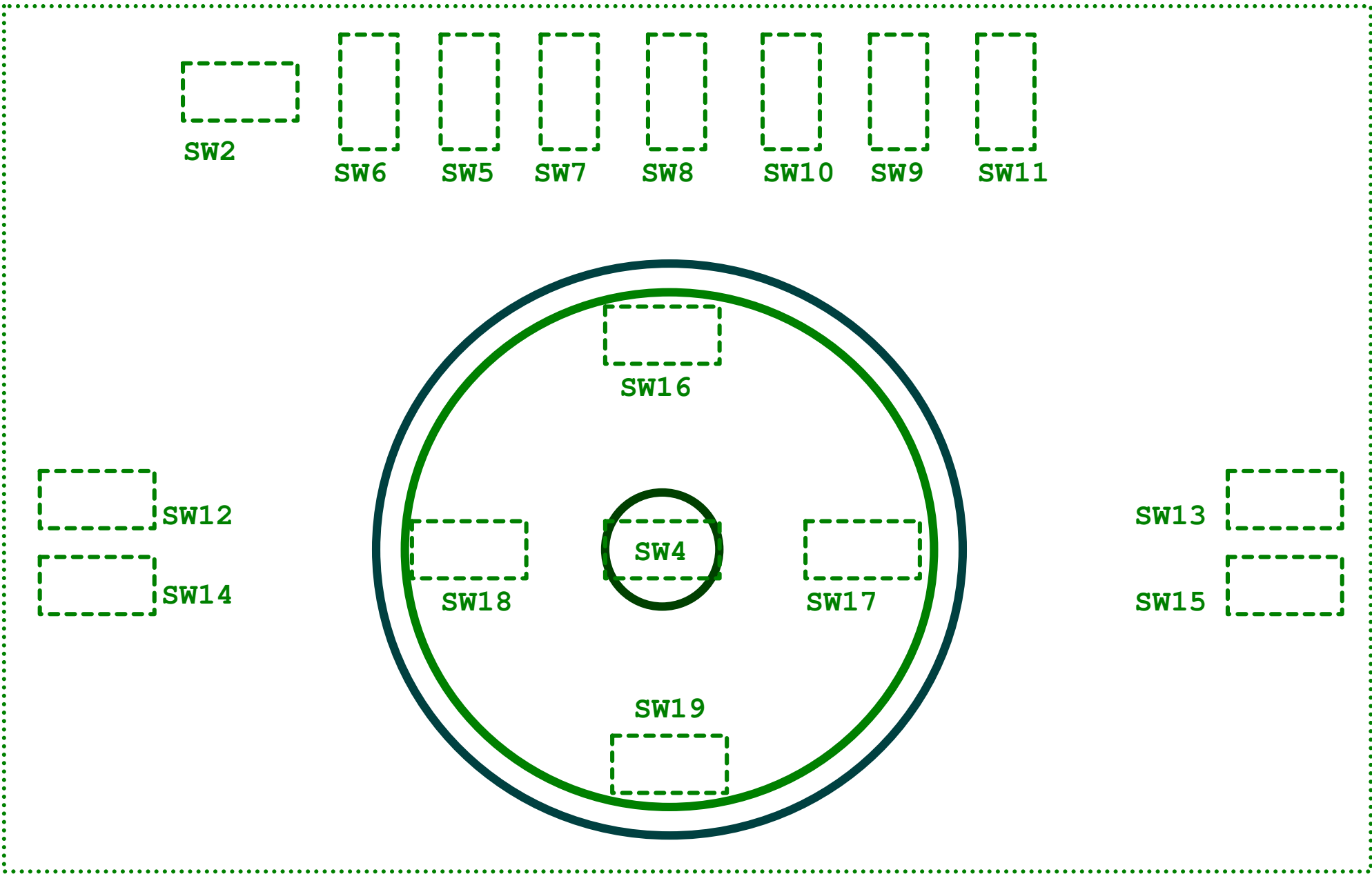






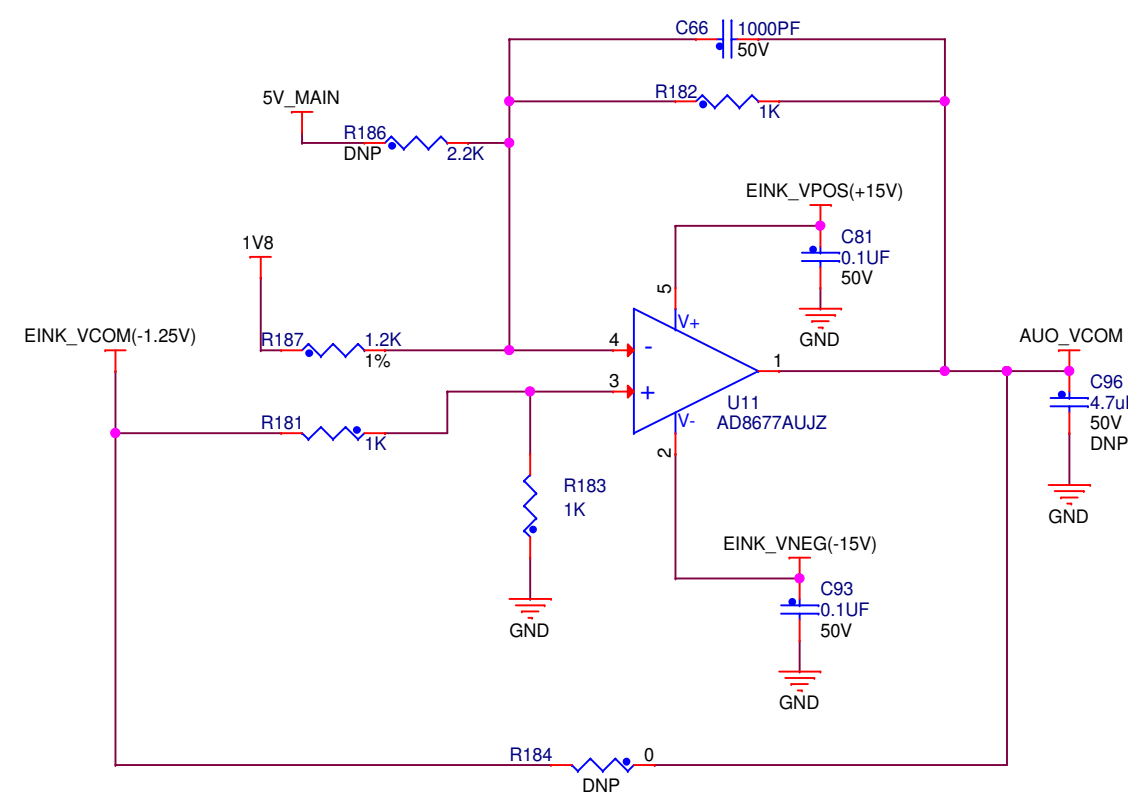
pag (3) KP\_COL0 << KP\_COL0  
pag (3) KP\_COL1 << KP\_COL1  
pag (3) KP\_COL2 << KP\_COL2  
pag (3) KP\_COL3 << KP\_COL3

# LAYOUT RECOMENDATIONS FOR SW4 TO SW19 & RESET (SW2).



ICAP Classification: FCP: FIUO: PUBI: X		
Drawing Title: IMXEBOOKDC3-E		
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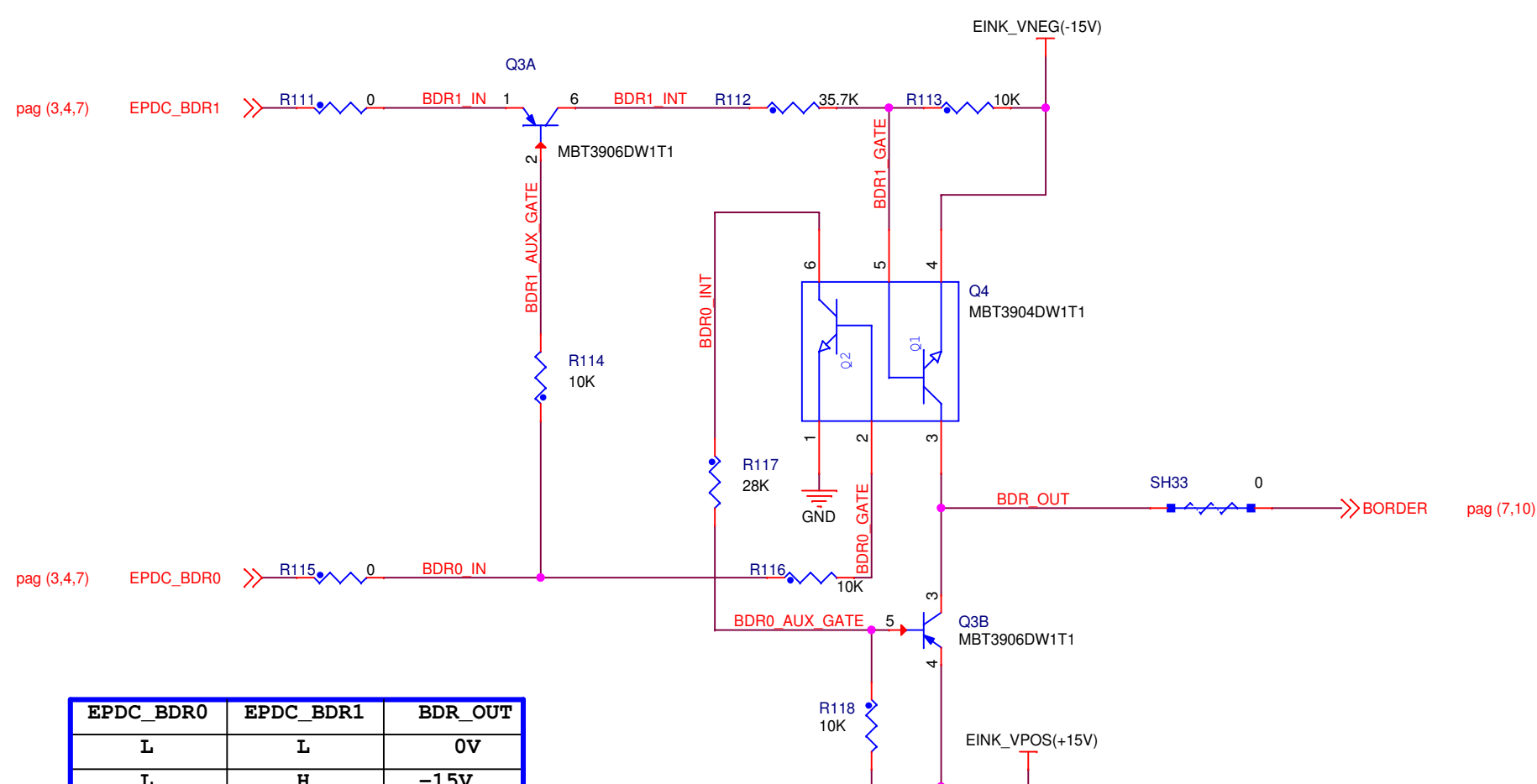
## VCOM Shifter Subtractor



$$V_{out} = V_{com} \left( \frac{(R182+R181)*R183}{(R183+R187)*R181} \right) - 1.8V \left( \frac{R182}{R181} \right)$$

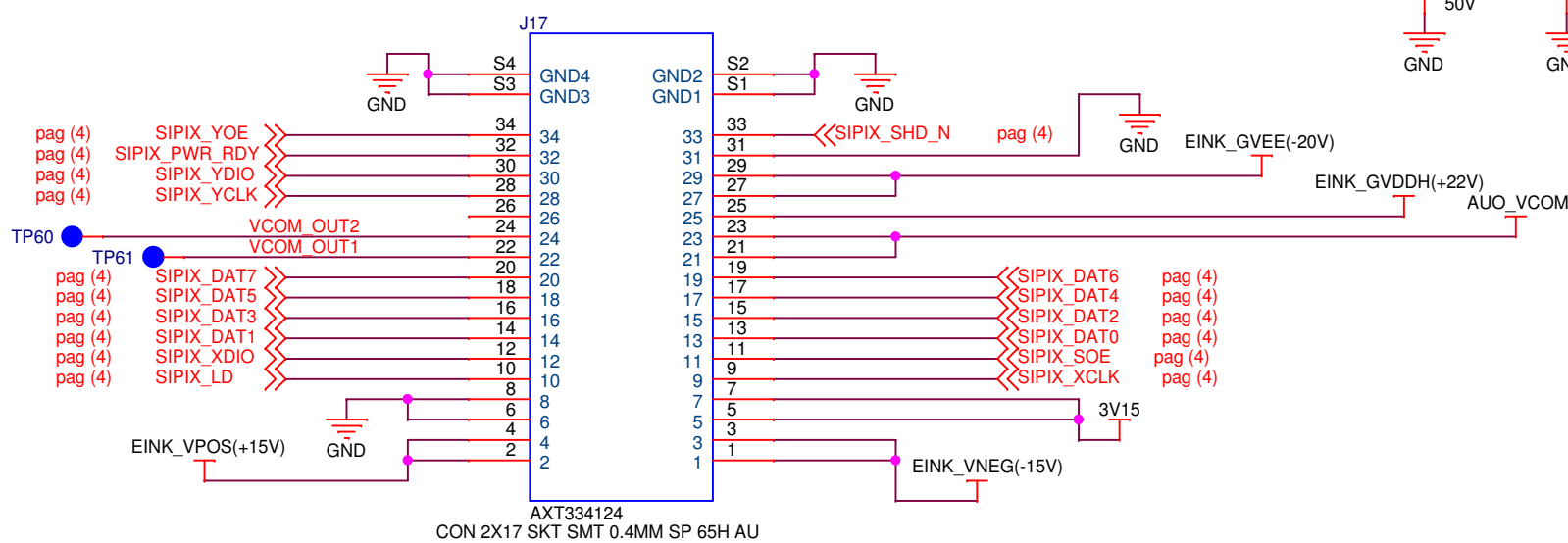
Min for EINK\_Vcom = -0.5V  
 AUO\_Vcom = -1.958V  
 Max for EINK\_Vcom = -3.05V  
 AUO\_Vcom = -4.293V

NOTE:  
 Max Requirements for AUO\_Vcom:  
 Current 9.2mA  
 Range Voltage: -4.0 to -2.0 Volts  
 AD8677  
 Current Drain Max 15mA



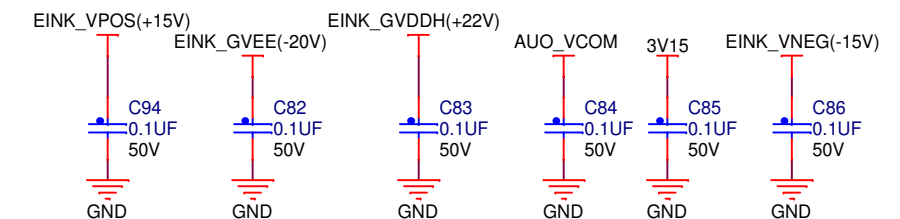
EPDC_BDR0	EPDC_BDR1	BDR_OUT
L	L	0V
L	H	-15V
H	L	15V
H	H	15V

## AUO A060SE03 & A060SE01

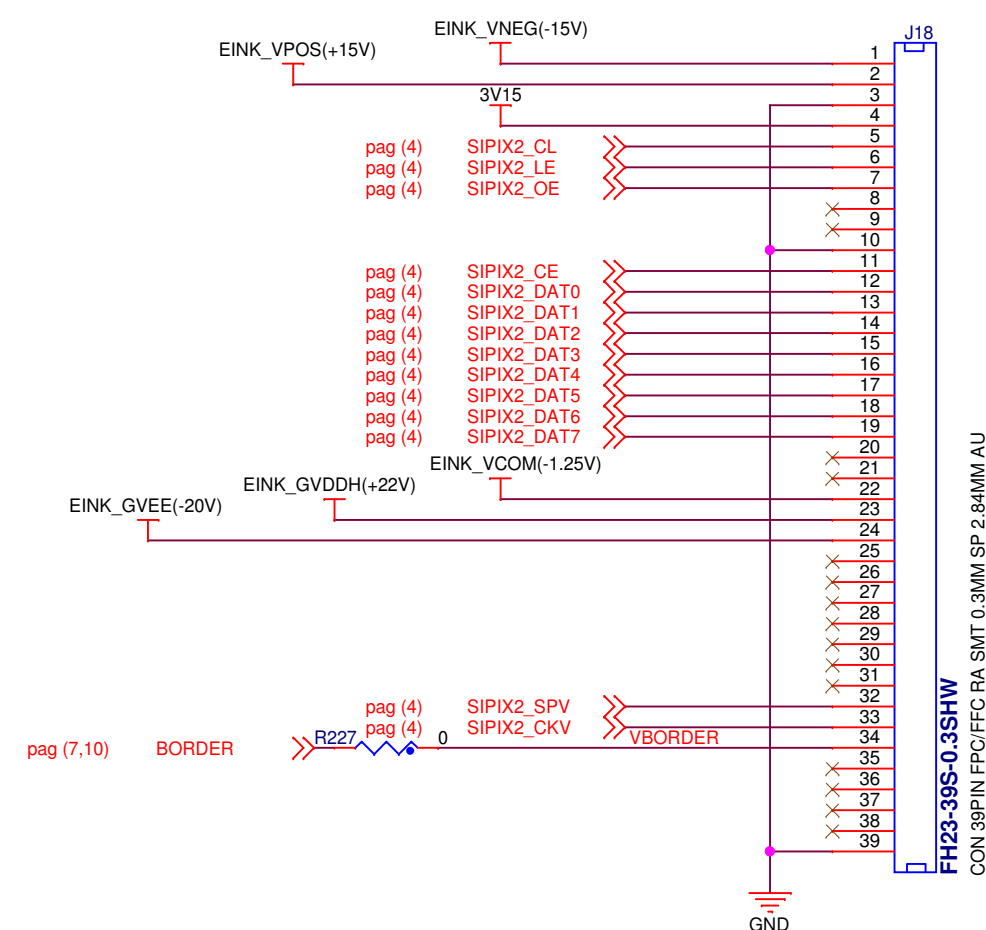


NOTE:  
 Next are GPIOs:  
 EPDC\_DAT9 => iMX as Input  
 EPDC\_DAT10 => iMX as Output

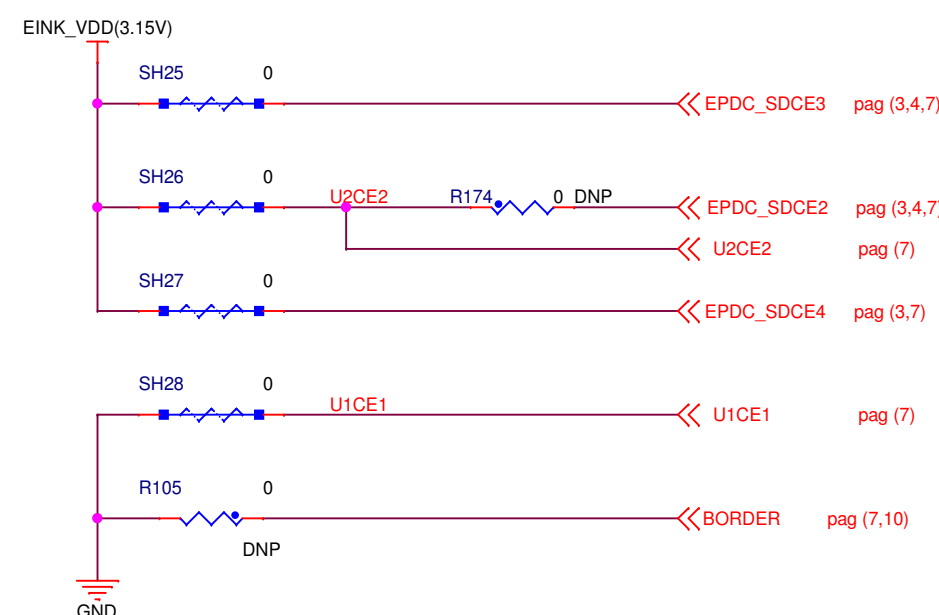
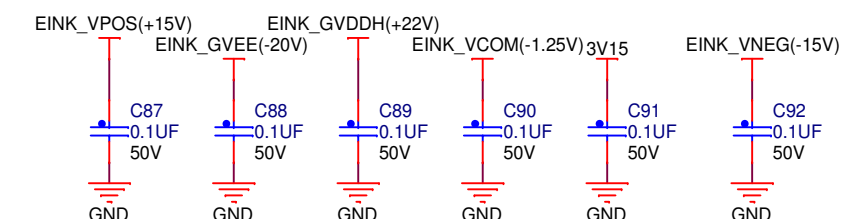
Layout Consideration  
 Close to J17



## LG LB060X03

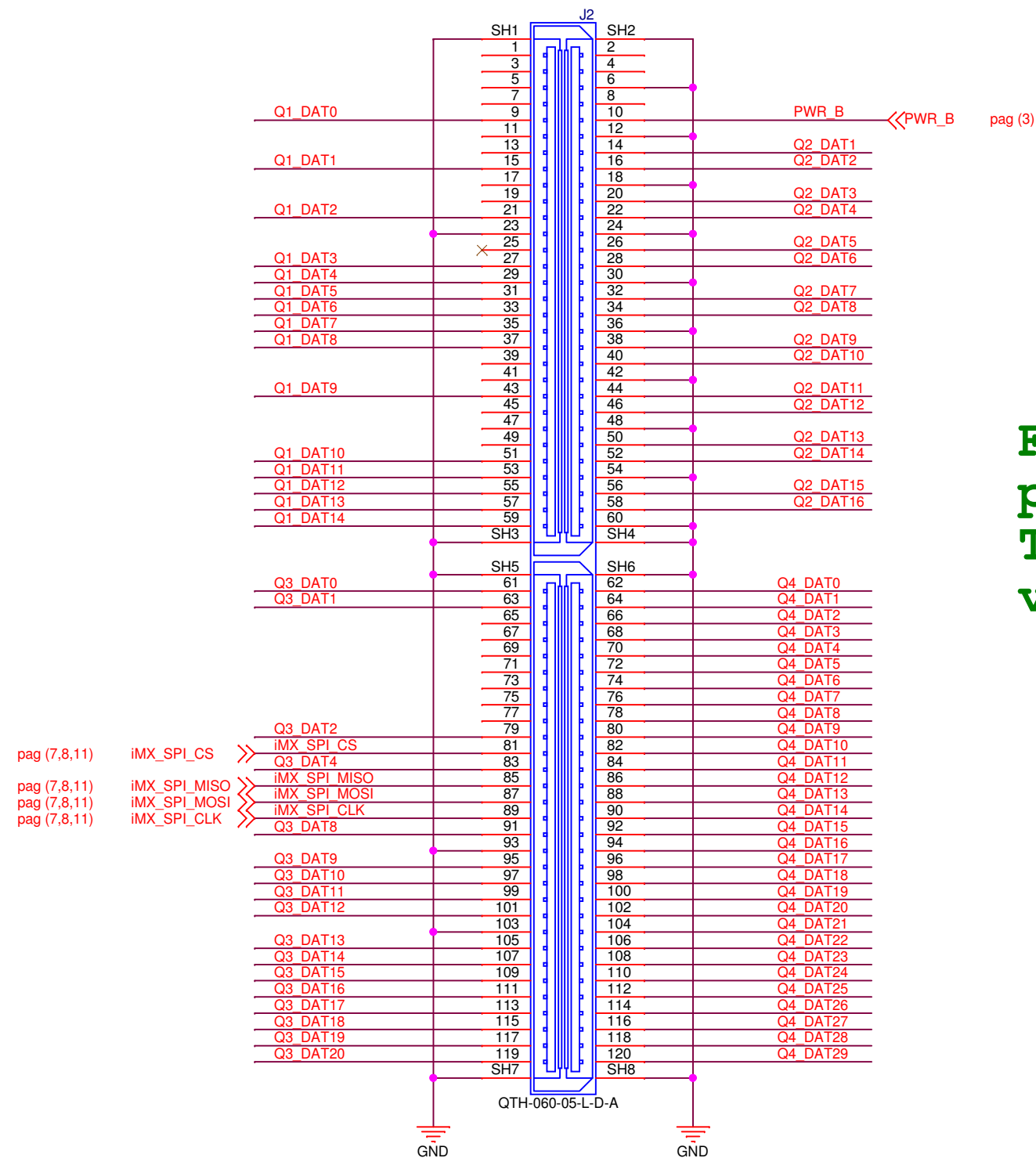


Layout Consideration  
 Close to J18



## LCD Expansion Port

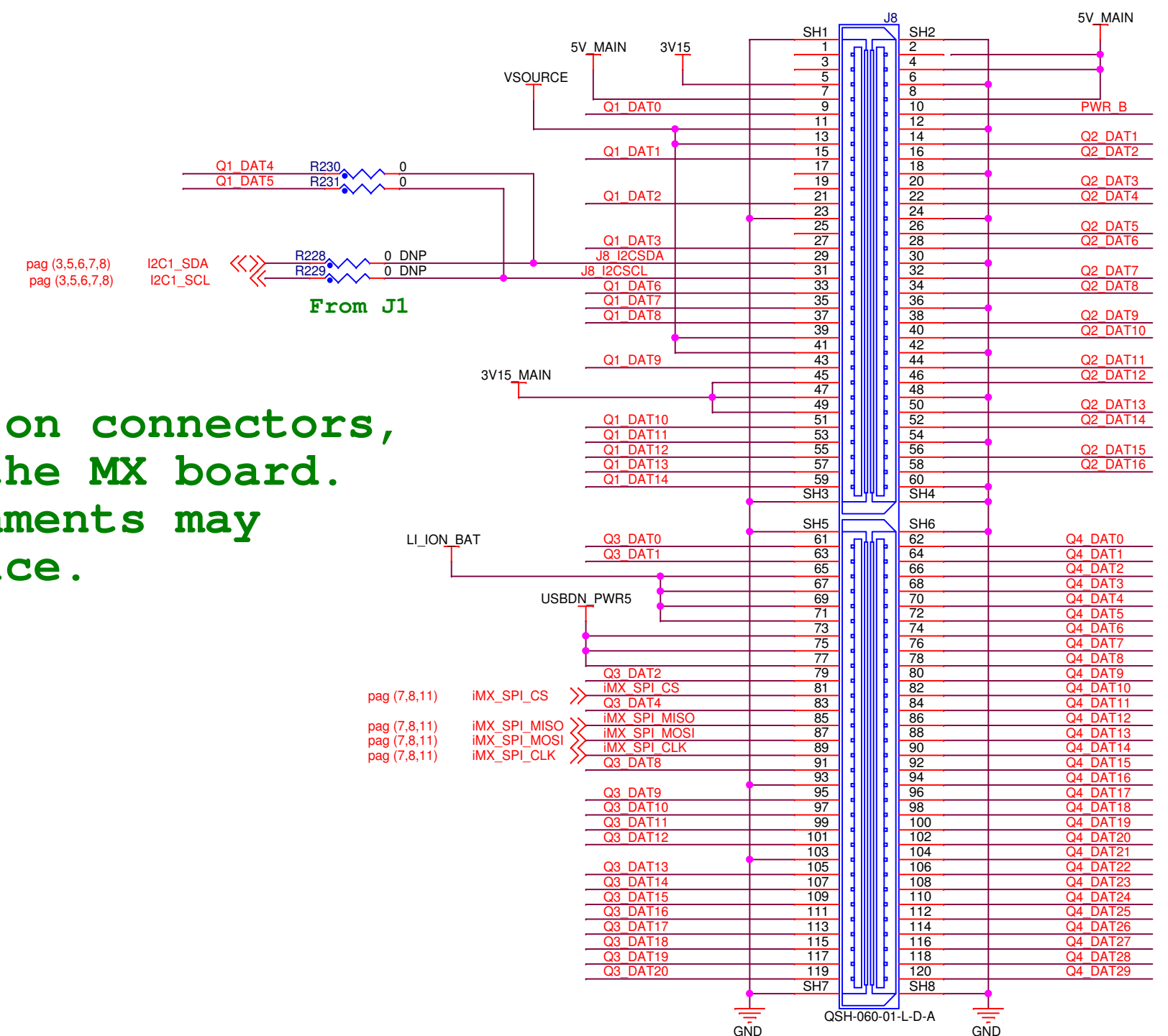
### Bottom Layer



For signal names on connectors,  
please refer to the MX board.  
The signal assignments may  
vary by i.MX device.

## LCD Pass-Through Signals

### Top Layer



ICAP Classification: FCP: FIUO: X PUBI:	
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