Verilog Code for Half Adder Data Flow Model

```
module hadd(
   input A,B,
   output S,C
   );
   assign S = A ^ B;
   assign C = A & B;
endmodule
```

Verilog Code for Half Adder Behavioral Model

```
module hadd(A,B,S,C);
input wire A,B;
output reg S,C;
always @(A or B)
begin
if (A==0 && B==0)
begin
S = 0;
C =0;
end
if (A==0 && B==1)
begin
S = 1;
C =0;
end
if (A==1 && B==0)
begin
S = 1;
C =0;
end
if (A==1 && B==1)
begin
S = 0;
C =1;
end
end
endmodule
```

Verilog Code for Half Adder Structural Model

```
module hadd(
   input A,B,
   output S,C
   );
   xor xor1 (S,A,B);
   and and1 (C,A,B);
endmodule
```