

PROGRESS

Slowing down the target to Single SPI allows capture, showing the SoC accessing the payload at **0x1d4744**

| CMD | ADDRESS | DATA |
|-------------------|----------|--|
| NORMAL READ(0X03) | 1D 47 44 | 00 BF 00 BF 00 BF 00 BF |
| NORMAL READ(0X03) | 1D 47 60 | 00 BF 00 BF 00 BF 00 BF |

ABSOLUTELY NOT BUSSIN

SPI “Auto” Mode

- Execute-in-Place (XiP)
- On-the-fly Decryption (start/end address configuration)
- Read Only

SPI “Manual” Mode

- Read/Write
- No On-the-fly Decryption

- Auto Mode: up-to 32 Mbyte transparent Code access for XIP (Execute-In-Place) and Data access with 3-byte and 4-byte addressing modes
- Manual Mode: Direct register access using the QSPIC register file
- Decrypt on-the-fly (AES-256b-CTR) capability while in auto mode operation