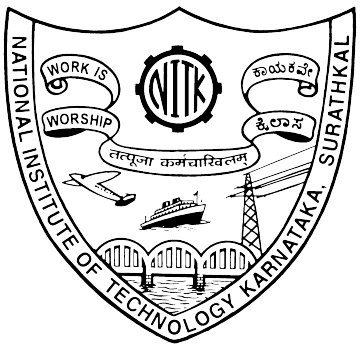

National Institute of Technology Karnataka,
Surathkal

EC372

VLSI Design Lab

VLSI Design Lab Report

Authors:
Anirudh BH 16EC105
Manan Sharma 16EC118

Supervisor:
Dr. Ramesh Kini

April 17, 2019

Contents

1 Study of MOS Inverter with Resistive Load **2**
1.1 Objective . . . 2
1.2 Introduction . . . 2
1.3 Circuit Diagram . . . 2
1.4 Netlist . . . 2
1.5 Simulation Results, Analysis and Observations . . . 3
1.5.1 Variation of R_L . . . 3
1.5.2 Variation of NMOS W . . . 5
1.5.3 Variation of NMOS L . . . 7
1.5.4 Variation of C_L . . . 9
1.6 Conclusion . . . 11

2 CMOS Inverter Layout and Characterisation **12**
2.1 Aim . . . 12
2.2 Circuit Diagram . . . 12
2.3 Introduction . . . 12
2.4 Layout . . . 13
2.5 Expected Netlist . . . 13
2.6 Netlist extracted from Magic . . . 13
2.7 Analysis and Observation . . . 14
2.8 Conclusion . . . 15

1 Study of MOS Inverter with Resistive Load

1.1 Objective

To study the:

1. Transfer Function
2. Noise Margin
3. Risetime and Fall time
4. Propagation Delay
5. Power and Energy consumed

with variation in R_L and W of the load resistor and pull-down transistor. Along with this, also calculate power and energy consumed for non ideal step input for resistive load inverter.

1.2 Introduction

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has logic level 0 and vice-versa. A resistive load inverter is characterised by an resistive load between the pull down transistor and the voltage source. The output is taken at the junction of the load resistance and the pull down transistor. The pull-up circuit is constituted by the resistor and pull-down resistor by the NMOS. When the input is low, the NMOS is open circuited and the output capacitance is charged to V_{DD} through R_L.

1.3 Circuit Diagram

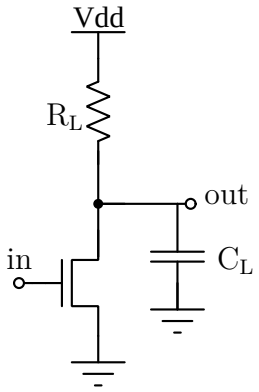

Figure 1: Circuit Diagram of Resistive Load Inverter

1.4 Netlist

```
* transistor and other circuit components definition
m0 out in 0 0 cmosn l=2.5u w=10u
rl supply out 7k
cl out meas 5n
```

```
* voltage source
vdd supply 0 dc 3.3
vin in 0 dc 3.3 pulse(0 3.3 0 0.1n 0.1n 0.5m 1m)
vcap meas 0 dc 0
```

1.5 Simulation Results, Analysis and Observations

Transfer characteristics were plotted for different values of R_L and different W and L values for the driver NMOS. The plots obtained were as follows:

1.5.1 Variation of R_L

The curves moving to the right imply that the threshold voltage is increasing and moving to the right. Figure(2) indicates that as R_L increases the voltage drop across it increases. This implies that the graph moves to the left as R_L increases.
Figure(3) indicates that as R_L increases the pull up resistance to the load increases. This results in the rise time increasing for an increase in R_L.
Figure(4) indicates that as R_L. increases the peak current drawn by the capacitor decreases. Figure(5) indicates that the current drawn from V_{DD} is the same. Table 1 contains the changes in both DC and Transient parameters.

Resistance	5kΩ	7kΩ	10kΩ
V_{OH}	3.3V	3.3V	3.3V
V_{OL}	0.347V	0.248V	0.173V
V_{IL}	0.661V	0.583V	0.528V
V_{IH}	1.768V	1.572V	1.39V
NM_H	1.532V	1.728V	1.91V
NM_L	0.314V	0.335V	0.355V
t_{rise}	51.83μs	73.6μs	0.109ms
t_{fall}	10μs	9.935μs	9.691μs
t_{PLH}	17.9μs	24.97μs	34.6μs
t_{PHL}	4.417μs	4.43μs	4.455μs
t_d	11.15μs	14.7μs	19.52μs
P_{avg}	1.01mW	0.762mW	0.561mW

Table 1: Effect of varying R_L on various DC and Transient Parameters

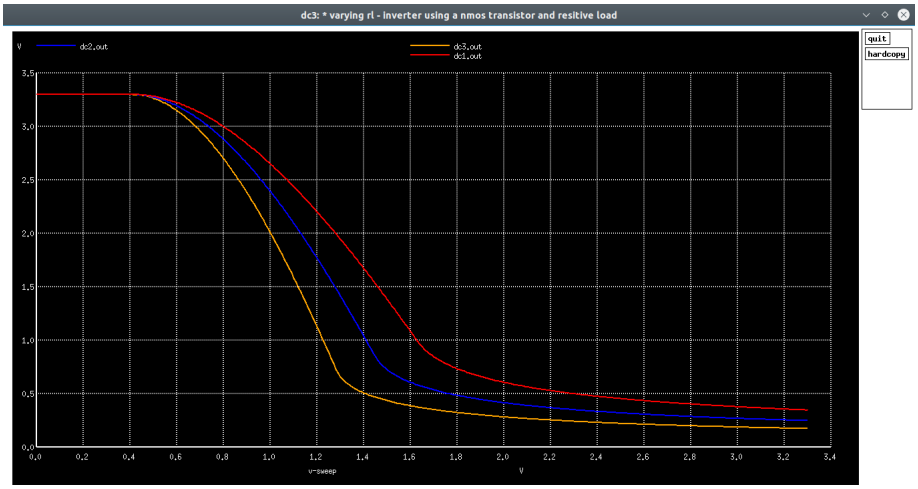

Figure 2: Transfer Characteristics Varying R_L(left to right: 10K, 7K, 5K)

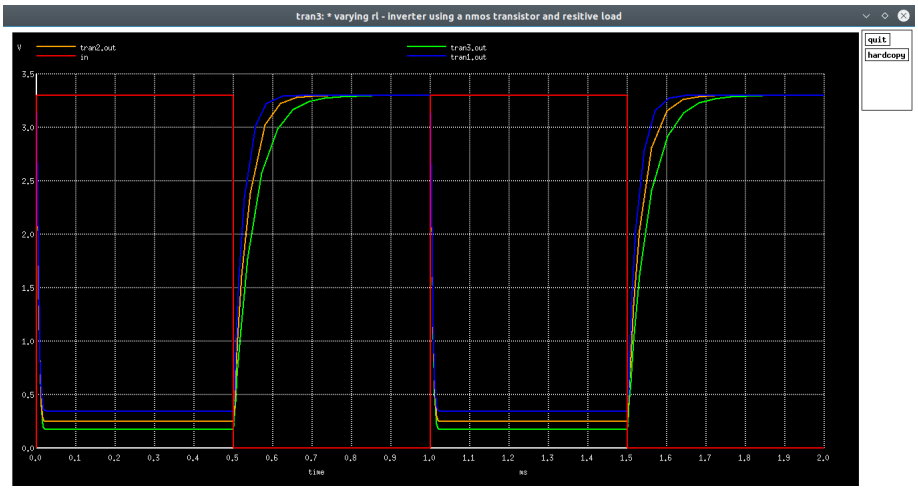

Figure 3: Transient Response Varying R_L(left to right: 5K, 7K, 10K)

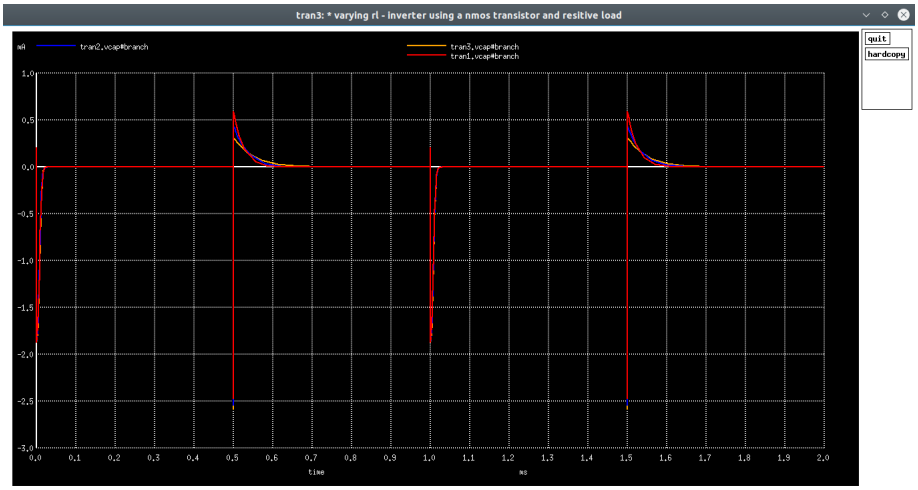

Figure 4: Capacitor Current Varying R_L

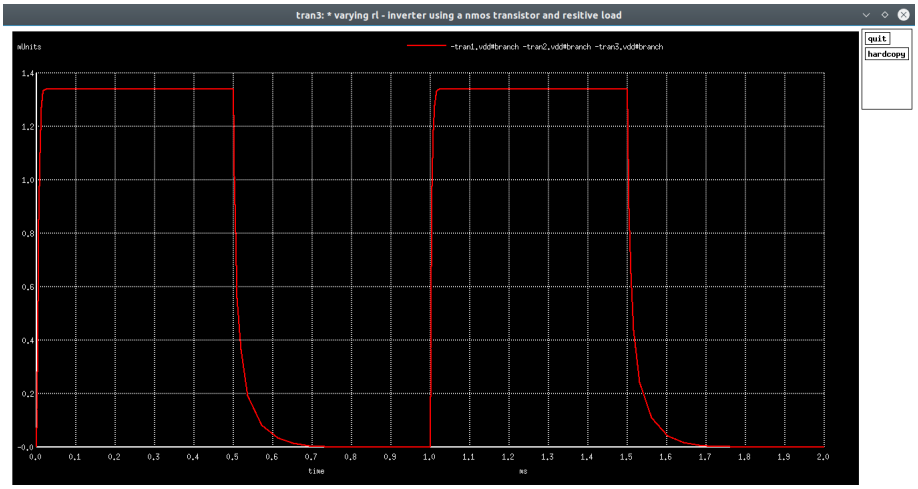

Figure 5: I_{DS} on Varying R_L

1.5.2 Variation of NMOS W

Figure(6) indicates that as W increases the voltage drop across the load R_L increases. This implies that the graph moves to the left as W increases.
Figure(7) indicates that as W increases the pull-down resistance to the ground decreases. This results in the rise time decreaseing for an increase in W.
Figure(8) indicates that as W increases the peak current drawn by the capacitor increases.
Figure(9) indicates that the current drawn from V_{DD} is the same. Table 2 contains the changes in both DC and Transient parameters.

W	5μ	10μ	20μ
V_{OH}	3.3V	3.3V	3.3V
V_{OL}	0.497V	0.248V	0.123V
V_{IL}	0.791V	0.58V	0.493V
V_{IH}	2V	1.57V	1.24V
NM_H	1.3V	1.73V	2.06V
NM_L	0.294V	0.332V	0.37V
t_{rise}	75.21μs	73.64μs	72.45μs
t_{fall}	20.02μs	9.935μs	4.82μs
t_{PLH}	24.81μs	24.97μs	25.15μs
t_{PHL}	8.56μs	4.43μs	2.22μs
t_d	16.685μs	14.4μs	13.685μs
P_{avg}	0.693mW	0.762mW	0.797mW

Table 2: Effect of varying W on various DC and Transient Parameters

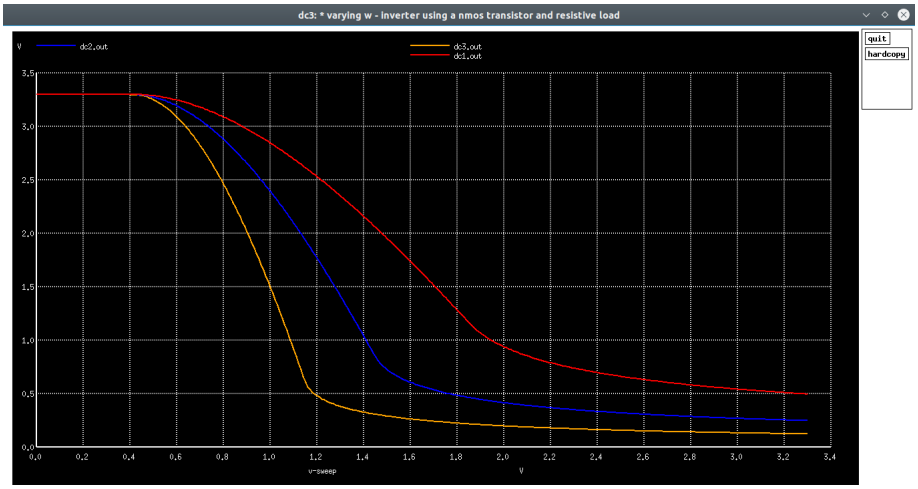

Figure 6: Transfer Characteristics Varying W

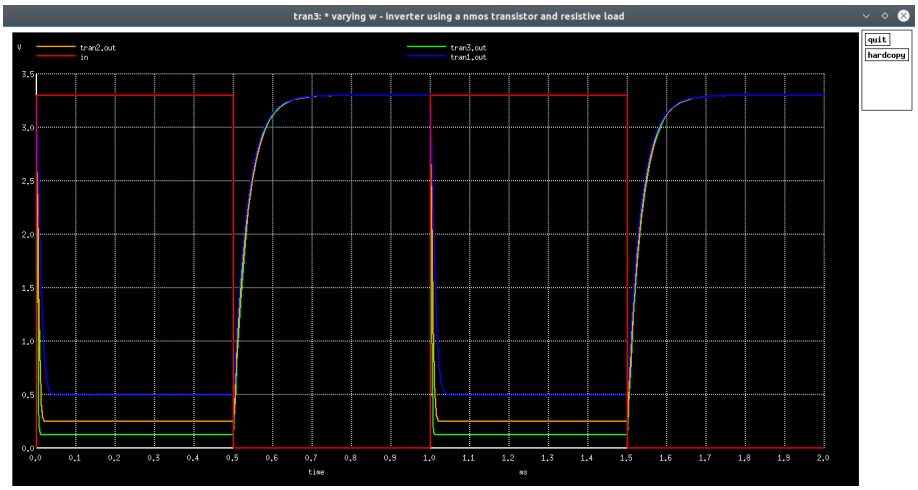

Figure 7: I_{DS} on Varying W

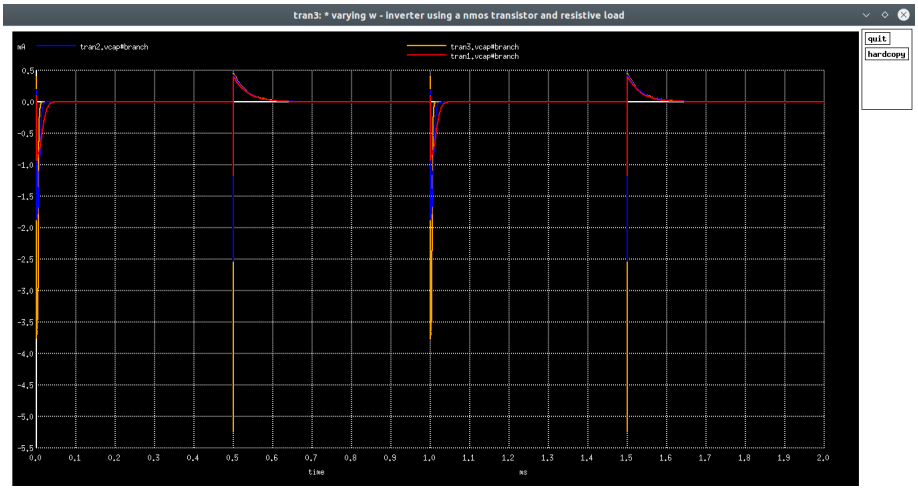

Figure 8: Capacitor Current Varying W

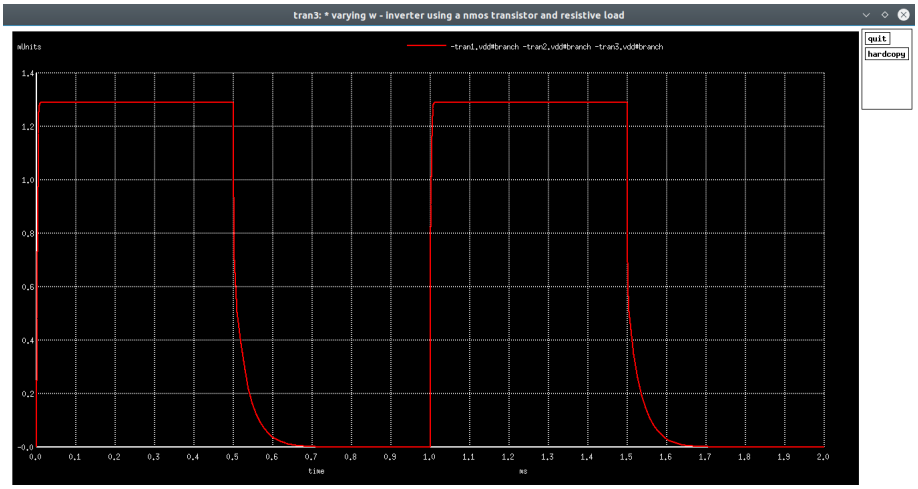

Figure 9: Transient Response Varying W

1.5.3 Variation of NMOS L

Figure(10) indicates that as L increases, the current decreases and the voltage drop across the load R_L decreases. This implies that the graph moves to the right as L increases.
Figure(11) indicates that as L increases the pull-down resistance to the ground increases. This results in the rise time increasing for an increase in L.
Figure(13) indicates that the current drawn from V_{DD} is the same. Table 3 contains the changes in both DC and Transient parameters.

L	1μ	2.5μ	10μ
V_{OH}	3.3V	3.3V	3.3V
V_{OL}	0.1V	0.248V	0.9V
V_{IL}	0.455V	0.583V	1.24V
V_{IH}	1.18V	1.57V	2.34V
NM_H	2.12V	1.73V	0.96V
NM_L	0.355V	0.335V	0.34V
t_{rise}	74.31μs	73.64μs	78.28μs
t_{fall}	4.89μs	9.935μs	32.62μs
t_{PLH}	25.15μs	24.97μs	24.209μs
t_{PHL}	2.32μs	4.43μs	12.79μs
t_d	13.73μs	14.7μs	18.499μs
P_{avg}	0.803mW	0.762mW	0.587mW

Table 3: Effect of varying L on various DC and Transient Parameters

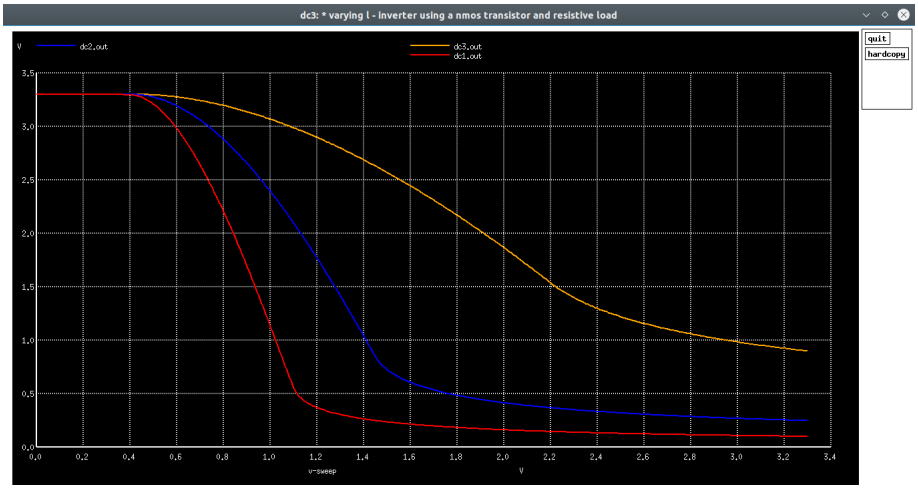

Figure 10: Transfer Characteristics Varying L

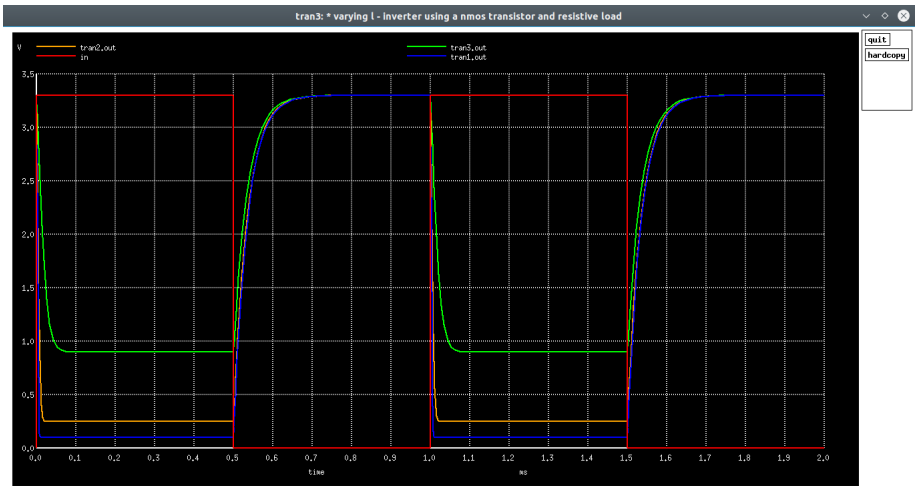

Figure 11: Transient Response Varying L

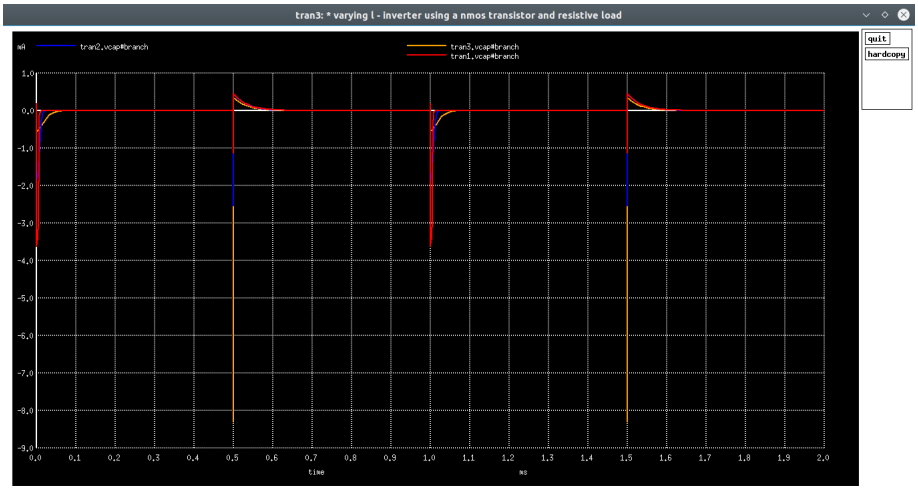

Figure 12: Capacitor Current Varying L

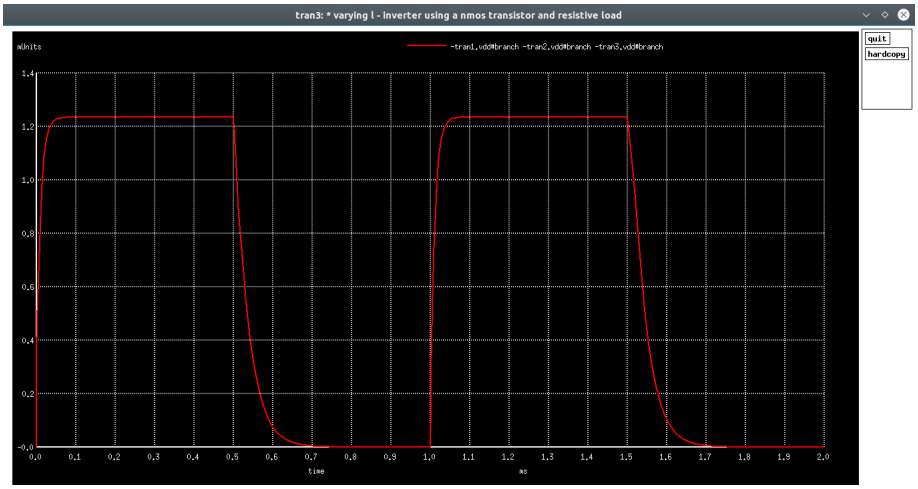

Figure 13: I_{DS} on Varying L

1.5.4 Variation of C_L

On varying C_L, no variation in DC parameters(NM_H, NM_L) is observed, as they are independent of the load capacitance. Whereas for transient parameters, we observe that as C_L increases, the rise time and fall time increase, as a larger value of capacitance takes more time to charge and discharge. Table 4 contains the changes in both DC and Transient parameters.

C_L	0.1nF	20nF
V_{OH}	3.3V	3.3V
V_{OL}	0.2481V	0.2481V
V_{IL}	0.583V	0.583V
V_{IH}	1.57V	1.572V
NM_H	1.728V	1.728V
NM_L	0.3349V	0.3349V
t_{rise}	1.55μs	0.302ms
t_{fall}	0.193μs	39.86μs
t_{PLH}	0.501μs	99.77μs
t_{PHL}	87.72ns	18.08μs
t_d	0.294μs	58.85μs
P_{avg}	0.702mW	0.8862mW

Table 4: Effect of varying C_L on various DC and Transient Parameters

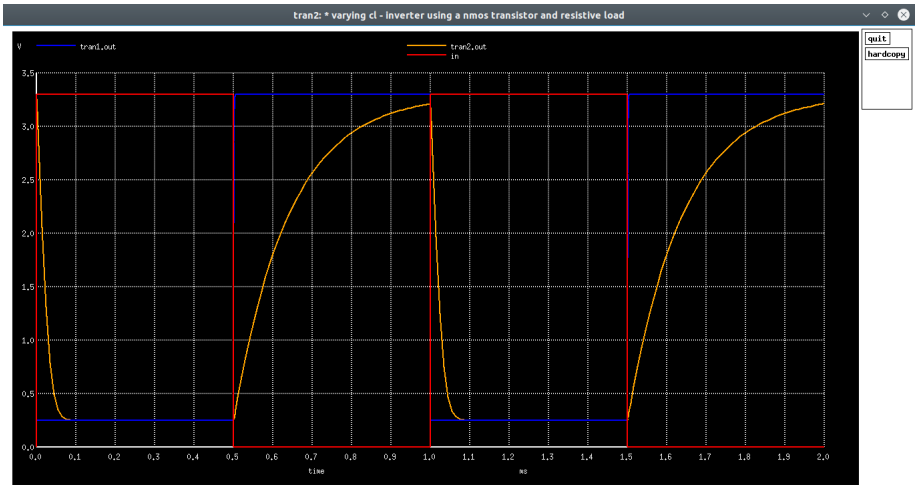

Figure 14: Transient Response Varying C_L

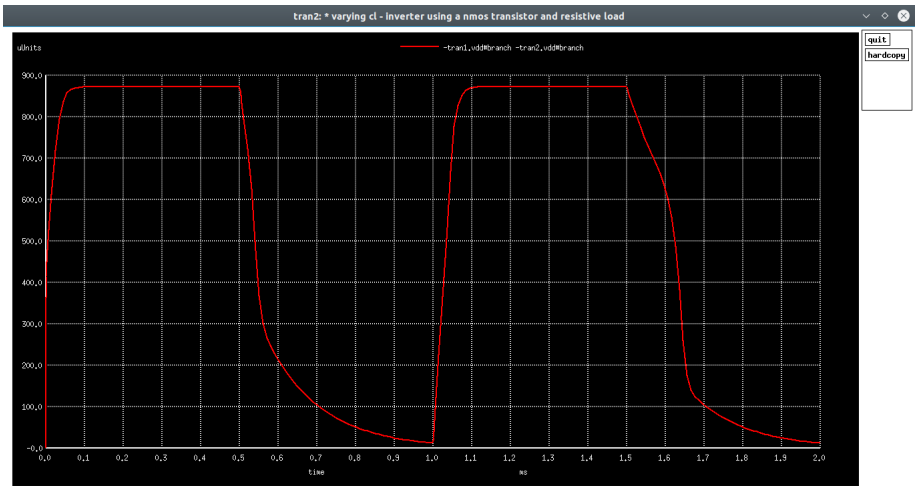

Figure 15: I_{DS} on Varying C_L

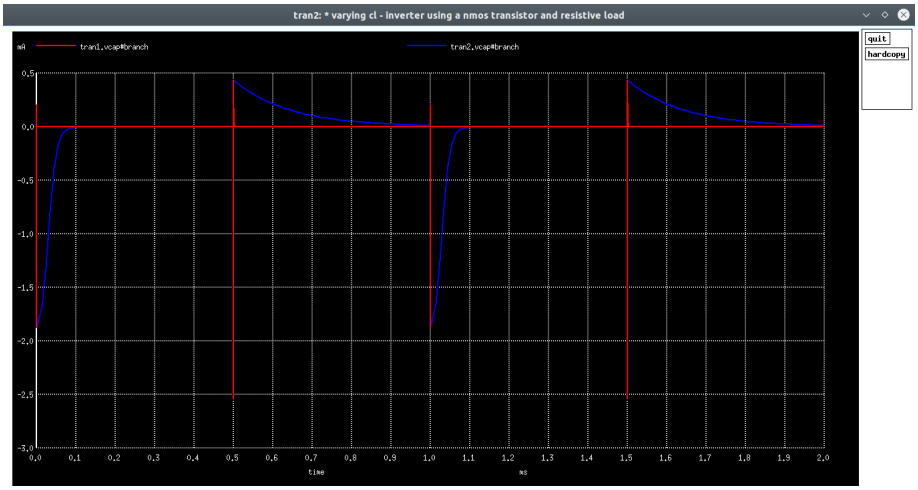

Figure 16: Capacitor current on Varying C_L

1.6 Conclusion

The experiment was performed, and all parameters were extracted and analysed. The values obtained agreed with theory, and hence simulations were verified. NGSPICE was the simulator used for this task.

2 CMOS Inverter Layout and Characterisation

2.1 Aim

To learn layout, extract, LVS and characterization processes in the design flow with CMOS inverter as example, and to compute parametrs such as input capactiance, output capacitance, rise time and fall time for various loads.

2.2 Circuit Diagram

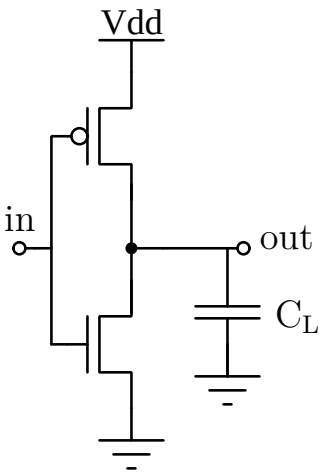

Figure 17: Circuit Diagram of CMOS Inverter

2.3 Introduction

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has a logic level 0 and vice-versa. CMOS stands for Complementary Metal Oxide Semiconductor. CMOS is one of the various families in logic gate design in Digital VLSI. A major difference in this family is, there is both a pull-up network as well as the pull-down network and only one of the path is on at any given time. The output is taken at the junction of pull-up and pull-down network. When pull-up network constructed using PMOS is ON, output capacitor is charged by the supply and when pull-down network constructed using NMOS is ON, the capacitor initially charged now discharges through this path to ground.

2.4 Layout

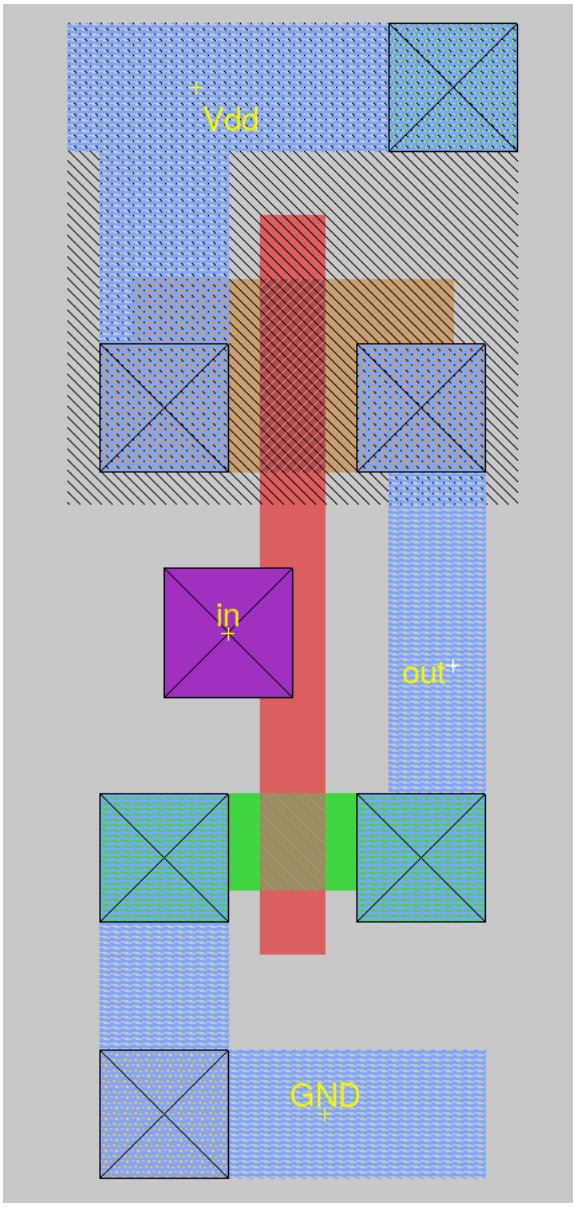

Figure 18: Layout of CMOS Inverter

From the layout in Figure(18), it is seen that the width of the pdiffusion layer is twice the ndiffusion layer. This is to compensate for the mobility of holes compared to electrons, so as to make the $t_{rise} \approx t_{fall}$.

2.5 Expected Netlist

```
m0 out in 0 0 cmosn l=0.25u w=10u
m1 out in Vdd Vdd cmosp l=0.25u w=31u
cl out 0 5n
```

2.6 Netlist extracted from Magic

```
M1000 out in Vdd Vdd cmosp w=6 l=2
+  ad=28 pd=22 as=28 ps=22
M1001 out in Gnd Gnd cmosn w=3 l=2
+  ad=19 pd=18 as=19 ps=18
C0 in Gnd 4.0fF
C1 out Gnd 2.07fF
```

2.7 Analysis and Observation

Area of the inverter cell = 504 microns

Input capacitance = 4 fF

Output capacitance = 2.07 fF

Sum of all nodal capacitance = 0.02540 pF

The DC transfer characteristics is shown in Figure(19). It is seen that the transfer characteristics does not change with different load capacitance C_L

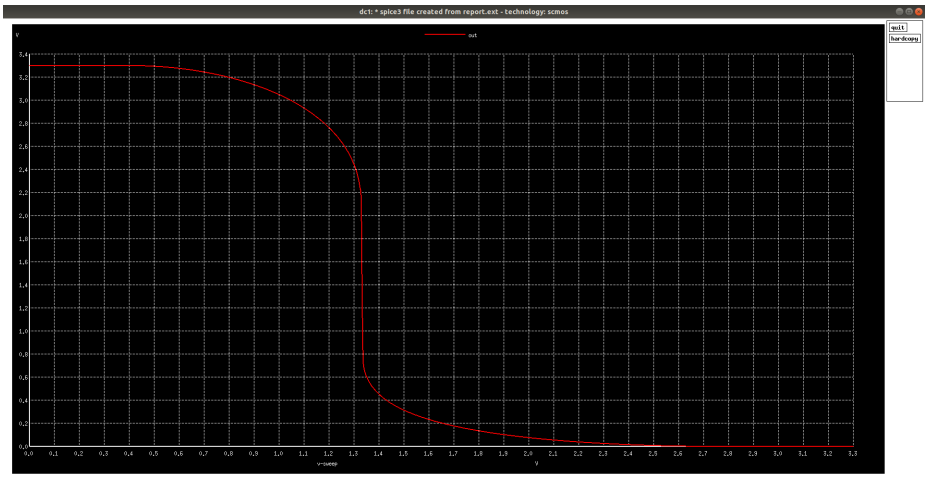

Figure 19: CMOS Inverter transfer characteristics

The transient response of the CMOS inverter can be seen in Figure(20). It can be seen that as the lthe load capacitance C_L increases, the output takes time to reach the maximum voltage. This is further supported by the values in Table(5). The rise and the tfall increases for increase in the load capacitance.

The value of the trise and the tfall can be approximated to

$$t_{rise} = 2.2 * R_{p_{eff}} * C \tag{1}$$

$$t_{fall} = 2.2 * R_{n_{eff}} * C \tag{2}$$

where $R_{p_{eff}}$ and $R_{n_{eff}}$ are the effective resistances exhibited by the PMOS and the NMOS during the pull-up and the pull-down phase respectively.

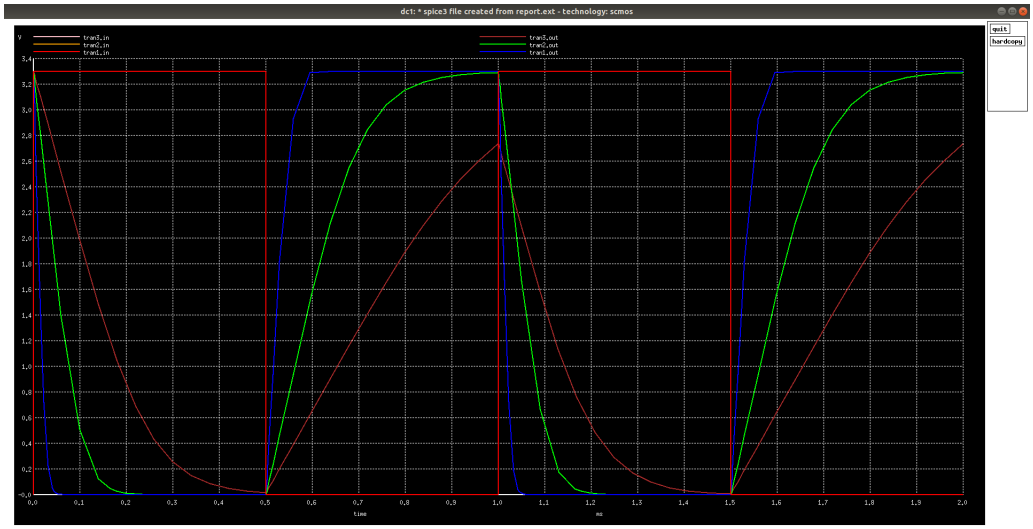

Figure 20: CMOS Inverter transient characteristics with various C_L(5nF, 20nF, 50nF)

C_L	5nF	20nF	50nF
t_{rise}	56.61μs	0.223ms	-
t_{fall}	26.64μs	0.107ms	0.25805ms
t_{PLH}	26.3μs	0.1045ms	0.2568ms
t_{PHL}	12.77μs	0.0109ms	0.1262ms
t_d	19.55μs	0.07781ms	0.191ms
P_{avg}	54.45μW	0.2173mW	0.449mW
$P_{dynamic}$	0.111mW	0.435mW	0.946mW
V_{OH}	3.3V		
V_{OL}	4.83nV		
V_{IL}	1.0034V		
V_{IH}	1.4996V		
NM_H	1.8003V		
NM_L	1.0034V		

Table 5: Effect of varying C_L on various DC and Transient Parameters

2.8 Conclusion

The experiment was performed, and a layout for CMOS inverter was designed using MAGIC software. The netlist was extracted and compared with a netlist designed for CMOS inverter, and was found to be the same. Various parameters have been found out and analysed.