VLSI DESGIN LABORATORY
LAB REPORT

CMOS INVERTER

Submitted to
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Characterization of CMOS Inverter

1 Objectives

Study the:

1. Transfer function
2. Noise Margin
3. Risetime and Fall time
4. Propagation delay
5. Power and Energy consumed

with variation in R_L and W of the Load Resistor and Pull-Down Transistor. Along with this also calculate power and energy consumed for non ideal step input for Resistive Load Inverter.

2 Introduction

Inverter is one that inverts the signal supplied at its input. If input is made high or logic level is 1, then the output has a logic level 0 and vice-versa. A resistive load inverter is characterised by an resistive load between the pull down transistor and the voltage source. The output is taken at the junction of the load resistance and the pull-down transistor. The pull-up circuit is constituted by the resistor and the pull-down resistor by the NMOS. When the input is low, the NMOS is open circuited and the output capacitance is charged to V_{DD} through R_L.

3 Netlist

```
* Voltage sources
V1 Vdd 0 5
V2 IN 0 5
```

```
* Transistor definition
M1 OUT IN Vdd Vdd CMOSP W=4u L=2u
M2 OUT IN 0 0 CMOSN W=2u L=2u
C OUT 0 10f
```

The above statements represent the SPICE netlist for the CMOS inverter where IN represents the input and OUT represents output.

4 Schematic

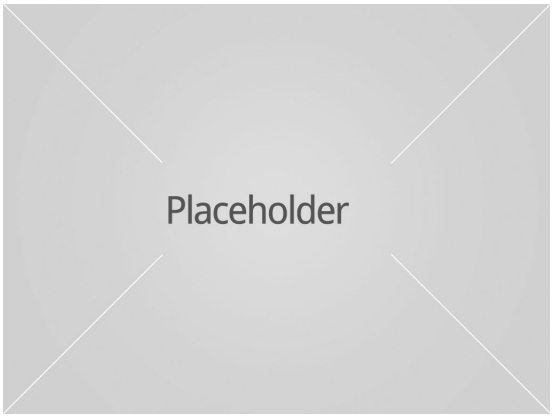

Figure 1: Schematic of CMOS Inverter

5 Analysis

Transfer functions were plotted for varying values of L and W of the driver and the load transistors and the plots obtained are as follows:

The curves moving to the right implies the switching threshold is changing and moving towards the right (increasing) and vice-versa.

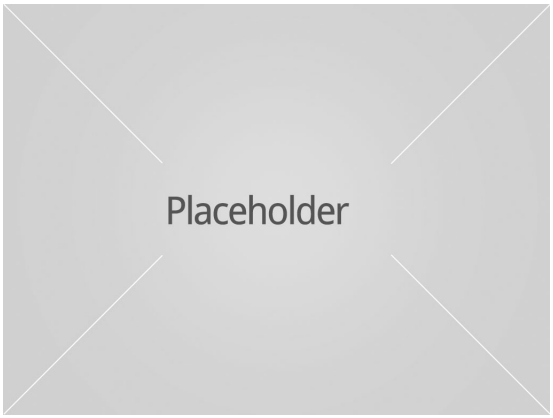

Figure 2: Transfer function when width of PMOS is varied

As width of the PMOS is increased, length remaining constant, the ratio Kd/Kl decreases and due to this the transfer function curves shift to the right in this setting. The ideal curve is assumed to cut the (2.5,2.5) point if the supply voltage is 5V. This is used as reference when we say moves towards the right or left.

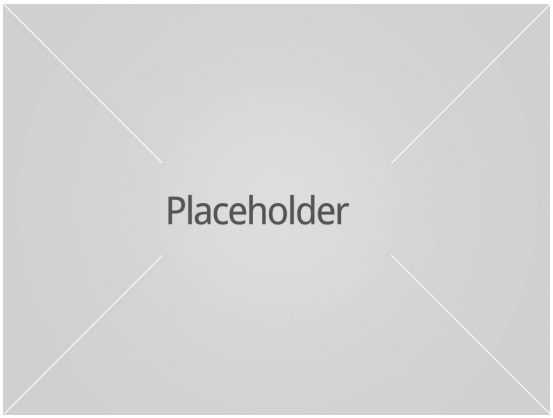

Figure 3: Transfer function when length of PMOS is varied

As the length of the PMOS is increased, width remaining constant, the ratio Kd/Kl (driver/load) increases and hence the curve shifts to the left.

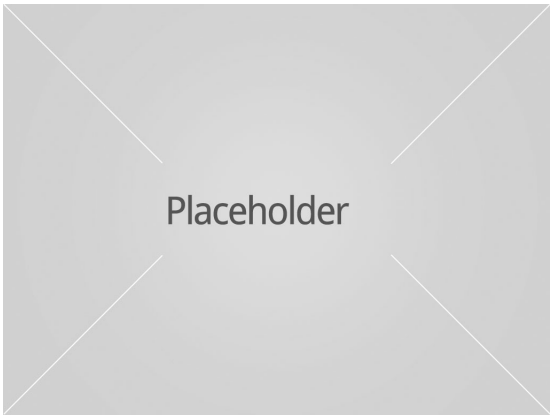

Figure 4: Transfer function when width of NMOS is varied

As width of the NMOS is increased, length remaining constant, the ratio Kd/Kl (driver/load) increases and due to this the transfer function curves shift to the left in this setting.

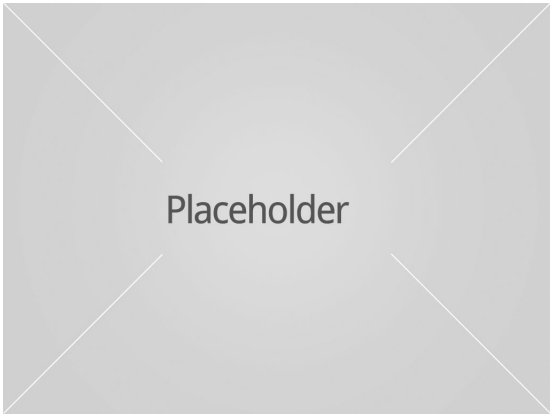

Figure 5: Transfer function when length of NMOS is varied

As the length of the NMOS is increased, width remaining constant, the ratio Kd/Kl (driver/load) decreases and hence the curve shifts to the right.

Transient characteristics for varying widths and lengths of PMOS and NMOS were plotted and the plots as as below:

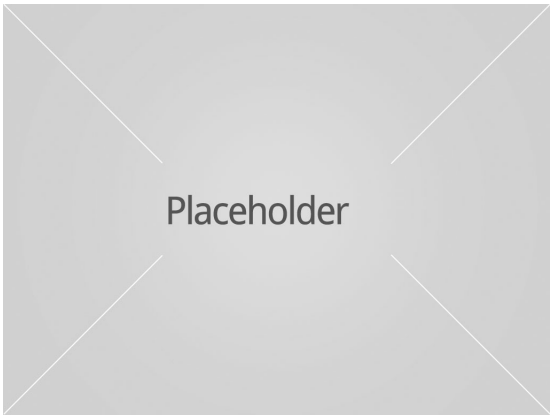

Figure 6: Transient behaviour(zoomed in) when length of PMOS is varied

When the length of PMOS is increased, the current through it reduces which in turn increases the resistance offered by it during charging resulting in a large time constant. Hence the curves are as seen in the plot.

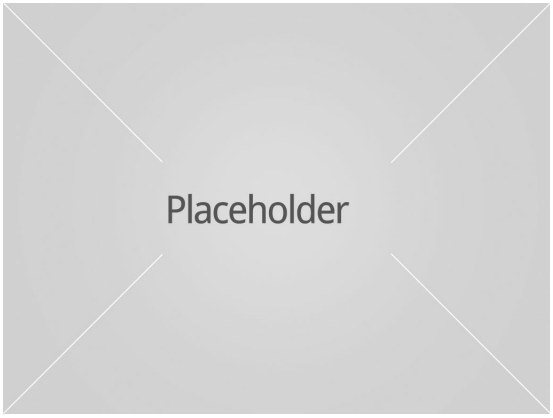

Figure 7: Transient behaviour when width of PMOS is varied

When the width of PMOS is increased, the current through it increases which in turn decreases the resistance offered by it during charging resulting in a small time constant. Hence the curves are as seen in the plot.

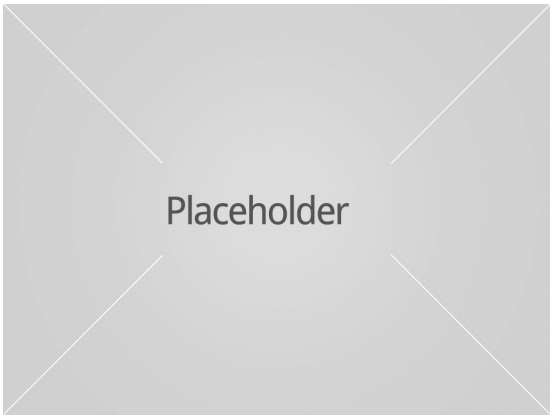

Figure 8: Transient behaviour when length of NMOS is varied

When the length of NMOS is increased, the current through it decreases which in turn increases the resistance offered by it during discharging resulting in a large time constant. Hence the curves are as seen in the plot. The last curve is the one with largest time constant, takes a longer time to discharge.

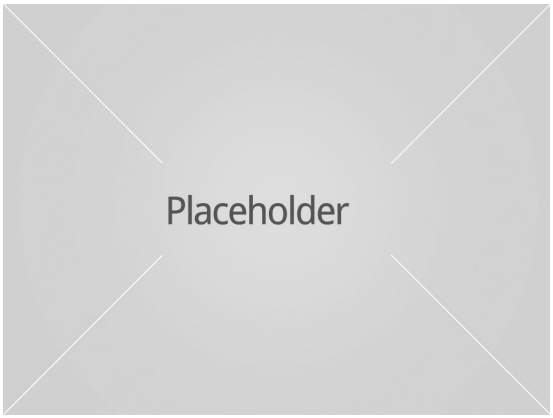

Figure 9: Transient behaviour when width of NMOS is varied

6 Observations and Results

The parameters such as Noise Margin, Rise time, Fall time, Propagation delay, Power dissipation are analyzed from the wave-forms and tabulated as follows:

All the timings parameters are in the order of 10 to the power of -11 and power dissipation in microwatt(μ W).

Voh for CMOS inverter is nearly 5V and Vol for CMOS inverter is nearly 0V as CMOS inverter achieves a perfect zero and a perfect 1.

When width of driver transistor (NMOS) is varied:

Parameter	0.25u	0.5u	2u	5u	7.5u	10u
NML	3.60	3.16	1.92	0.94	0.644	0.524
NMH	0.75	1.03	2.02	2.82	3.15	3.36
trise	3.59	3.69	3.69	3.77	3.71	4.14
tfall	19.9	10.3	3.46	2.48	2.5	2.27
tp	9.08	5.275	2.691	2.117	2.073	1.954
Power	8.25	8.935	10.845	13.425	15.63	17.05

Table 1: Effect of varying width of NMOS

When length of driver transistor (NMOS) is varied:

Parameter	0.25u	0.5u	1u	2u	3u
NML	1.922	2.38	2.75	3.11	3.3
NMH	2.014	1.68	1.28	0.91	0.75
trise	3.69	3.57	3.24	2.71	2.86
tfall	3.46	3.99	6.29	12.39	20.19
tp	2.691	3.139	3.97	5.67	7.51
Power	10.845	9.85	10.8	13.03	15.6

Table 2: Effect of varying length of NMOS

When width of load transistor (PMOS) is varied:

Parameter	0.25u	0.5u	2u	5u	7.5u	10u
NML	0.329	0.407	1.00	1.94	2.33	2.59
NMH	4.017	3.731	2.8	2.01	1.676	1.47
trise	36.64	18.7	5.97	3.53	3.28	3.16
tfall	3.26	3.3	3.33	3.44	3.44	3.63
tp	12.253	6.175	2.92	2.6	2.58	2.746
Power	6.3	6.45	8.3	10.7	12.25	13.95

Table 3: Effect of varying width of PMOS

When length of load transistor (PMOS) is varied:

Parameter	0.25u	0.5u	1u	2u	3u
NML	1.921	1.29	0.686	0.446	0.385
NMH	2.02	2.66	3.15	3.56	3.745
trise	3.69	5.71	11.5	30.98	58.1
tfall	3.46	3.10	2.75	2.64	2.70
tp	2.687	3.45	5.07	8.09	11.57
Power	10.845	10.95	14.045	15	15.65

Table 4: Effect of varying length of PMOS

The analysis was performed by for varying loads(capacitance) and non-ideal step input. Here by non ideal step input means duty cycle varied from the ideal. ON time is 25ns and OFF time is 75ns but total period remains 100ns.

Non-ideal step input:

Parameter	5f	10f	15f
trise	2.99	3.69	4.50
tfall	2.63	3.41	4.269
tp	2.184	2.691	3.066
Power	8.35	10.84	12.985

Table 5: Non ideal step input results

Ideal step input:

Parameter	5f	10f	15f
trise	2.99	3.69	4.50
tfall	2.63	3.41	4.26
tp	2.175	2.689	3.06
Power	4.035	4.07	4.06

Table 6: Ideal step input results

7 Conclusion

The experiment was performed and all parameters were extracted and analyzed. The values obtained agreed with the theory and hence simulations were verified. NGSPICE was the simulator used in this task.