COURSE PLAN AND EVALUATION PLAN

1. Course Code : EC372
2. Course title : VLSI Design Lab (0-0-3)
3. Pre-requisite : Solid-state devices.
   Circuit analysis fundamentals
   Boolean algebra and combinational logic
4. Teaching Department : Electronics & Communication Engineering.
5. Course Instructor : Ramesh Kini. M.
6. Objectives of the course : Understanding of VLSI design through laboratory experiments using modern-day computer aided design (CAD) tools.
7. Course Coverage (12 – Lab sessions)

Module	Contents	Objectives	Week
1. SPICE Analysis	Analysis of NMOS & PMOS input-output characteristics. NMOS inverter	Introduction to SPICE. To understand MOS transistor theory & MOS circuits through SPICE analysis	Week 1-3
2. CMOS layout	Implementation of CMOS logic circuits using magic. Circuit Extraction and Simulation of the extracted netlist using SPICE. Introduction to standard cell design	Introduction to magic. To develop the students ability to design the physical layout of VLSI circuits	Week 4-8
3. Term Project	CMOS subsystem design – Adders, Multipliers, Shift Registers etc	Complete design & implementation of CMOS VLSI systems	Week 9-12

8. Detailed Plan

Sl. No	Contents	Lab
1.	Spice analysis of MOSFET input, output characteristics with parametric sweeps.	Lab 1
2.	Spice analysis of NMOS inverters	Lab 2
3.	Spice analysis of CMOS gates	Lab 3
4.	Layout of CMOS gates	Lab 4
5.	Spice analysis of extracted Layout of CMOS gates	Lab 5 - 8
6.	Term Project (involves layout, LVS, switch level simulation	Lab 9 - 12

References

1. SPICE3 Version 3f3 User's Manual
2. Magic Tutorial 1-8
3. IRSIM Manual / Tutorial

7. Evaluation Plan.

Continuous Evaluation	: 20% (Performance and documentation: 5%, Quiz: 10%, Regularity: 5%)
Mid Sem	: 25%
Mini Project	: 25%
End Sem	: 30%

12. Suggested Term projects: Design, Simulation, Layout, verification and characterization of
i) 32 x 32 barrel shifter ii) 4 x 4 multiplier iv) 256 bit SRAM cell array with decoder iv) CMOS standard cell library components like 2 and 3 input NAND, NOR, AND, OR gates, and D Flip-flop.

Prepared By

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Approved By

27/12/18

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