Contents

References

[1] The Sniper Multi-Core Simulator

[2] O. Tange (2011): GNU Parallel - The Command-Line Power Tool

[3] S. C. Woo, M. Ohara, E. Torrie, J. P. Singh and A. Gupta, The SPLASH-2 Programs: Characterizaion and Methodological Considerations, Proceedings 22nd Annual International Symposium on Computer Architecture, Santa Margherita Ligure, Italy, 1995, pp. 24-36

[4] Bailey DH, Barszcz E, Barton JT, et al. The Nas Parallel Benchmarks. The International Journal of Supercomputing Applications. 1991;5(3):63-73. doi:10.1177/109434209100500306

[5] John L. Hennessy and David A. Patterson. 2017. Computer Architecture, Sixth Edition: A Quantitative Approach (6th. ed.). Morgan Kaufmann Publishers Inc., San Francisco, CA, USA.

[6] S. M. Londono and J. P. de Gyvez, "Extending Amdahl's law for energy-efficiency," 2010 International Conference on Energy Aware Computing, Cairo, Egypt, 2010, pp. 1-4, doi: 10.1109/ICEAC.2010.5702300.

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Benchmark	L3 Associativity	L3 Eviction Policy
splash2-ocean.cont	8	LRU
splash2-radix	16	SRRIP
npb-is	32	Round Robin

Table 1: Configuration parameters and values swept in the experiment.

1 Intro

This experiement sweeps different test applications (benchmarks) across different configurations of L3 cache associativity and replacement policy, in order to see effects on power and performance. We analyze the affects of L3 cache associativity and replacement policy on instructions per clock cycle (IPC), energy consumption, and miss rates. It is observed that these sweeps had little effect on energy consumption, and close to none on IPC; variations were seen between the differences in the individual benchmarks when comparing their types of operations. Finally, miss rate appears to decrease with high associativity; however, parallelism does not improve it when the workload is memory intensive.

2 Experimental Setup

Simulations ran for an x86 architecture simulator, Sniper 7.3 [1]. Each were configured with 4 cores and the same L1, L2, and L3 cache sizes (64 KB, 128 KB, and 512 KB, respectively, each using 64 byte blocks); remaining relevant configuration values were set in the `gainestown.cfg`. Input size used for all tests was preset `large`. Figure 1 visualizes the topologies for all simulations since cache sizes remained constant.

Three different L3 cache associativities, three different L3 replacement policies, and three benchmarks were swept in this experiment, for a total of 27 simulations (see Table 1). L3 is the largest and slowest cached memory unit compared to L1 and L2; it is also shared across the four cores, while each core has their own L1 and L2 caches. Therefore, we picked the lowest performing cache level used by the processing unit to sweep because it is likely to have common impact on performance and energy that is observable on all four cores. The different configurations were simulated with two `splash2` benchmarks (`ocean.cont` and `radix` [3]) and one NAS parallel benchmark (`npb`) (`is` [4]). The workloads are briefly described as follow:

splash2-ocean.cont : The `ocean` suite of test studies large-scale ocean movements based on currents, and uses 4D array grids and a red-black Gauss-Seidel multigrid equation solver.

splash2-radix : The `radix` suite uses an iterative radix sort algorithm that generates histograms and has each processor permute array index keys, a process that depends on processors communicating in order to determine keys thorough writes.

npb-is : The NASA Advanced Supercomputing (NAS) Parallel Benchmarks (NPB) are a set of benchmarks tuned for highly parallel workloads. The `is` kernal performs a sorting

operation that is important as "particle method" code (ex. simulations of mechanics (solid, fluid, etc.) as discrete "particles"), testing both integer computation speed and communication performance. This benchmark excludes floating point arithmetic.

Three varied replacement policies were chosen in order to observe the effects of different replacement models on power and performance. They are as follow:

Least Recently Used (LRU) : LRU is a recency-based policy that replaces the least recently used block, which involved tracking when blocks are accessed/re-referenced.

Static Re-Reference Interval Prediction (SRRIP) : SRRIP is a policy that uses a re-reference prediction value (RRPV) to "predict" the how likely a block will be referenced again; this policy uses 2-bit RRPV and is likely to evict recently inserted cache blocks.

Round Robin : Round robin is a queue-based policy that replaces the cache blocks in sequential order, evicting the oldest block in a set in a first-in-first-out (FIFO) manner.

Simulations had either 8-, 16-, or 32-way L3 set associativity in order to observe how power and performance changed with the number of ways. L1 and L2 caches remained 4- and 8-way set associative, respectively, and both used LRU by default. SniperSim McPAT could not output data for a 64-way set associativity for the given L3 cache size (512 KB) and block size (64 bytes) and so was excluded from the experiment.

All the simulations ran concurrently using bash script(s) and GNU `parallel` shell tool [2], and post processing of the data were handled with python (v2.7) and bash scripts (included separately). Simulations ran on a python virtual environment and in a detached `tmux` session, due to long duration of the experiments. Sniper provided data processing tools used were: `gen_topology.py`, `cpi-stack.py`, and `mcpat.py`.

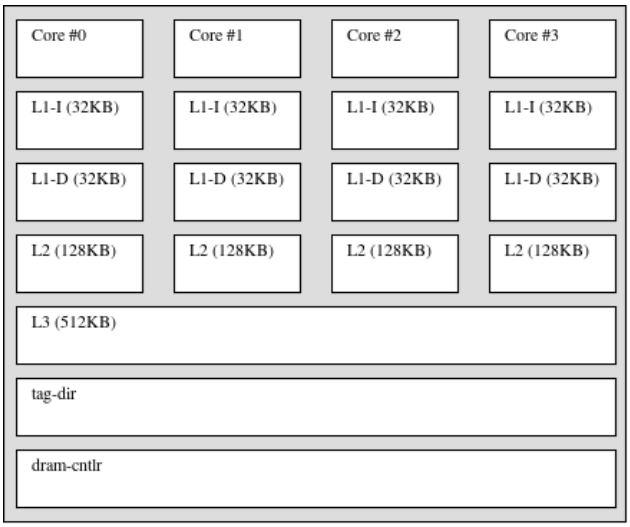


Figure 1: Topology for `npb-is`, `splash2-ocean.cont`, and `splash2-radix` benchmark tests with all consistent cache sizes: 32 KB L1, 128 KS L2, and 512 KB L3. All benchmarks were run in `Sniper-7.3` with the `gainestown` configuration using the `--viz` and `--roi` options.

3 Results & Analysis

3.1 Energy Consumption

Because only associativity and replacement policy were swept across the L3 cache, energy consumption was not expected to significantly vary across an L3 sweep within an individual benchmark. These figures are in the appendix for organization purposes, but are discussed briefly here to expand on differences observed between individual benchmarks.

Total energy usage across associativity and replacement policies different by hundredths to tenths of joules. The `npb-is` benchmark had total energy consumption ranging from 16.35 J - 16.87 J, and L3 energy consumption ranging 0.20 J - 0.27 J (Fig. 9 - 11). The `splash2-ocean.cont` benchmark had total energy consumption ranging from 61.39 J - 61.91 J, and L3 energy consumption ranging 0.86 J - 1.19 J (Fig. 23 - 25). The `splash2-radix` benchmark had total energy consumption ranging from 1.29 J - 1.31. J, and L3 energy consumption ranging 0.02 J - 0.03 J (Fig. 37 - 39).

Energy consumption within each benchmark remained consistent, however it is clear that certain workloads used more power than others. As previously observe in [7], `ocean.cont` consumed about 60x more energy than `radix`; from their CPI stacks (Fig. 30 - 32 and Fig. 44 - 46, respectively) as well as the workload descriptions in Sec. 2, `ocean.cont` had more memory accesses than `radix`, which itself was dominated by integer and floating point operations. Fewer memory accesses resulted in less power usage. This, likewise, applies to `radix` having less power than `npb-is`, as it also has more memory accessing operations than `radix` (Fig. 16 - 18). `ocean.cont` is seen to consume 4x more energy than `npb-is` despite having similar fractions of time spent on memory accessing operations. This is likely due to `npb-is` being a parallel workload and parallelism can be exploited for energy savings [6]. Memory accesses consuming more energy and parallelsim contributing to saving energy is also seen in Fig. 2, where each L3 peak dynamic power of all three benchmarks are plotted together; `ocean.cont` peaked higher than the other two.

In plotting the individual *peak* dynamic power across the workloads, we see that in most cases, as associativity increases, so do peak dynamic power of the processor (Fig. 3) and the L3 cache (Fig. 4). While this matches the general observation that higher associativity increases power consumption ([5], Ch 2), the increases are only on the order of tenths or hundreths (for processor) and thousandths (for L3) of Watts. More significant differences may be observed in tests sweeping higher associativity, block sizes, or more diverse workloads (in terms of fractions of memory accesses).

For the `npb-is` SRRIP tests, it is seen that 16-way set associativity had lower peak dynamic power for both processor and L3 (Fig. 3c and 4c) then either of the 8- and 32-way. Since this was only observed for `npb-is` for an L3 using SRRIP replacement policy, this may be unique to a re-reference interval prediction replacement policy for parallel test applications, and would better be served in sweeping more replacement policies or a wider range of L3 associativities. Alternatively, similar to how higher block sizes do not improve performance but can degrade it pass a certain point ([5], App. B), these results could also imply that power consumptions does not improve at too low or too high associativities.

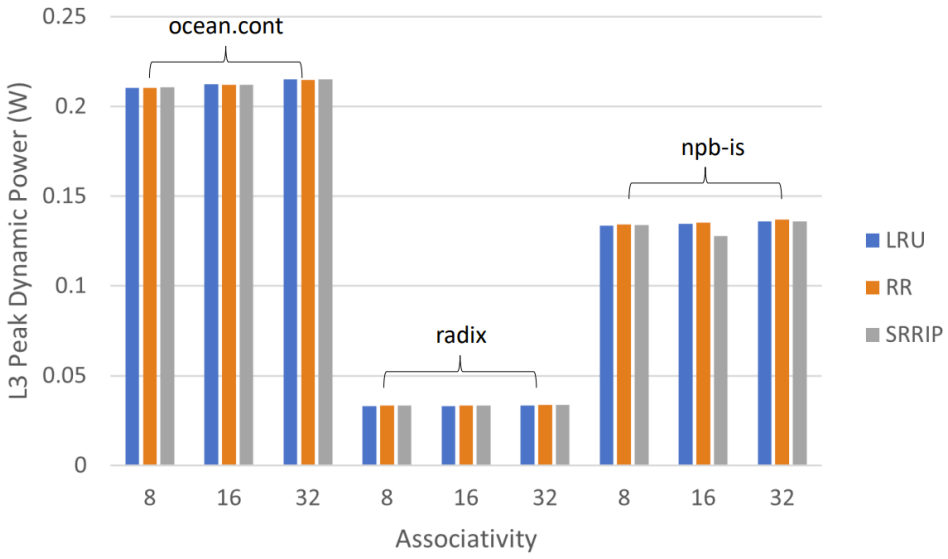
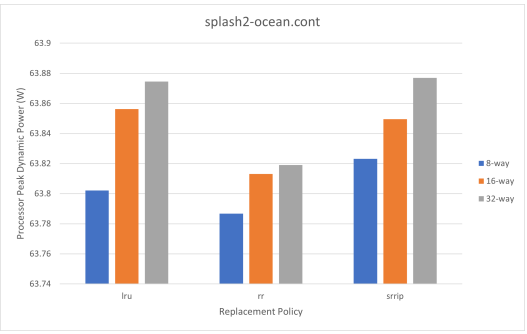
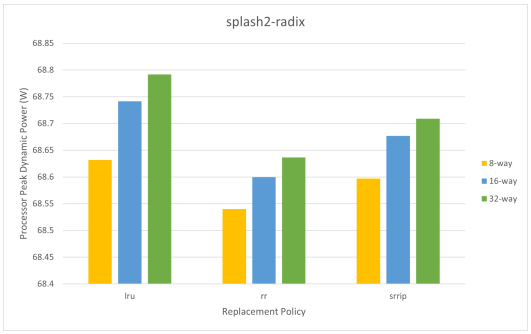


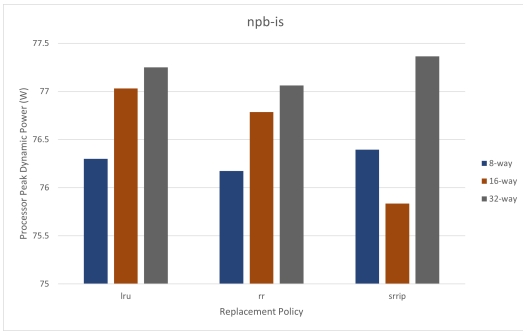
Figure 2: L3 cache associativity and replacement policy graphed against **Peak Dynamic Power of L3** for all three benchmarks.



(a)

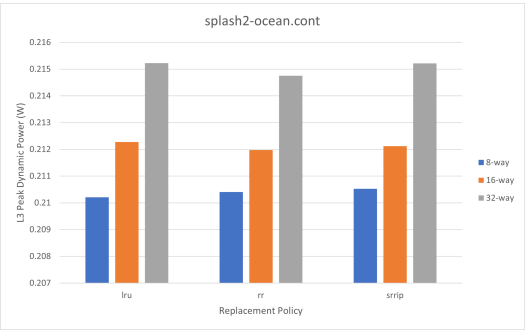


(b)

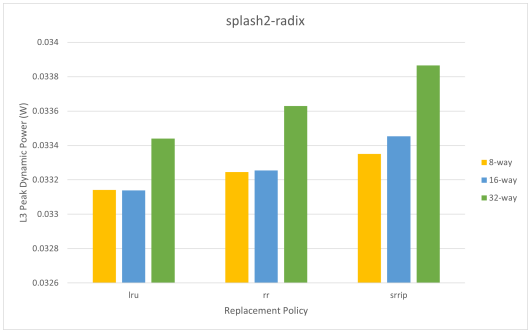


(c)

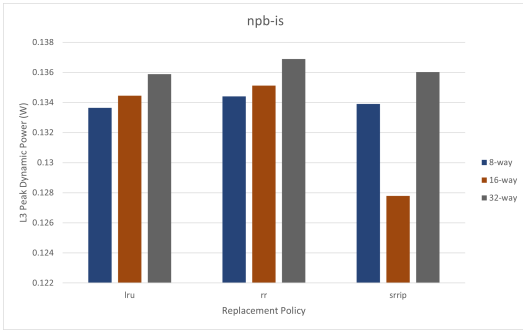
Figure 3: Peak Dynamic Power of Processor across the L3 sweep.



(a)



(b)



(c)

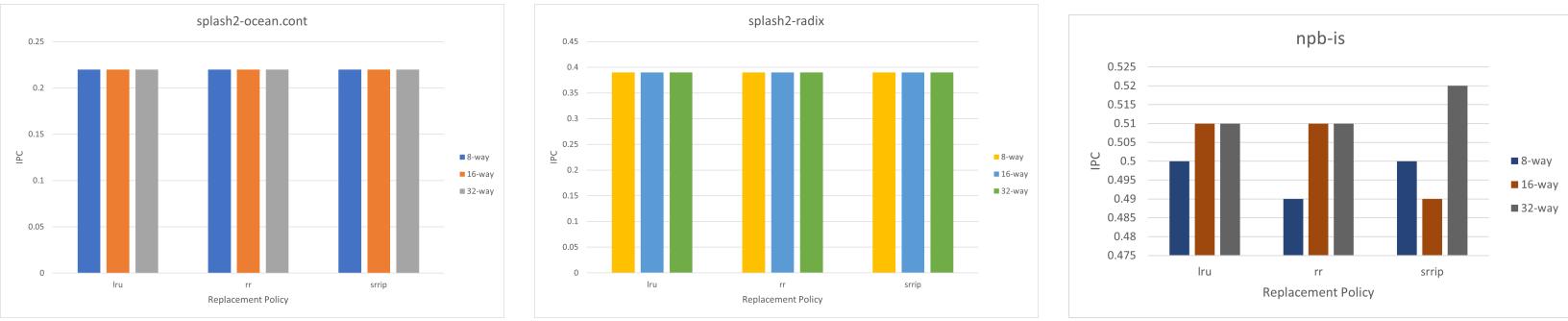
Figure 4: Peak Dynamic Power of L3 cache across the L3 sweep.

A few consistent effects on energy consumption were seen by replacement policy choice. In particular, round robin, a simple policy implementation, showed lower peak dynamic power for processor and L3 (Fig. 3, 4). This was less conistently observed for the `npb-is` benchmark (Fig. 3c, 4). These results implies that the type of workload and cache associativity affects energy consumption more than these few policy choice.

3.2 Performance Analysis: IPC

Fig. 5 shows that IPC is affected differently based on the test application swept. Replacement policy is not expected to affect IPC, however, Fig. 5a and 5b also show that associativity does not affect it, either, for the `ocean.cont` and `radix` tests. Because this is not observed for `npb-is` (Fig. 5c), this may again be due to the parallelism, because the mix of operations for `ocean.cont` and `radix` are sufficiently different (see CPI stacks in Fig. 30, 44). For the parallel workload, IPC slightly improves with increased associativity; another exception is observed for the `npb-is` workload with an SRRIP L3 cache, in which the 16-way associativity has lower IPC than either the 8- or 32-ways. This aligns with the previously observed lower energy consumption for `npb-is` 16-way, SRRIP L3 cache test in Sec. 3.1, since fewer instructions execute per clock in this particular scenario.

Interestingly, Fig. 6 shows `npb-is` had higher IPC than `radix`, which itself has higher IPC than `ocean.cont` across all sweeps. This difference is explained by the parallelism since the increased instruction count per clocks comes from more executing at the same time, compared to `ocean.cont` and `radix`, which are not tuned for parallelism.



(a) (b) (c)

Figure 5: IPC across the L3 sweep in separate benchmarks.

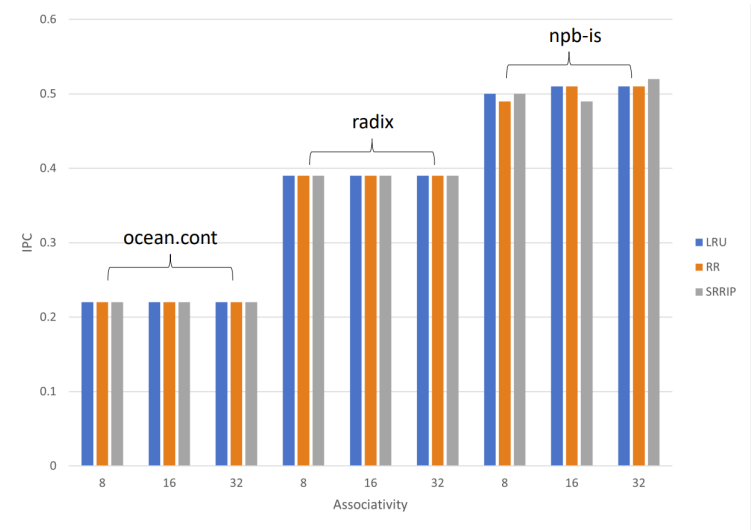
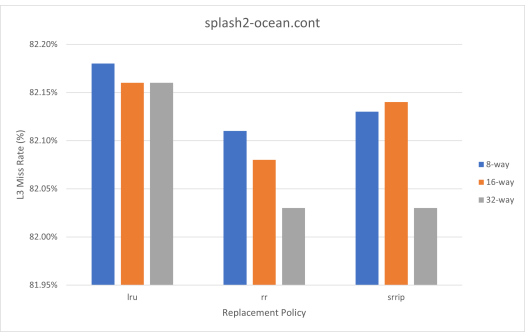


Figure 6: L3 cache associativity and replacement policy graphed against **IPC** for all three benchmarks.

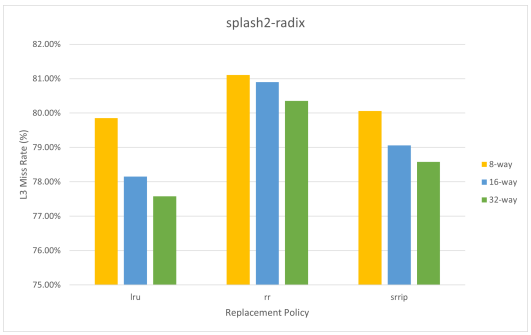
3.3 Performance Analysis: Miss Rate

Fig. 7 shows that miss rate improves with higher associativity. This is because with more blocks in each set, this lowers the chance of conflict misses when memory accesses index to the same set ([5], Ch 2). However, this is also at the cost of 1) hit time, as more blocks are being searched in parallel for an access, and 2) higher power consumption (Sec. 3.1). When compared against each other, `npb-is` shows higher miss rate than either `ocean.cont` or `radix`; `radix` had the least memory access operations, and therefore expected to have the lowest miss rate. `nbp-is` is also more memory intensive than `ocean.cont`; despite parallelism previously shown to have helped with energy saving for overall power consumption and peak dynamic power in L3, it does not help the miss rate, as seen in how significantly higher the miss rate for `npb-is` is than for `ocean.cont` (Fig. 8).

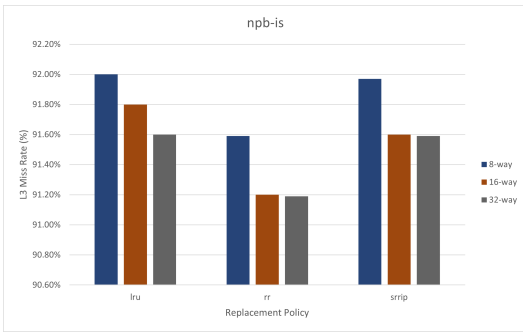
The type of workload also appears to have had miss rate affected differently by replacement policy. In particular, memory intensive `ocean.cont` and `npb-is` has lower miss rate with round robin, while `radix` has higher miss rate with round robin. This tells us that more complex replacement policies on memory intensive workloads are a detriment to performance, while simple replacement policies do not benefit the performance of applications with less memory access operations.



(a)



(b)



(c)

Figure 7: Miss rate across the L3 sweep.

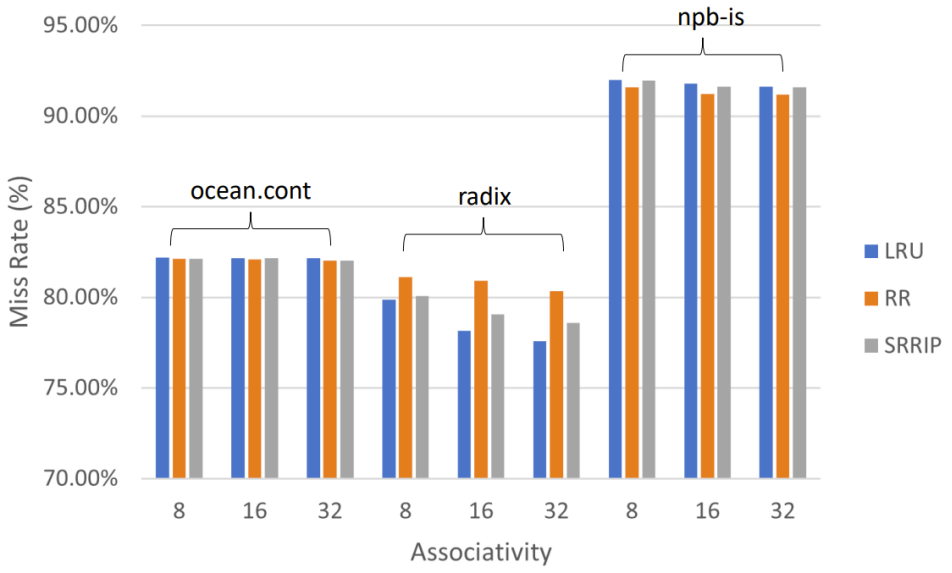


Figure 8: L3 cache associativity and replacement policy graphed against **miss rate** for all three benchmarks.

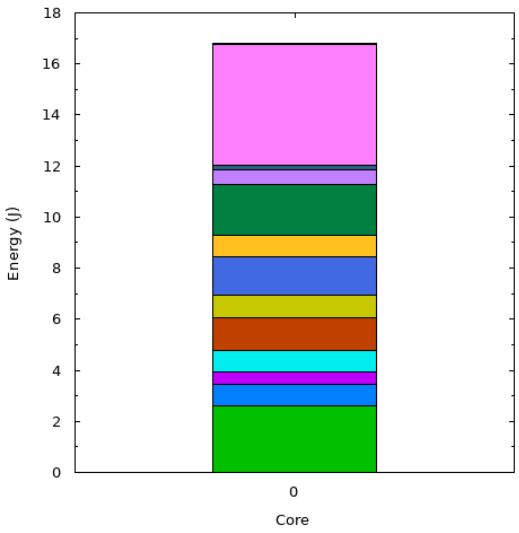
4 Conclusion

Sweeping the associativity and replacement policy of a unified last level cache show interesting effects on energy consumption and performance. While there were not huge differences in energy consumption in individual benchmarks while varying associativity and replacement policy, some of the trends of increased power were consistent with increasing associativity. More evident was that miss rate did decrease with associativity increasing. Surprisingly, IPC was not impacted by either sweeps, and those seen in the pallel application was inconsistent. And while it was clear that more memory intensive workloads (`ocean.cont` and `npb-is`) costed more in terms of energy and performance, we did observe unexpected results in the memory intense parallel benchmark, which showed that parallelism had some energy saving benefits but did not improve in miss rates for more memory intensive operations. If time permitted, this experiment could be expanded upon to included a wider range of replacement policies and associativity. I would expect to see too low and too high associativity to degrade memory performance. And we would sweep aditional parallel workloads, and those with more diverse sets of operations, given variance in the data observed for `npb-is`; it would be interesting to see if other workloads yield similar deviations or reveal new trends.

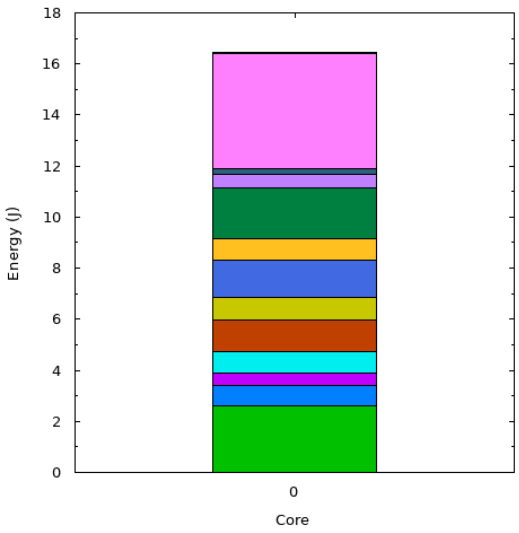
5 Appendix: Raw Post Processed Data

5.1 npb-is

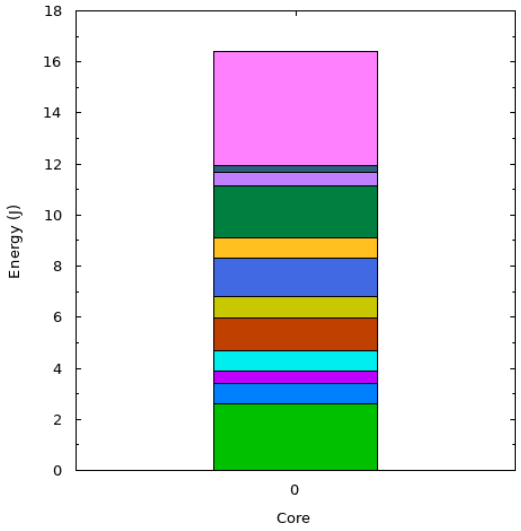
5.1.1 Power Results



(a) L3 energy 0.20 J; Total energy 16.79 J

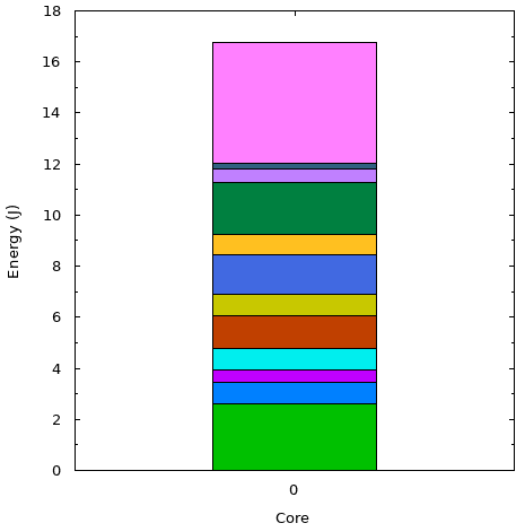


(b) L3 energy 0.21 J; Total energy 16.43 J

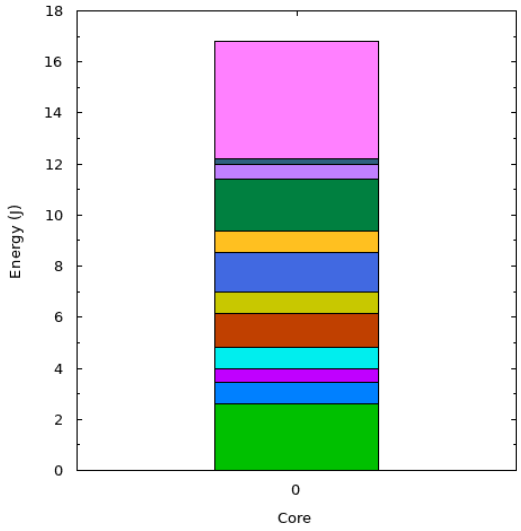


(c) L3 energy 0.27 J; Total energy 16.40 J

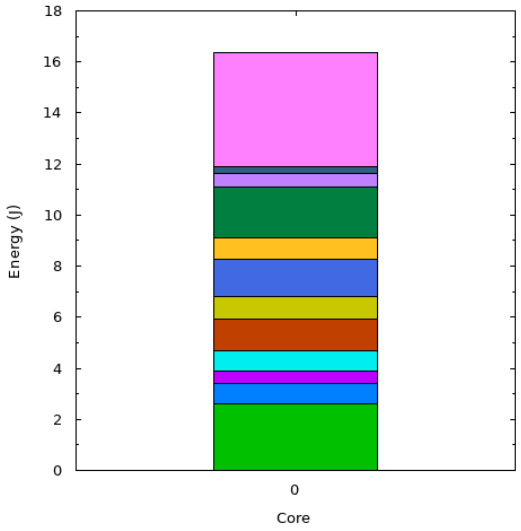
Figure 9: Processor power with an (9a) 8-way, (9b) 16-way, and (9c) 32-way L3 cache using LRU replacement policy.



(a) L3 energy 0.20 J; Total energy 16.75 J

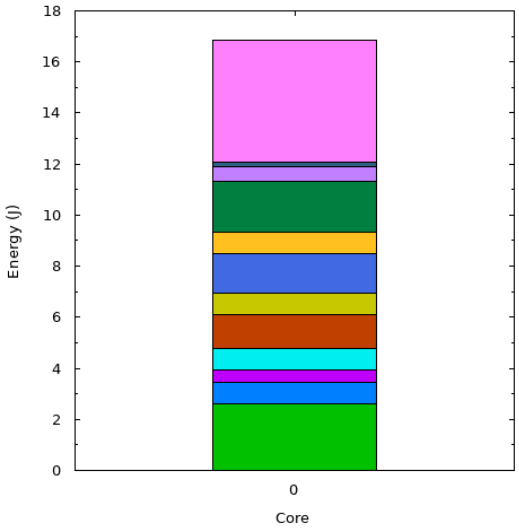


(b) L3 energy 0.22 J; Total energy 16.82 J

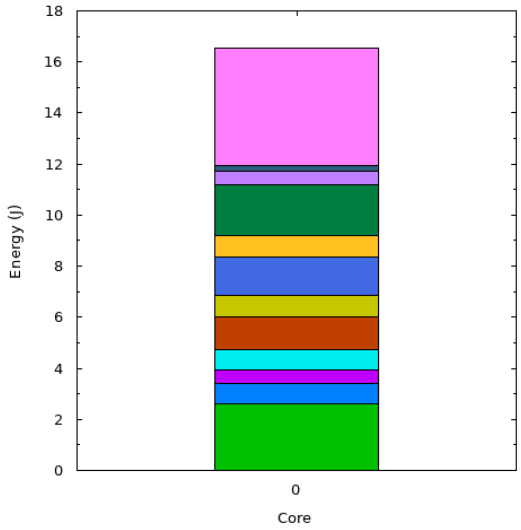


(c) L3 energy 0.27 J; Total energy 16.35 J

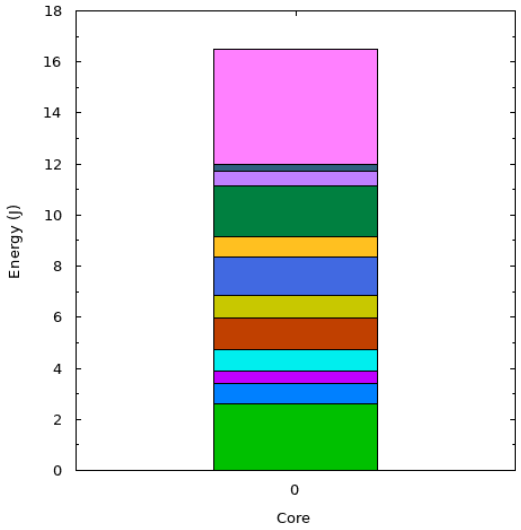
Figure 10: Processor power with an (10a) 8-way, (10b) 16-way, and (10c) 32-way L3 cache using SRRIP replacement policy.



(a) L3 energy 0.20 J; Total energy 16.87 J

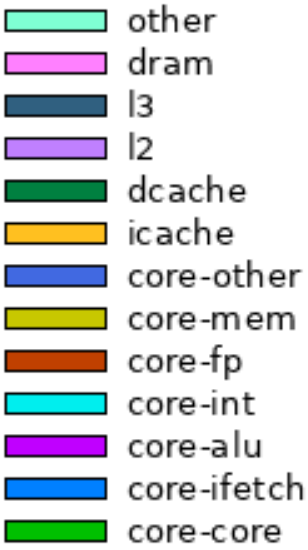


(b) L3 energy 0.21 J; Total energy 16.56 J



(c) L3 energy 0.27 J; Total energy 16.51 J

Figure 11: Processor power with an (11a) 8-way, (11b) 16-way, and (11c) 32-way L3 cache using round robin replacement policy.


other
dram
l3
l2
dcache
icache
core-other
core-mem
core-fp
core-int
core-alu
core-ifetch
core-core

	Power	Energy	Energy %
core-core	5.96 W	2.60 J	15.48%
core-ifetch	1.92 W	0.84 J	4.99%
core-alu	1.17 W	0.51 J	3.02%
core-int	1.90 W	0.83 J	4.94%
core-fp	2.97 W	1.29 J	7.71%
core-mem	1.98 W	0.86 J	5.13%
core-other	3.48 W	1.52 J	9.02%
icache	1.92 W	0.84 J	4.99%
dcache	4.62 W	2.01 J	11.99%
l2	1.26 W	0.55 J	3.28%
l3	0.46 W	0.20 J	1.19%
dram	10.86 W	4.73 J	28.19%
other	0.03 W	0.01 J	0.07%
core	19.38 W	8.45 J	50.29%
cache	8.27 W	3.60 J	21.45%
total	38.53 W	16.79 J	100.00%

(a)

	Power	Energy	Energy %
core-core	6.13 W	2.59 J	15.77%
core-ifetch	1.95 W	0.82 J	5.02%
core-alu	1.17 W	0.49 J	3.00%
core-int	1.93 W	0.82 J	4.96%
core-fp	2.97 W	1.26 J	7.65%
core-mem	2.03 W	0.86 J	5.22%
core-other	3.49 W	1.48 J	8.99%
icache	1.96 W	0.83 J	5.04%
dcache	4.72 W	2.00 J	12.16%
l2	1.26 W	0.53 J	3.25%
l3	0.49 W	0.21 J	1.27%
dram	10.72 W	4.54 J	27.61%
other	0.03 W	0.01 J	0.07%
core	19.66 W	8.32 J	50.60%
cache	8.44 W	3.57 J	21.72%
total	38.85 W	16.43 J	100.00%

(b)

	Power	Energy	Energy %
core-core	6.17 W	2.59 J	15.78%
core-ifetch	1.96 W	0.82 J	5.00%
core-alu	1.17 W	0.49 J	2.98%
core-int	1.93 W	0.81 J	4.95%
core-fp	2.97 W	1.25 J	7.59%
core-mem	2.04 W	0.86 J	5.22%
core-other	3.56 W	1.49 J	9.11%
icache	1.97 W	0.82 J	5.03%
dcache	4.76 W	1.99 J	12.16%
l2	1.26 W	0.53 J	3.23%
l3	0.64 W	0.27 J	1.63%
dram	10.66 W	4.47 J	27.25%
other	0.03 W	0.01 J	0.07%
core	19.81 W	8.31 J	50.64%
cache	8.63 W	3.62 J	22.05%
total	39.12 W	16.40 J	100.00%

(c)

Figure 13: Specific values for each components' power consumption (See. Fig. 9), for `npb-is` benchmark with (LRU) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

	Power	Energy	Energy %
core-core	5.99 W	2.60 J	15.51%
core-ifetch	1.92 W	0.84 J	4.99%
core-alu	1.17 W	0.51 J	3.02%
core-int	1.91 W	0.83 J	4.94%
core-fp	2.97 W	1.29 J	7.70%
core-mem	1.98 W	0.86 J	5.14%
core-other	3.48 W	1.51 J	9.01%
icache	1.93 W	0.84 J	5.00%
dcache	4.63 W	2.01 J	12.01%
l2	1.27 W	0.55 J	3.28%
l3	0.46 W	0.20 J	1.19%
dram	10.87 W	4.72 J	28.16%
other	0.03 W	0.01 J	0.07%
core	19.41 W	8.43 J	50.30%
cache	8.29 W	3.60 J	21.47%
total	38.59 W	16.75 J	100.00%

(a)

	Power	Energy	Energy %
core-core	5.86 W	2.60 J	15.48%
core-ifetch	1.90 W	0.85 J	5.03%
core-alu	1.17 W	0.52 J	3.08%
core-int	1.89 W	0.84 J	4.99%
core-fp	2.97 W	1.32 J	7.85%
core-mem	1.94 W	0.86 J	5.14%
core-other	3.49 W	1.55 J	9.23%
icache	1.90 W	0.85 J	5.03%
dcache	4.55 W	2.02 J	12.02%
l2	1.26 W	0.56 J	3.33%
l3	0.49 W	0.22 J	1.30%
dram	10.40 W	4.62 J	27.47%
other	0.03 W	0.01 J	0.07%
core	19.23 W	8.54 J	50.78%
cache	8.21 W	3.65 J	21.67%
total	37.87 W	16.82 J	100.00%

(b)

	Power	Energy	Energy %
core-core	6.20 W	2.59 J	15.82%
core-ifetch	1.96 W	0.82 J	5.01%
core-alu	1.17 W	0.49 J	2.97%
core-int	1.94 W	0.81 J	4.95%
core-fp	2.97 W	1.24 J	7.58%
core-mem	2.05 W	0.86 J	5.23%
core-other	3.56 W	1.49 J	9.09%
icache	1.97 W	0.82 J	5.03%
dcache	4.77 W	1.99 J	12.18%
l2	1.26 W	0.53 J	3.23%
l3	0.64 W	0.27 J	1.63%
dram	10.66 W	4.45 J	27.20%
other	0.03 W	0.01 J	0.07%
core	19.85 W	8.28 J	50.66%
cache	8.65 W	3.61 J	22.07%
total	39.18 W	16.35 J	100.00%

(c)

Figure 14: Specific values for each components' power consumption (See. Fig. 10), for `npb-is` benchmark with (SRRIP) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

	Power	Energy	Energy %
core-core	5.94 W	2.60 J	15.42%
core-ifetch	1.92 W	0.84 J	4.98%
core-alu	1.17 W	0.51 J	3.03%
core-int	1.90 W	0.83 J	4.93%
core-fp	2.97 W	1.30 J	7.72%
core-mem	1.97 W	0.86 J	5.11%
core-other	3.48 W	1.52 J	9.03%
icache	1.92 W	0.84 J	4.98%
dcache	4.60 W	2.02 J	11.96%
l2	1.27 W	0.55 J	3.29%
l3	0.46 W	0.20 J	1.19%
dram	10.89 W	4.77 J	28.29%
other	0.03 W	0.01 J	0.07%
core	19.33 W	8.47 J	50.22%
cache	8.24 W	3.61 J	21.42%
total	38.49 W	16.87 J	100.00%

(a)

	Power	Energy	Energy %
core-core	6.07 W	2.59 J	15.67%
core-ifetch	1.94 W	0.83 J	5.00%
core-alu	1.17 W	0.50 J	3.01%
core-int	1.92 W	0.82 J	4.95%
core-fp	2.97 W	1.27 J	7.67%
core-mem	2.01 W	0.86 J	5.19%
core-other	3.49 W	1.49 J	9.02%
icache	1.95 W	0.83 J	5.02%
dcache	4.69 W	2.00 J	12.10%
l2	1.26 W	0.54 J	3.26%
l3	0.49 W	0.21 J	1.27%
dram	10.76 W	4.60 J	27.77%
other	0.03 W	0.01 J	0.07%
core	19.57 W	8.36 J	50.50%
cache	8.39 W	3.59 J	21.66%
total	38.75 W	16.56 J	100.00%

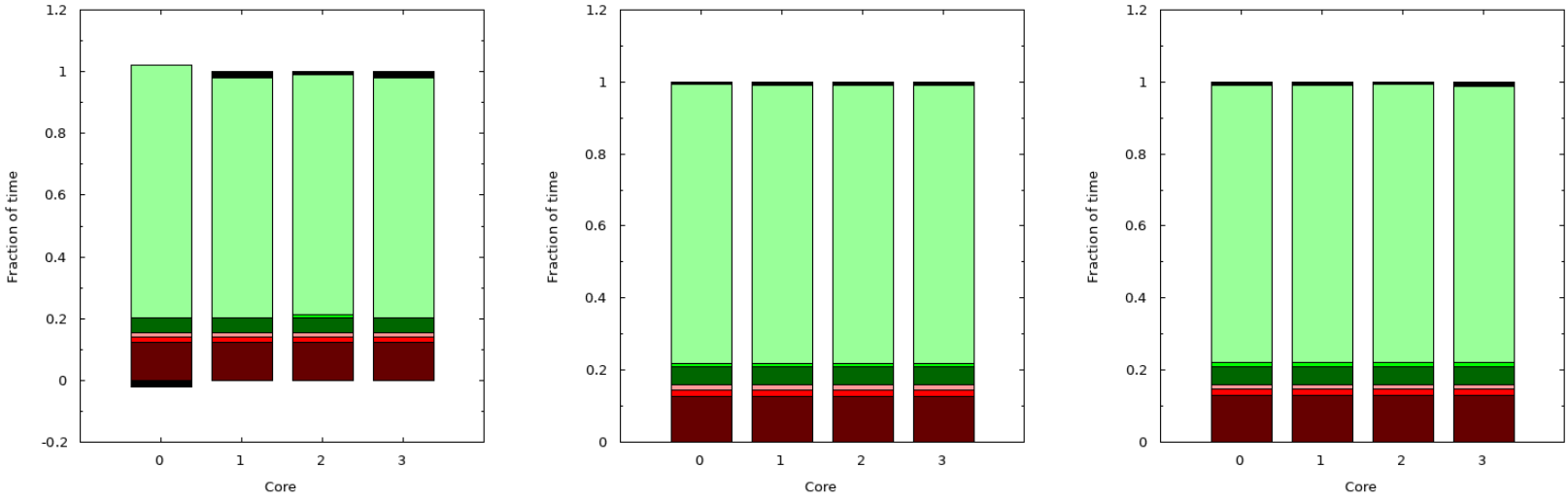
(b)

	Power	Energy	Energy %
core-core	6.13 W	2.59 J	15.69%
core-ifetch	1.95 W	0.82 J	4.99%
core-alu	1.17 W	0.49 J	2.98%
core-int	1.93 W	0.81 J	4.94%
core-fp	2.97 W	1.26 J	7.60%
core-mem	2.03 W	0.86 J	5.19%
core-other	3.56 W	1.51 J	9.12%
icache	1.96 W	0.83 J	5.01%
dcache	4.73 W	2.00 J	12.11%
l2	1.26 W	0.53 J	3.24%
l3	0.64 W	0.27 J	1.64%
dram	10.71 W	4.53 J	27.42%
other	0.03 W	0.01 J	0.07%
core	19.74 W	8.34 J	50.52%
cache	8.59 W	3.63 J	21.99%
total	39.07 W	16.51 J	100.00%

(c)

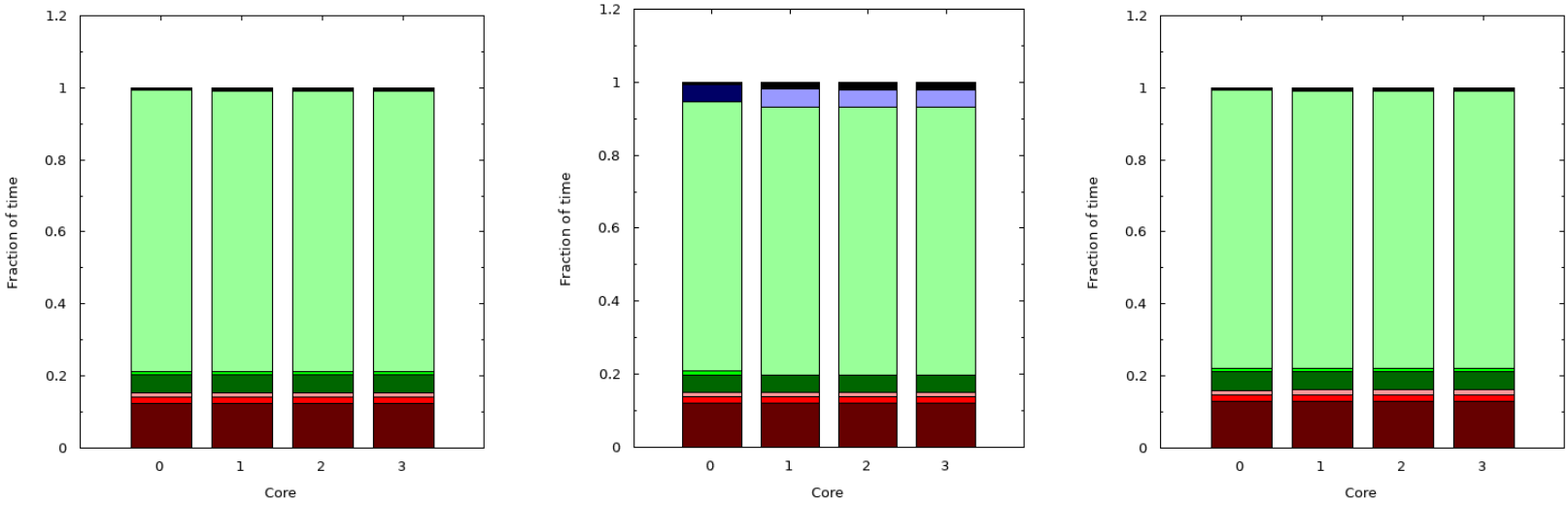
Figure 15: Specific values for each components' power consumption (See. Fig. 11), for `npb-is` benchmark with (round robin) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

5.1.2 CPI Stacks



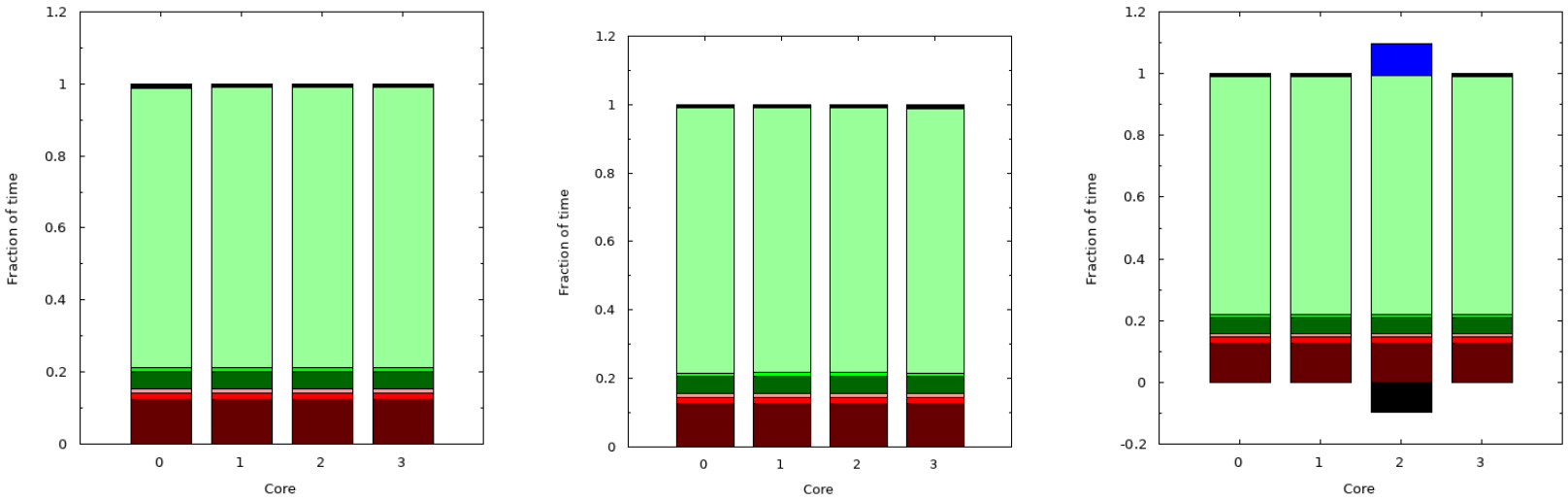
(a) (b) (c)

Figure 16: CPI stack with an (16a) 8-way, (16b) 16-way, and (16c) 32-way L3 cache using LRU replacement policy.



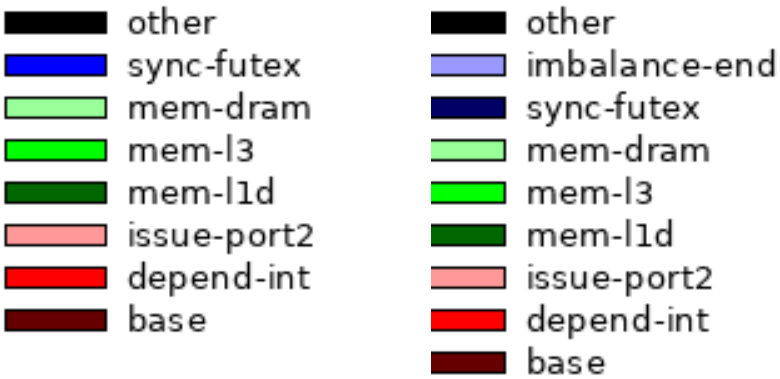
(a) (b) (c)

Figure 17: CPI stack with an (17a) 8-way, (17b) 16-way, and (17c) 32-way L3 cache using SRRIP replacement policy.



(a) (b) (c)

Figure 18: CPI stack with an (18a) 8-way, (18b) 16-way, and (18c) 32-way L3 cache using round robin replacement policy.



CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.00	0.00	0.02	0.00
mem-dram	1.65	1.57	1.57	1.57
other	-0.04	0.04	0.02	0.04
total	2.02	2.02	2.02	2.02

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.52	1.51	1.51	1.51
other	0.01	0.02	0.02	0.02
total	1.96	1.96	1.96	1.96

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.50	1.50	1.50	1.49
other	0.02	0.02	0.01	0.02
total	1.94	1.94	1.94	1.94

(c)

Figure 20: Specific values for each components' CPI stack fraction of time (See. Fig. 16), for `npb-is` benchmark with (LRU) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.57	1.56	1.56	1.56
other	0.01	0.02	0.02	0.02
total	2.01	2.01	2.01	2.01

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.00	0.00	0.00
mem-dram	1.52	1.51	1.51	1.51
sync-futex	0.10	0.00	0.00	0.00
imbalance-end	0.00	0.10	0.10	0.10
other	0.01	0.04	0.04	0.04
total	2.06	2.06	2.06	2.06

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.49	1.49	1.48	1.49
other	0.01	0.02	0.02	0.02
total	1.93	1.93	1.93	1.93

(c)

Figure 21: Specific values for each components' CPI stack fraction of time (See. Fig. 17), for `npb-is` benchmark with (SRRIP) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.58	1.58	1.58	1.58
other	0.02	0.02	0.02	0.02
total	2.03	2.03	2.03	2.03

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.53	1.53	1.53	1.53
other	0.02	0.02	0.02	0.02
total	1.98	1.98	1.98	1.98

(b)

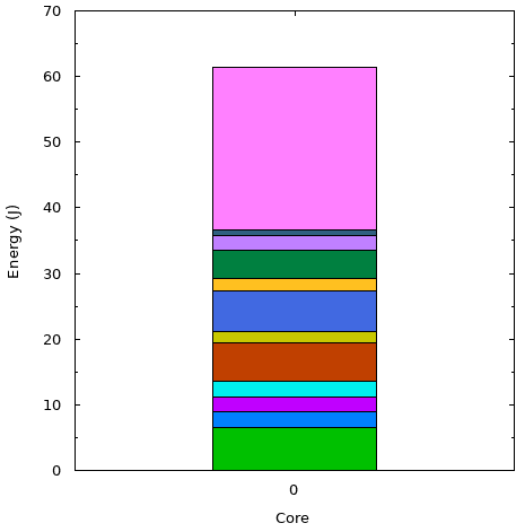
CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.04	0.04	0.04	0.04
issue-port2	0.03	0.03	0.03	0.03
mem-l1d	0.10	0.10	0.10	0.10
mem-l3	0.02	0.02	0.02	0.02
mem-dram	1.51	1.51	1.52	1.51
sync-futex	0.00	0.00	0.20	0.00
other	0.02	0.02	-0.19	0.02
total	1.96	1.96	1.96	1.96

(c)

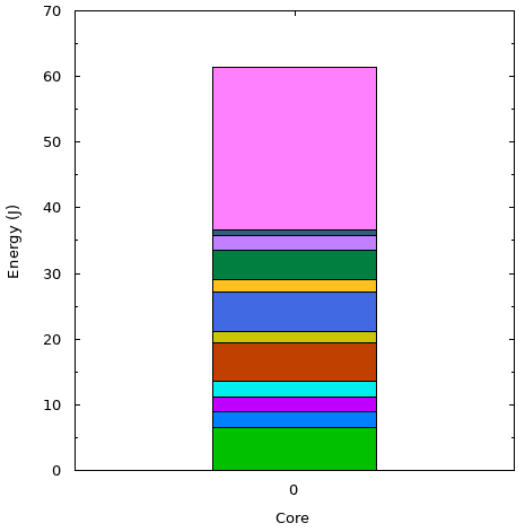
Figure 22: Specific values for each components' CPI stack fraction of time (See. Fig. 18), for `npb-is` benchmark with (round robin) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

5.2 splash2-ocean.cont

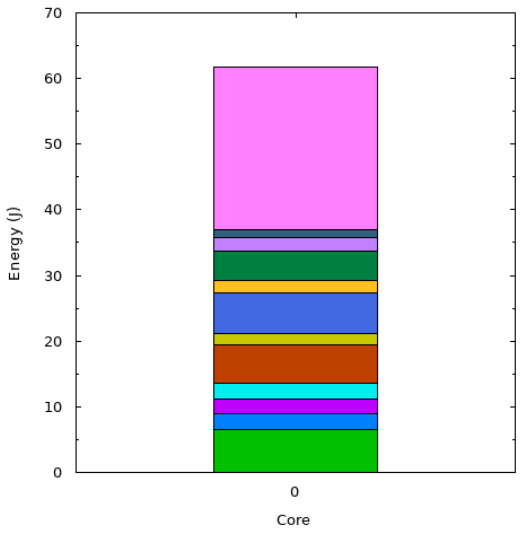
5.2.1 Power Results



(a) L3 energy 0.86 J; Total energy 61.46 J

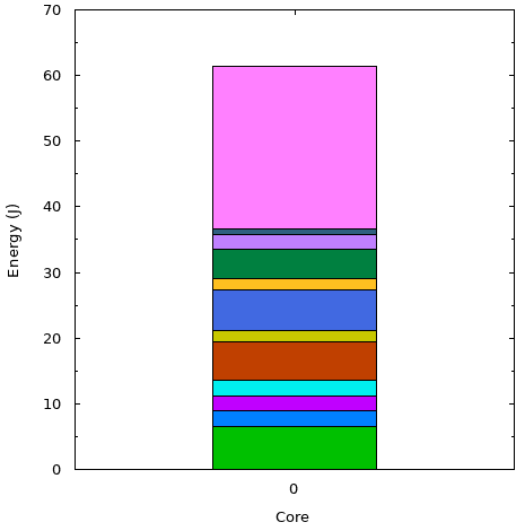


(b) L3 energy 0.92 J; Total energy 61.40 J

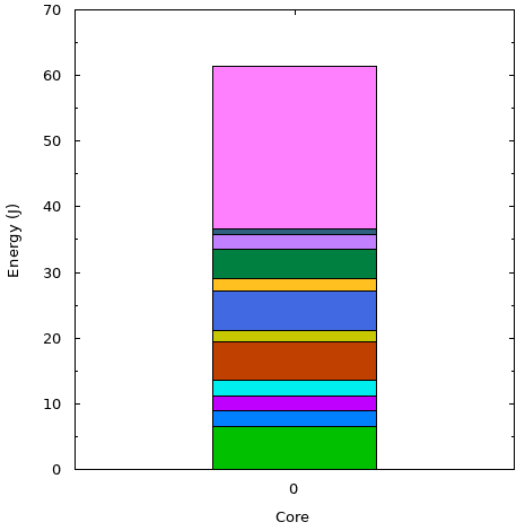


(c) L3 energy 1.18 J; Total energy 61.74 J

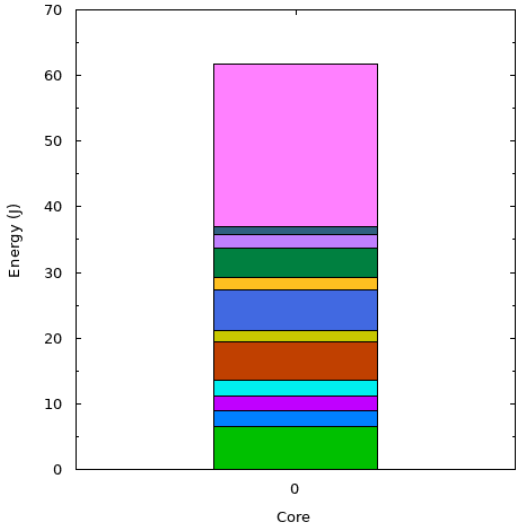
Figure 23: Processor power with an (23a) 8-way, (23b) 16-way, and (23c) 32-way L3 cache using LRU replacement policy.



(a) L3 energy 0.86 J; Total energy 61.39 J

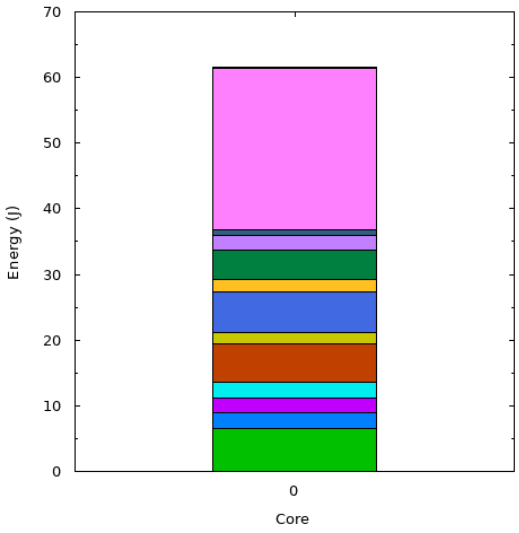


(b) L3 energy 0.92 J; Total energy 61.41 J

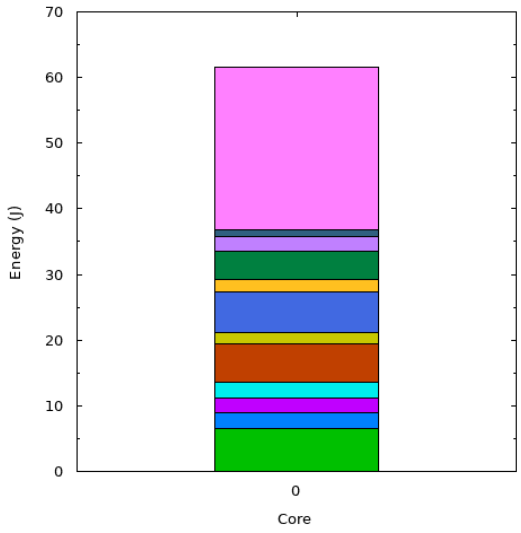


(c) L3 energy 1.18 J; Total energy 61.72

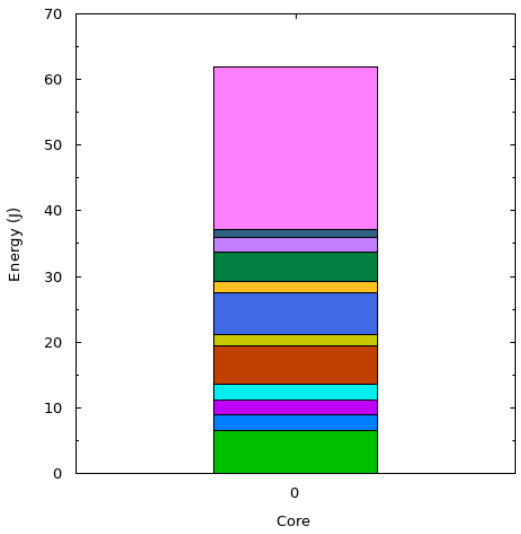
Figure 24: Processor power with an (24a) 8-way, (24b) 16-way, and (24c) 32-way L3 cache using SRRIP replacement policy.



(a) L3 energy 0.86 J; Total energy 61.52 J

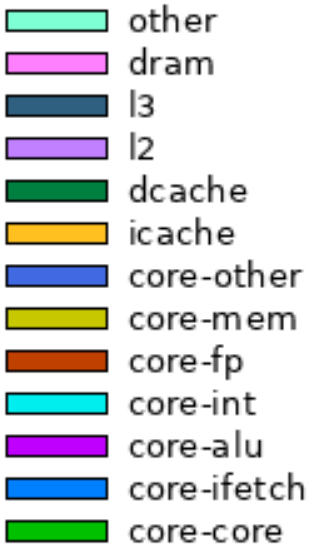


(b) L3 energy 0.93 J; Total energy 61.54 J



(c) L3 energy 1.19 J; Total energy 61.91 J

Figure 25: Processor power with an (25a) 8-way, (25b) 16-way, and (25c) 32-way L3 cache using round robin replacement policy.



	Power	Energy	Energy %
core-core	3.71 W	6.55 J	10.66%
core-ifetch	1.39 W	2.46 J	4.00%
core-alu	1.24 W	2.20 J	3.57%
core-int	1.34 W	2.37 J	3.85%
core-fp	3.35 W	5.93 J	9.64%
core-mem	0.93 W	1.65 J	2.68%
core-other	3.48 W	6.15 J	10.00%
icache	1.06 W	1.88 J	3.06%
dcache	2.50 W	4.43 J	7.20%
l2	1.26 W	2.24 J	3.64%
l3	0.49 W	0.86 J	1.40%
dram	13.97 W	24.71 J	40.20%
other	0.03 W	0.05 J	0.08%
core	15.44 W	27.30 J	44.42%
cache	5.32 W	9.40 J	15.30%
total	34.76 W	61.46 J	100.00%

(a)

	Power	Energy	Energy %
core-core	3.72 W	6.55 J	10.67%
core-ifetch	1.39 W	2.45 J	3.99%
core-alu	1.24 W	2.19 J	3.56%
core-int	1.34 W	2.36 J	3.84%
core-fp	3.35 W	5.90 J	9.61%
core-mem	0.94 W	1.65 J	2.68%
core-other	3.49 W	6.15 J	10.02%
icache	1.07 W	1.87 J	3.05%
dcache	2.51 W	4.42 J	7.19%
l2	1.26 W	2.23 J	3.62%
l3	0.52 W	0.92 J	1.50%
dram	14.01 W	24.67 J	40.17%
other	0.03 W	0.05 J	0.08%
core	15.48 W	27.25 J	44.37%
cache	5.36 W	9.44 J	15.37%
total	34.89 W	61.40 J	100.00%

(b)

	Power	Energy	Energy %
core-core	3.73 W	6.55 J	10.61%
core-ifetch	1.39 W	2.45 J	3.97%
core-alu	1.24 W	2.18 J	3.54%
core-int	1.34 W	2.36 J	3.82%
core-fp	3.35 W	5.90 J	9.55%
core-mem	0.94 W	1.65 J	2.67%
core-other	3.56 W	6.26 J	10.14%
icache	1.07 W	1.87 J	3.03%
dcache	2.51 W	4.41 J	7.15%
l2	1.26 W	2.22 J	3.60%
l3	0.67 W	1.18 J	1.92%
dram	14.03 W	24.65 J	39.93%
other	0.03 W	0.05 J	0.08%
core	15.56 W	27.34 J	44.29%
cache	5.51 W	9.69 J	15.70%
total	35.12 W	61.74 J	100.00%

(c)

Figure 27: Specific values for each components' power consumption (See. Fig. 23), for `splash2-ocean.cont` benchmark with (LRU) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

	Power	Energy	Energy %
core-core	3.71 W	6.55 J	10.67%
core-ifetch	1.39 W	2.46 J	4.00%
core-alu	1.24 W	2.19 J	3.57%
core-int	1.34 W	2.36 J	3.85%
core-fp	3.35 W	5.92 J	9.64%
core-mem	0.93 W	1.65 J	2.69%
core-other	3.48 W	6.14 J	9.99%
icache	1.06 W	1.88 J	3.06%
dcache	2.51 W	4.42 J	7.20%
l2	1.26 W	2.23 J	3.63%
l3	0.49 W	0.86 J	1.40%
dram	13.99 W	24.68 J	40.21%
other	0.03 W	0.05 J	0.08%
core	15.45 W	27.27 J	44.42%
cache	5.32 W	9.39 J	15.30%
total	34.78 W	61.39 J	100.00%

(a)

	Power	Energy	Energy %
core-core	3.72 W	6.55 J	10.67%
core-ifetch	1.39 W	2.45 J	3.99%
core-alu	1.24 W	2.19 J	3.56%
core-int	1.34 W	2.36 J	3.84%
core-fp	3.35 W	5.91 J	9.62%
core-mem	0.94 W	1.65 J	2.68%
core-other	3.49 W	6.15 J	10.02%
icache	1.07 W	1.88 J	3.05%
dcache	2.51 W	4.42 J	7.19%
l2	1.26 W	2.23 J	3.63%
l3	0.52 W	0.92 J	1.50%
dram	14.01 W	24.66 J	40.16%
other	0.03 W	0.05 J	0.08%
core	15.48 W	27.26 J	44.38%
cache	5.36 W	9.44 J	15.38%
total	34.87 W	61.41 J	100.00%

(b)

	Power	Energy	Energy %
core-core	3.73 W	6.55 J	10.61%
core-ifetch	1.39 W	2.45 J	3.97%
core-alu	1.24 W	2.18 J	3.54%
core-int	1.34 W	2.36 J	3.82%
core-fp	3.35 W	5.90 J	9.55%
core-mem	0.94 W	1.65 J	2.67%
core-other	3.56 W	6.26 J	10.14%
icache	1.07 W	1.87 J	3.03%
dcache	2.51 W	4.41 J	7.15%
l2	1.26 W	2.22 J	3.60%
l3	0.67 W	1.18 J	1.92%
dram	14.02 W	24.64 J	39.93%
other	0.03 W	0.05 J	0.08%
core	15.56 W	27.34 J	44.29%
cache	5.52 W	9.69 J	15.70%
total	35.12 W	61.72 J	100.00%

(c)

Figure 28: Specific values for each components' power consumption (See. Fig. 24), for `splash2-ocean.cont` benchmark with (SRRIP) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

	Power	Energy	Energy %
core-core	3.70 W	6.56 J	10.66%
core-ifetch	1.39 W	2.46 J	4.00%
core-alu	1.24 W	2.20 J	3.57%
core-int	1.34 W	2.37 J	3.85%
core-fp	3.35 W	5.93 J	9.65%
core-mem	0.93 W	1.65 J	2.68%
core-other	3.48 W	6.15 J	10.01%
icache	1.06 W	1.88 J	3.06%
dcache	2.50 W	4.43 J	7.20%
l2	1.26 W	2.24 J	3.64%
l3	0.49 W	0.86 J	1.40%
dram	13.97 W	24.73 J	40.20%
other	0.03 W	0.05 J	0.08%
core	15.43 W	27.33 J	44.42%
cache	5.32 W	9.41 J	15.30%
total	34.75 W	61.52 J	100.00%

(a)

	Power	Energy	Energy %
core-core	3.71 W	6.55 J	10.65%
core-ifetch	1.39 W	2.46 J	4.00%
core-alu	1.24 W	2.19 J	3.56%
core-int	1.34 W	2.37 J	3.84%
core-fp	3.35 W	5.92 J	9.62%
core-mem	0.93 W	1.65 J	2.68%
core-other	3.49 W	6.17 J	10.03%
icache	1.06 W	1.88 J	3.06%
dcache	2.50 W	4.42 J	7.19%
l2	1.26 W	2.23 J	3.63%
l3	0.52 W	0.93 J	1.50%
dram	13.99 W	24.71 J	40.15%
other	0.03 W	0.05 J	0.08%
core	15.46 W	27.32 J	44.39%
cache	5.36 W	9.47 J	15.38%
total	34.83 W	61.54 J	100.00%

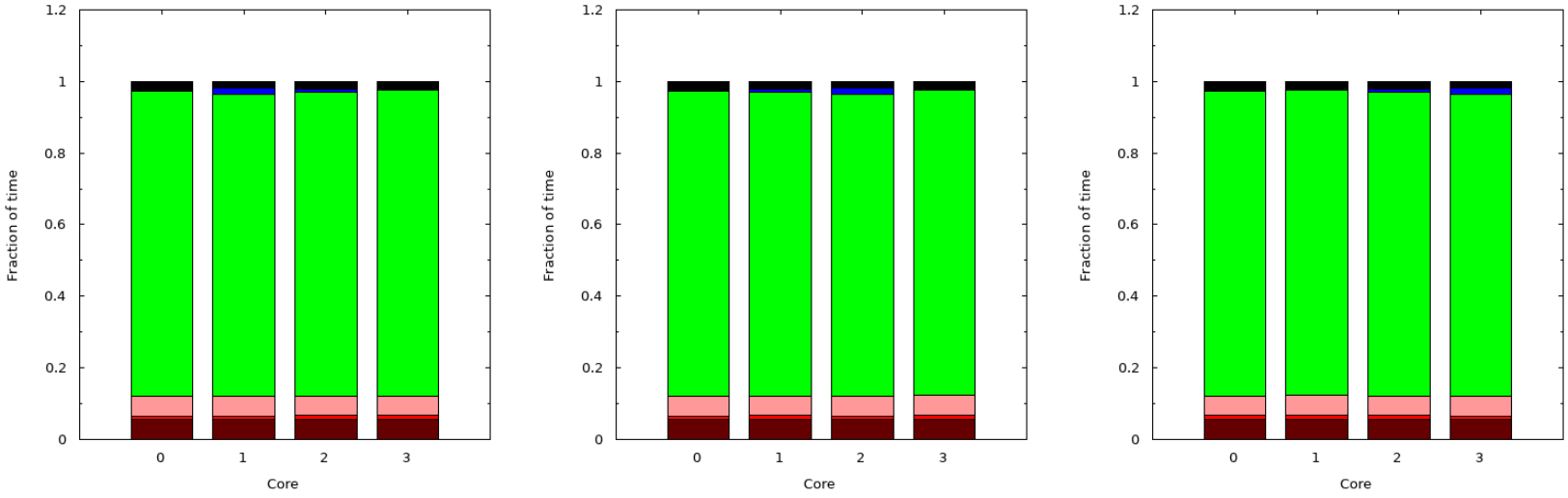
(b)

	Power	Energy	Energy %
core-core	3.71 W	6.55 J	10.58%
core-ifetch	1.39 W	2.46 J	3.97%
core-alu	1.24 W	2.19 J	3.54%
core-int	1.34 W	2.37 J	3.82%
core-fp	3.35 W	5.92 J	9.56%
core-mem	0.93 W	1.65 J	2.66%
core-other	3.56 W	6.29 J	10.16%
icache	1.06 W	1.88 J	3.04%
dcache	2.50 W	4.42 J	7.15%
l2	1.26 W	2.23 J	3.61%
l3	0.67 W	1.19 J	1.92%
dram	13.99 W	24.71 J	39.91%
other	0.03 W	0.05 J	0.08%
core	15.53 W	27.43 J	44.31%
cache	5.51 W	9.73 J	15.71%
total	35.06 W	61.91 J	100.00%

(c)

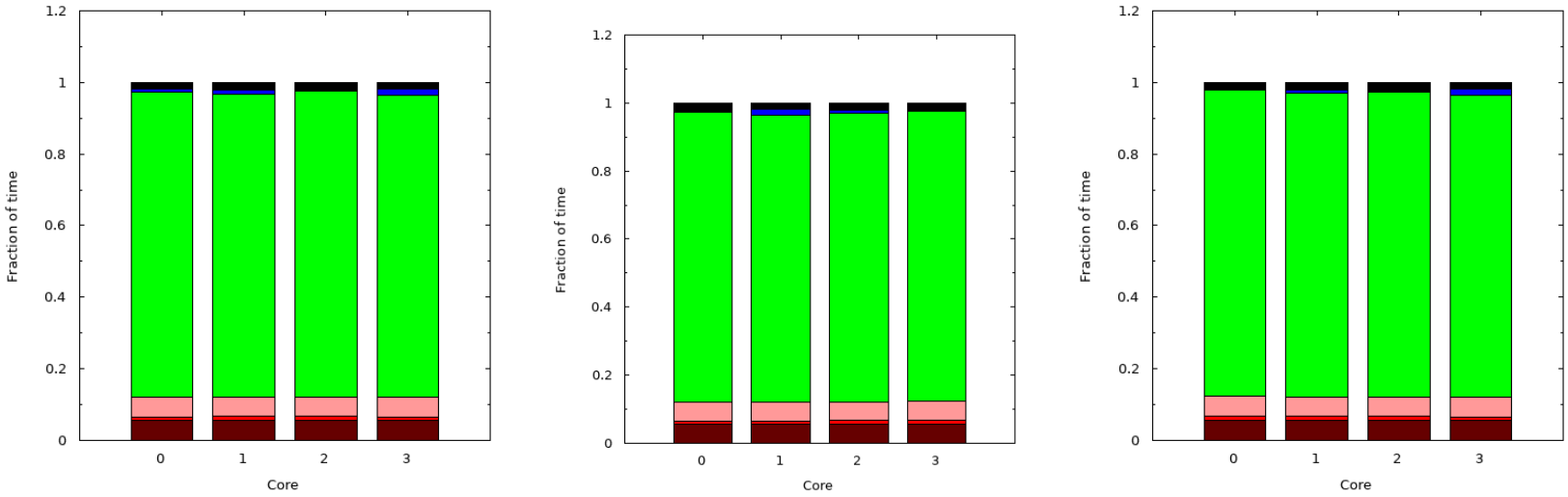
Figure 29: Specific values for each components' power consumption (See. Fig. 25), for `splash2-ocean.cont` benchmark with (round robin) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

5.2.2 CPI Stacks



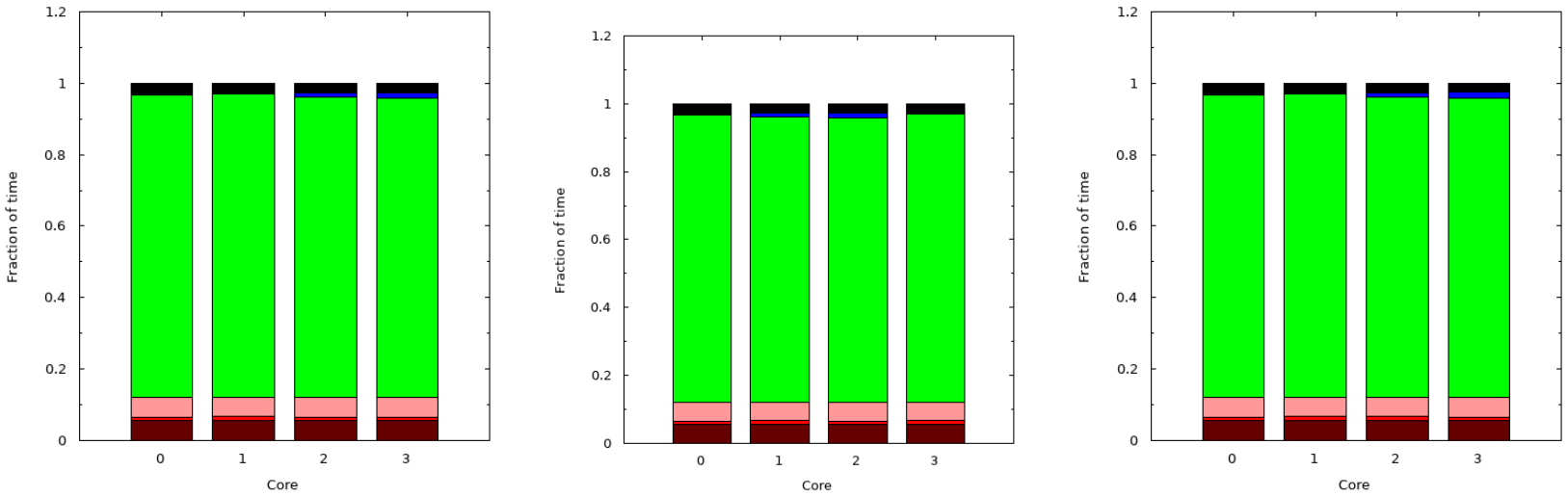
(a) (b) (c)

Figure 30: CPI stack with an (30a) 8-way, (30b) 16-way, and (30c) 32-way L3 cache using LRU replacement policy.



(a) (b) (c)

Figure 31: CPI stack with an (31a) 8-way, (31b) 16-way, and (31c) 32-way L3 cache using SRRIP replacement policy.



(a) (b) (c)

Figure 32: CPI stack with an (32a) 8-way, (32b) 16-way, and (32c) 32-way L3 cache using round robin replacement policy.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.24	0.24	0.25
mem-dram	3.87	3.83	3.82	3.84
sync-futex	0.00	0.07	0.05	0.00
other	0.12	0.09	0.09	0.11
total	4.54	4.53	4.50	4.50

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.24	0.24	0.25
mem-dram	3.85	3.80	3.81	3.83
sync-futex	0.00	0.05	0.07	0.00
other	0.12	0.09	0.08	0.10
total	4.52	4.48	4.51	4.48

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.25	0.24	0.24
mem-dram	3.84	3.82	3.79	3.81
sync-futex	0.00	0.00	0.05	0.08
other	0.12	0.10	0.09	0.08
total	4.51	4.47	4.48	4.51

(c)

Figure 34: Specific values for each components' CPI stack fraction of time (See. Fig. 30), for `splash2-ocean.cont` benchmark with (LRU) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.24	0.25	0.24
mem-dram	3.86	3.81	3.84	3.83
sync-futex	0.05	0.05	0.00	0.07
other	0.08	0.09	0.10	0.08
total	4.53	4.49	4.49	4.53

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.24	0.24	0.25
mem-dram	3.85	3.82	3.80	3.83
sync-futex	0.00	0.07	0.05	0.00
other	0.12	0.08	0.09	0.10
total	4.52	4.52	4.48	4.48

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.24	0.25	0.24
mem-dram	3.82	3.79	3.84	3.81
sync-futex	0.00	0.05	0.00	0.07
other	0.10	0.09	0.12	0.08
total	4.47	4.48	4.51	4.51

(c)

Figure 35: Specific values for each components' CPI stack fraction of time (See. Fig. 31), for `splash2-ocean.cont` benchmark with (SRRIP) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.25	0.24	0.24
mem-dram	3.84	3.82	3.79	3.81
sync-futex	0.00	0.00	0.05	0.07
other	0.16	0.14	0.13	0.12
total	4.54	4.51	4.51	4.54

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.24	0.24	0.25
mem-dram	3.83	3.78	3.80	3.81
sync-futex	0.00	0.05	0.07	0.00
other	0.15	0.13	0.12	0.14
total	4.53	4.50	4.53	4.50

(b)

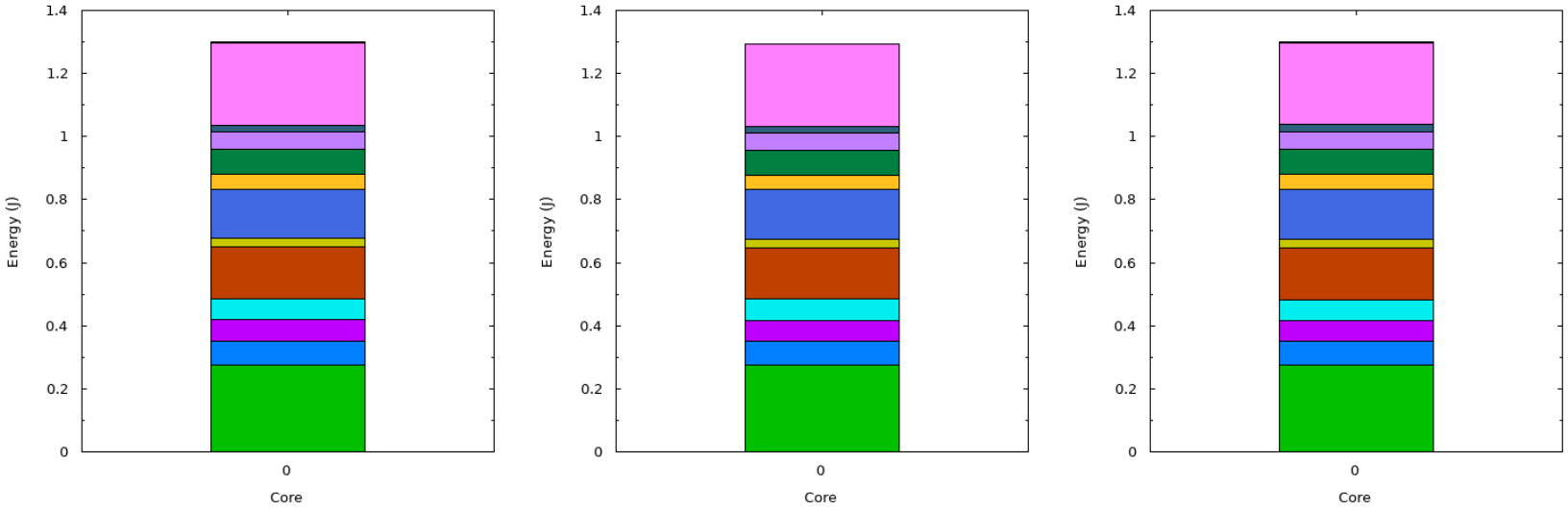
CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.05	0.05	0.05	0.05
depend-fp	0.25	0.25	0.24	0.24
mem-dram	3.83	3.81	3.79	3.80
sync-futex	0.00	0.00	0.05	0.07
other	0.16	0.14	0.12	0.11
total	4.53	4.50	4.50	4.53

(c)

Figure 36: Specific values for each components' CPI stack fraction of time (See. Fig. 32), for `splash2-ocean.cont` benchmark with (round robin) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

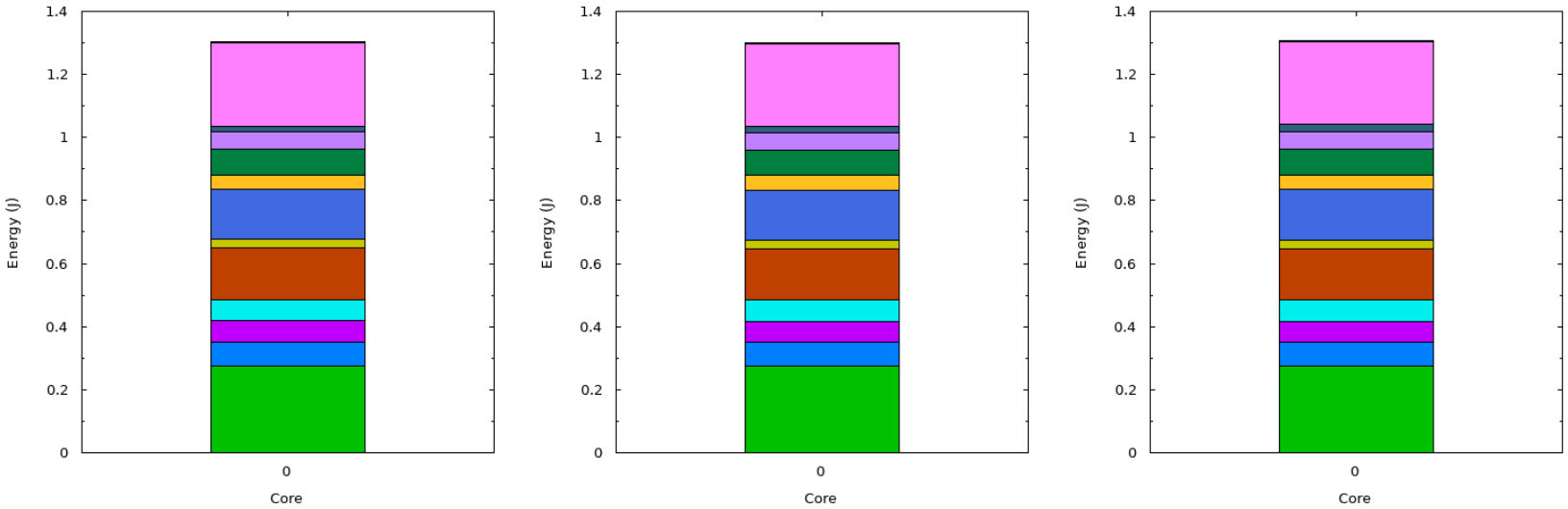
5.3 splash2-radix

5.3.1 Power Results



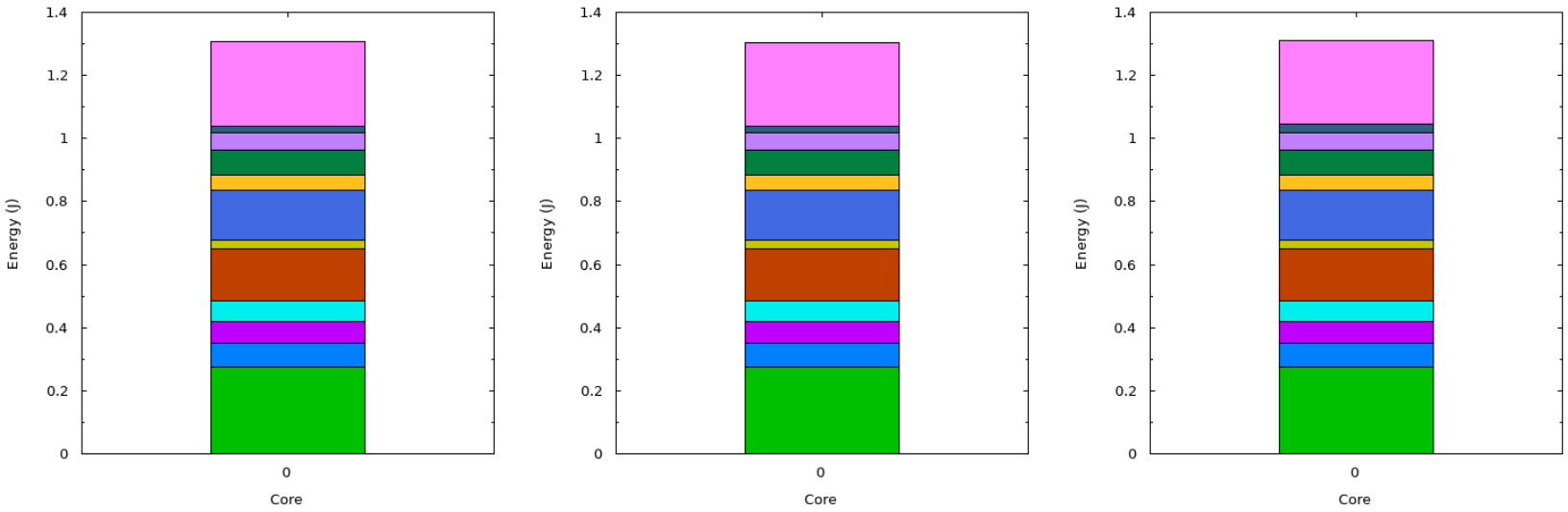
(a) L3 energy 0.02 J; Total energy 1.30 J (b) L3 energy 0.02 J; Total energy 1.29 J (c) L3 energy 0.03 J; Total energy 1.30 J

Figure 37: Processor power with an (37a) 8-way, (37b) 16-way, and (37c) 32-way L3 cache using LRU replacement policy.



(a) L3 energy 0.02 J; Total energy 1.30 J (b) L3 energy 0.02 J; Total energy 1.30 J (c) L3 energy 0.03 J; Total energy 1.31 J

Figure 38: Processor power with an (38a) 8-way, (38b) 16-way, and (38c) 32-way L3 cache using SRRIP replacement policy.



(a) L3 energy 0.02 J; Total energy 1.31 J (b) L3 energy 0.02 J; Total energy 1.30 J (c) L3 energy 0.03 J; Total energy 1.31 J

Figure 39: Processor power with an (39a) 8-way, (39b) 16-way, and (39c) 32-way L3 cache using round robin replacement policy.

	Power	Energy	Energy %
core-core	6.12 W	0.28 J	21.23%
core-ifetch	1.69 W	0.08 J	5.87%
core-alu	1.46 W	0.07 J	5.08%
core-int	1.48 W	0.07 J	5.14%
core-fp	3.64 W	0.16 J	12.63%
core-mem	0.61 W	0.03 J	2.12%
core-other	3.48 W	0.16 J	12.05%
icache	1.06 W	0.05 J	3.66%
dcache	1.77 W	0.08 J	6.14%
l2	1.22 W	0.05 J	4.23%
l3	0.43 W	0.02 J	1.47%
dram	5.85 W	0.26 J	20.29%
other	0.03 W	1.22 mJ	0.09%
core	18.49 W	0.83 J	64.11%
cache	4.47 W	0.20 J	15.50%
total	28.85 W	1.30 J	100.00%

(a)

	Power	Energy	Energy %
core-core	6.16 W	0.28 J	21.32%
core-ifetch	1.70 W	0.08 J	5.87%
core-alu	1.47 W	0.07 J	5.07%
core-int	1.49 W	0.07 J	5.14%
core-fp	3.65 W	0.16 J	12.62%
core-mem	0.61 W	0.03 J	2.13%
core-other	3.49 W	0.16 J	12.09%
icache	1.06 W	0.05 J	3.66%
dcache	1.78 W	0.08 J	6.15%
l2	1.22 W	0.05 J	4.22%
l3	0.46 W	0.02 J	1.60%
dram	5.79 W	0.26 J	20.05%
other	0.03 W	1.22 mJ	0.09%
core	18.56 W	0.83 J	64.24%
cache	4.51 W	0.20 J	15.62%
total	28.90 W	1.29 J	100.00%

(b)

	Power	Energy	Energy %
core-core	6.18 W	0.28 J	21.22%
core-ifetch	1.70 W	0.08 J	5.84%
core-alu	1.47 W	0.07 J	5.04%
core-int	1.49 W	0.07 J	5.11%
core-fp	3.65 W	0.16 J	12.54%
core-mem	0.62 W	0.03 J	2.11%
core-other	3.56 W	0.16 J	12.24%
icache	1.06 W	0.05 J	3.63%
dcache	1.78 W	0.08 J	6.11%
l2	1.22 W	0.05 J	4.19%
l3	0.61 W	0.03 J	2.08%
dram	5.77 W	0.26 J	19.81%
other	0.03 W	1.22 mJ	0.09%
core	18.66 W	0.83 J	64.08%
cache	4.66 W	0.21 J	16.01%
total	29.11 W	1.30 J	100.00%

(c)

Figure 41: Specific values for each components' power consumption (See. Fig. 37), for `splash2-radix` benchmark with (LRU) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

	Power	Energy	Energy %
core-core	6.11 W	0.28 J	21.18%
core-ifetch	1.69 W	0.08 J	5.86%
core-alu	1.46 W	0.07 J	5.07%
core-int	1.48 W	0.07 J	5.14%
core-fp	3.64 W	0.16 J	12.62%
core-mem	0.61 W	0.03 J	2.12%
core-other	3.48 W	0.16 J	12.05%
icache	1.06 W	0.05 J	3.66%
dcache	1.77 W	0.08 J	6.14%
l2	1.22 W	0.06 J	4.23%
l3	0.43 W	0.02 J	1.47%
dram	5.88 W	0.27 J	20.37%
other	0.03 W	1.22 mJ	0.09%
core	18.48 W	0.83 J	64.04%
cache	4.47 W	0.20 J	15.50%
total	28.85 W	1.30 J	100.00%

(a)

	Power	Energy	Energy %
core-core	6.14 W	0.28 J	21.23%
core-ifetch	1.69 W	0.08 J	5.86%
core-alu	1.46 W	0.07 J	5.07%
core-int	1.48 W	0.07 J	5.13%
core-fp	3.64 W	0.16 J	12.61%
core-mem	0.61 W	0.03 J	2.12%
core-other	3.49 W	0.16 J	12.09%
icache	1.06 W	0.05 J	3.65%
dcache	1.77 W	0.08 J	6.13%
l2	1.22 W	0.05 J	4.22%
l3	0.46 W	0.02 J	1.60%
dram	5.84 W	0.26 J	20.19%
other	0.03 W	1.22 mJ	0.09%
core	18.53 W	0.83 J	64.11%
cache	4.51 W	0.20 J	15.61%
total	28.91 W	1.30 J	100.00%

(b)

	Power	Energy	Energy %
core-core	6.15 W	0.28 J	21.11%
core-ifetch	1.70 W	0.08 J	5.82%
core-alu	1.47 W	0.07 J	5.03%
core-int	1.48 W	0.07 J	5.10%
core-fp	3.65 W	0.16 J	12.52%
core-mem	0.61 W	0.03 J	2.11%
core-other	3.56 W	0.16 J	12.23%
icache	1.06 W	0.05 J	3.63%
dcache	1.77 W	0.08 J	6.09%
l2	1.22 W	0.05 J	4.19%
l3	0.61 W	0.03 J	2.08%
dram	5.82 W	0.26 J	19.99%
other	0.03 W	1.23 mJ	0.09%
core	18.62 W	0.83 J	63.92%
cache	4.66 W	0.21 J	16.00%
total	29.12 W	1.31 J	100.00%

(c)

Figure 42: Specific values for each components' power consumption (See. Fig. 38), for `splash2-radix.cont` benchmark with (SRRIP) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

	Power	Energy	Energy %
core-core	6.09 W	0.28 J	21.12%
core-ifetch	1.69 W	0.08 J	5.85%
core-alu	1.46 W	0.07 J	5.07%
core-int	1.48 W	0.07 J	5.13%
core-fp	3.64 W	0.16 J	12.62%
core-mem	0.61 W	0.03 J	2.12%
core-other	3.48 W	0.16 J	12.05%
icache	1.05 W	0.05 J	3.66%
dcache	1.77 W	0.08 J	6.13%
l2	1.22 W	0.06 J	4.23%
l3	0.43 W	0.02 J	1.48%
dram	5.90 W	0.27 J	20.45%
other	0.03 W	1.23 mJ	0.09%
core	18.45 W	0.84 J	63.96%
cache	4.47 W	0.20 J	15.49%
total	28.85 W	1.31 J	100.00%

(a)

	Power	Energy	Energy %
core-core	6.11 W	0.28 J	21.15%
core-ifetch	1.69 W	0.08 J	5.85%
core-alu	1.46 W	0.07 J	5.06%
core-int	1.48 W	0.07 J	5.13%
core-fp	3.64 W	0.16 J	12.60%
core-mem	0.61 W	0.03 J	2.12%
core-other	3.49 W	0.16 J	12.09%
icache	1.06 W	0.05 J	3.65%
dcache	1.77 W	0.08 J	6.13%
l2	1.22 W	0.06 J	4.22%
l3	0.46 W	0.02 J	1.60%
dram	5.87 W	0.27 J	20.32%
other	0.03 W	1.23 mJ	0.09%
core	18.50 W	0.83 J	63.99%
cache	4.51 W	0.20 J	15.59%
total	28.90 W	1.30 J	100.00%

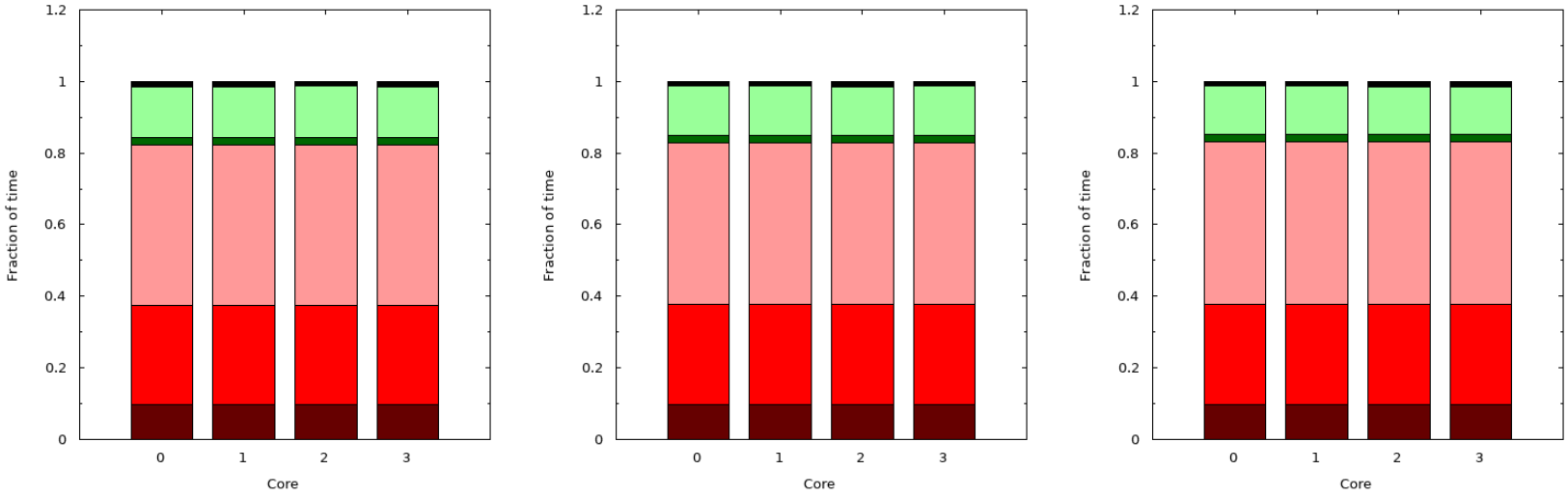
(b)

	Power	Energy	Energy %
core-core	6.12 W	0.28 J	21.03%
core-ifetch	1.69 W	0.08 J	5.81%
core-alu	1.46 W	0.07 J	5.03%
core-int	1.48 W	0.07 J	5.09%
core-fp	3.64 W	0.16 J	12.51%
core-mem	0.61 W	0.03 J	2.10%
core-other	3.56 W	0.16 J	12.23%
icache	1.06 W	0.05 J	3.63%
dcache	1.77 W	0.08 J	6.08%
l2	1.22 W	0.05 J	4.19%
l3	0.61 W	0.03 J	2.08%
dram	5.86 W	0.26 J	20.12%
other	0.03 W	1.23 mJ	0.09%
core	18.58 W	0.84 J	63.80%
cache	4.65 W	0.21 J	15.98%
total	29.13 W	1.31 J	100.00%

(c)

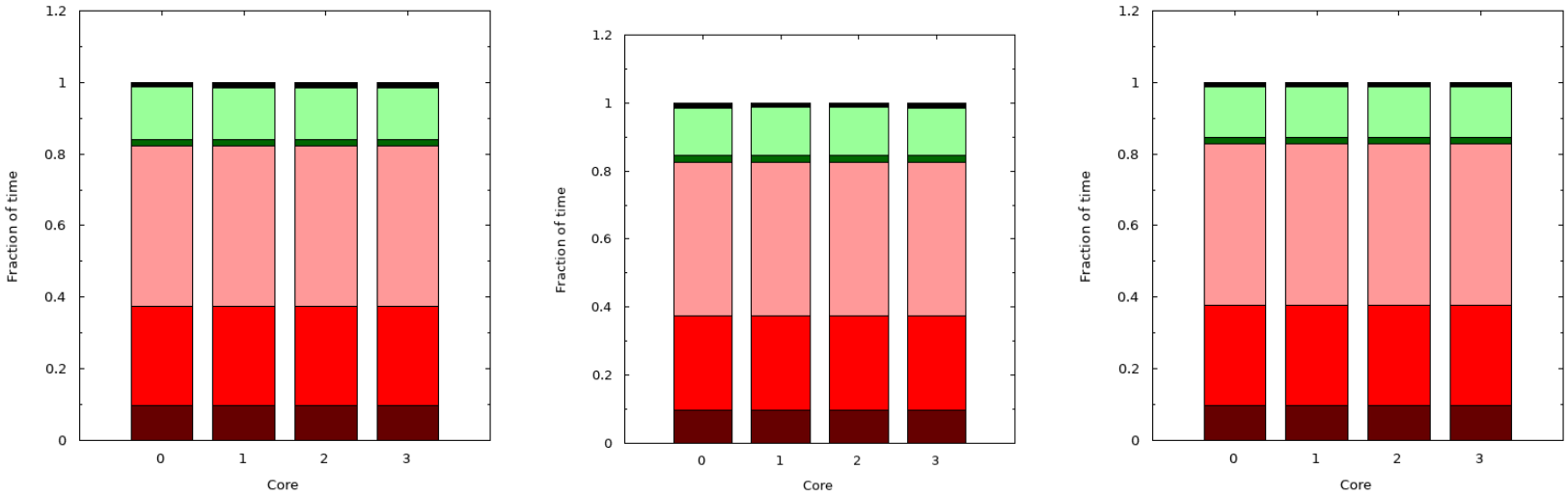
Figure 43: Specific values for each components' power consumption (See. Fig. 39), for `splash2-radix` benchmark with (round robin) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

5.3.2 CPI Stacks



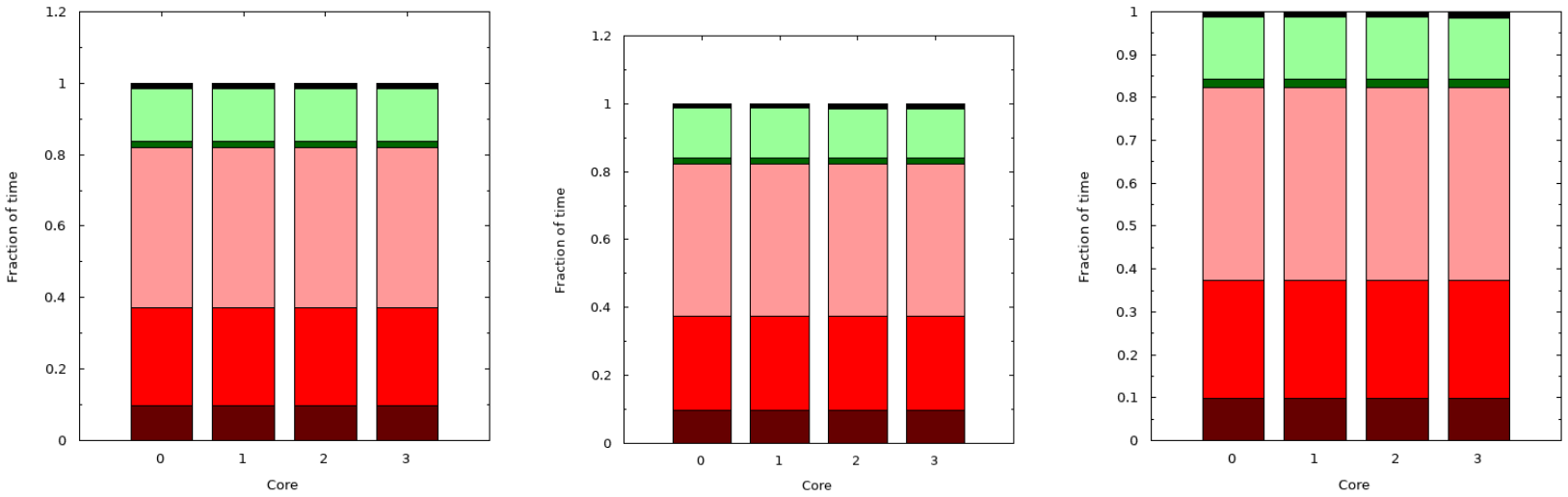
(a) (b) (c)

Figure 44: CPI stack with an (44a) 8-way, (44b) 16-way, and (44c) 32-way L3 cache using LRU replacement policy.



(a) (b) (c)

Figure 45: CPI stack with an (45a) 8-way, (45b) 16-way, and (45c) 32-way L3 cache using SRRIP replacement policy.



(a) (b) (c)

Figure 46: CPI stack with an (46a) 8-way, (46b) 16-way, and (46c) 32-way L3 cache using round robin replacement policy.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.37	0.37	0.37	0.36
other	0.04	0.04	0.04	0.04
total	2.56	2.56	2.56	2.56

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.35	0.35	0.35	0.35
other	0.03	0.03	0.04	0.03
total	2.55	2.55	2.55	2.55

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.34	0.35	0.34	0.34
other	0.03	0.03	0.04	0.04
total	2.54	2.54	2.54	2.54

(c)

Figure 48: Specific values for each components' CPI stack fraction of time (See. Fig. 44), for `splash2-radix` benchmark with (LRU) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.37	0.37	0.37	0.37
other	0.03	0.04	0.04	0.04
total	2.57	2.57	2.57	2.57

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.36	0.36	0.36	0.36
other	0.04	0.03	0.03	0.04
total	2.56	2.56	2.56	2.56

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.36	0.36	0.36	0.36
other	0.03	0.03	0.03	0.03
total	2.55	2.55	2.55	2.55

(c)

Figure 49: Specific values for each components' CPI stack fraction of time (See. Fig. 45), for `splash2-radix` benchmark with (SRRIP) L3 associativity of (a) 8, (b) 16, and (c) 32 way.

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.38	0.38	0.38	0.38
other	0.04	0.04	0.04	0.04
total	2.58	2.58	2.58	2.58

(a)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.37	0.37	0.37	0.37
other	0.04	0.03	0.04	0.04
total	2.57	2.57	2.57	2.57

(b)

CPI	Core 0	Core 1	Core 2	Core 3
base	0.25	0.25	0.25	0.25
depend-int	0.71	0.71	0.71	0.71
depend-fp	1.15	1.15	1.15	1.15
mem-l1d	0.05	0.05	0.05	0.05
mem-dram	0.37	0.37	0.37	0.37
other	0.03	0.03	0.03	0.03
total	2.56	2.56	2.56	2.56

(c)

Figure 50: Specific values for each components' CPI stack fraction of time (See. Fig. 46), for `splash2-radix` benchmark with (round robin) L3 associativity of (a) 8, (b) 16, and (c) 32 way.