EE 156
Advanced Topics in Computer Architecture

Unit1 Memory Systems

Sample Questions

1 (Virtual Memory)	/15
2 (Cache)	/15
3 (Coherence)	/15
4 (Cache)	/15
5 (Essay)	/10
6 (True / False)	/10
Total	/80

Name:

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1) Virtual Memory

a.) A virtual memory system has the following parameters.

(1) Virtual address length: 36-bit
(2) Physical Memory Size: 1GB
(3) Page Size: 4MB
(4) Additional valid, sharing and protection bits: 3
(5) 64-entry Data TLB, 16-way set-associative

Calculate the following:

Length of offset bits in virtual address (bits)	
Length of offset bits in the physical address (bits)	
Length of the Virtual Page Number (bits)	
Length of the Physical Page Number (bits)	
Total number of Virtual Pages	
Size of a page table entry (bits)	
Page Table Size (bits)	
Size of a single TLB entry – Tag only (bits)	
Size of a single TLB entry – Data only (bits)	
Total memory for the entire TLB (bits)	

b.) Describe one of the benefits of virtual memory. Which of the above fields and supporting mechanisms are used to provide this feature?

2) **Caches and Cache Access**

A test application accesses the following memory addresses (8-bit addresses), shown in hex:

0x02, 0x06, 0x0E, 0x03, 0x12, 0x06, 0x03, 0x0E

The L1 cache has the following parameters:

- Word size one byte
- Block size 2 bytes
- Cache capacity: 12 bytes
- Associativity: 3-way set associative
- Physical address size: 8-bits
- Cache Eviction Policy: LRU

Address	Tag	Index	Offset	Hit/Miss
0x02				
0x06				
0x0E				
0x03				
0x12				
0x06				
0x03				
0x0E				

a.) Calculate the size of the Tag, index and offset bits and populate in the table above.

b) Record each access as a hit or miss in the table above. Draw a diagram showing the final contents of the data and tag portion of the cache below. The cache is initially empty.

d) The pattern above has a significant number of misses. Why and what type of misses?

e) How many bits would you need for the tag, index and offset if you switched to a direct-mapped cache with the same block size and cache size (in words) as the first cache configuration.

3.) **Cache Coherence**

Assume a processor with two cores (Core A and Core B). Each core has a private L1 **byte addressable data cache** that is kept consistent using the MSI cache coherence protocol. The L1 caches each have the following parameters:

- Block size 64 Bytes
- Cache capacity: 1 K bytes
- Associativity: 4-way set associative
- Physical address size: 16-bits
- Cache Eviction Policy: LRU

a.) Calculate the size of the tag, index and offset bits.

b.) Show how the following set of memory accesses changes state bits. Assume the bus is fast enough that there is no latency in the transfer. Report if state changed for the two shared addresses xF000, xD000. The cache is initially empty.

	Commands			**State of Cache Line xF000 (I/S/M)**			**State of Cache Line xD000 (I/S/M)**	
Cycle	**Core A**	**Core B**		**Core A**	**Core B**		**Core A**	**Core B**
10	Write xF000	Read xD000		Modified	Invalid		Invalid	Shared
20	Write xD000	Read xF000						
30	Read xF000	Read xD000						
40	Write xF000	Read xD000						
50	Read xF000	Write xD000						
60	Read xD000	Write xF000						

4) **Cache Size Calculation:** Calculate the following cache features based on the Intel Sandybridge memory hiearchy:
    a. 32 kB L1 Data Cache Capacity, byte addressable
    b. 64 B blocks
    c. 8-way set associative
    d. Memory addresses of 48-bits

    Calculate the following:
    e. Bits for the **tag** of the L1 data cache?
    f. Bits for **index** of the L1 data cache?
    g. Bits for the **offset** of the L1 data cache

5) Essay Questions

b.) Define *the Memory Wall* and explain why it has threatened to hinder the progress promised by Moore's Law. Second, describe a technique computer architects have used to mostly keep the effects of the Memory Wall from reducing application performance.

b.) What are the 3 Cs of cache misses? Give one example of how a using technique to address one type of miss could actually increase the number of misses of a different type.

6) **True and False Questions** (2 points each)
(Just circle true/false no explanation required)

a) In *The Performance Equation*, each term is independent; improving one term such as CPI with a hardware software technique never impacts any of the other terms (true/false)

b) The TLB is managed by software through the operating system's scheduler (true/false)