

1 Summary

The Microarchitecture of Superscalar Processors (1995): The authors detail the benefits and techniques used in general superscalar microarchitectures of the time. Superscalars exploit instruction-level parallelism, executing instructions in parallel while also seemingly maintaining a sequential execution model, i.e. out-of-order (OOO) execution. They describe the mechanisms of each phase of the architecture (instruction fetch, decode and register dependence analysis, instruction issue or memory operation analysis and execution, and instruction reorder and commit), overview three of the recent superscalar microprocessors and their differences (MIPS R10000, Alpha 21164, and AMD K5), and discuss likely outlook and direction of future work in superscalar and increased parallelism in processors.

2 Strengths

- Section 2 sets the stage well by outlining problems encountered by previous generations of processors and reinforces why superscalar implementations are important in addresses these problems with more sophisticated architectures that increase performance.
- Section 3 comprehensively describes techniques use at each phase of the microarchitecture without complicating details of the mechanisms or implementations. This entry reads much like what one sees in a modern college textbook on the same subject.

3 Weaknesses

- Figures like those seen in section 3 (Figures 3, 5, 6) do not appear to be visually helpful in supporting what is described in their respective subsections.
- Section 4 is verbose and repetitive following the contents of Section 3.

4 Rating: 4

5 Comments

This paper is an early, comprehensive overview of the current state of superscalar processors of the time. However, it could still be improved in the ways they present their discussion. The figures mentioned previously were brief and did not seem to enrich their review, at least compared to more recent/modern diagrams of similar OOO architectures. They do not complicate the explanations, but they do not help, either. An additional figure that summarizes the entire design discussed in Section 3 would be helpful in visualizing how each phase ties together. And the bulk of the discussion on the individual microprocessor did not appear necessary. Details regarding how each microprocessor fits into each technique discussed in Section 3 can be placed in Sec. 3, whereas Section 4 could go over finer details and tradeoffs between the three microprocessors. Largely missing from the paper was quantitative data on energy and/or performance, and those could have fit well here. Otherwise, the author didn't make any bold or controversial assertions, and their conclusions about the future of superscalar and related techniques that were based on existing data and processor trends are agreeable and have manifested in the two decades since this was published.