# Contents



# References

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| **Benchmark** |
|---|
| `splash2-ocean.cont` |
| `splash2-radix` |
| `splash2-barnes` |
| `npb-is` |
| `npb-cg` |

| **Reservation Station Entries** |
|---|
| 2 |
| 4 |
| 8 |
| 16 |
| 32 |
| 48 |
| 64 |
| 98 |
| 128 |

Table 1: Configuration parameters and values swept in the experiment.

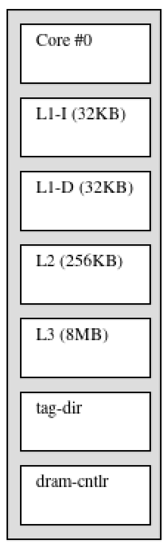



Figure 1: Topology for all five benchmark tests where only the number of reservation stations was varied (all cache sizes remained consistent through every simulation). All benchmarks were run in `Sniper-7.3` with the `gainestown` and `rob` configuration using the `--viz` and `--roi` options.

# 1 Intro

Tomasulo's algorithm is a hardware algorithm that permits in-order instruction issues and commits, but out-of-order (OOO) executions [5, 9]. This allows instructions that follow those associated with a miss to still be fetched and decoded. One technique that helps avoid data hazards is register renaming, provided by reservation stations (RS). RS' fetch and buffer the operands of an associated instruction (with their register specifiers renamed for the RS) as soon as it is read without having to read them from registers. An architecture can have a number of RS entries, improving the parallel execution of instructions that stall due to dependencies with other architectures. This experiment sweeps the number of RS entries, showing that increasing the number of RS' improves the performance and energy consumption for workloads that implement a notable amount of parallelism, but only to a point, and then the results plateau. Given the scope of the experiment and due to time constraints, no other trends are observed, but we do not exclude the possibility of performance degradation in some workloads at a higher number of RS'.

# 2 Experimental Setup

Simulations ran for an x86 architecture simulator, Sniper 7.3 [1]. Since this experiment looked to sweep instruction-level parallelism (ILP) thorugh reservation station (RS) entries, each simulation was configured with 1 core to isolate the feature of multiple instructions simultaneouly in-flight. The same default configurations were set in `gainestown.cfg` and `rob.cfg`. Those worth noting for purposes of this experiment are a window size of 128, and L1, L2 and L3 cache sizes of 64 KB, 256 KB, and 8192 KB, respectively, each using 64 byte blocks.Figure 1 visualizes the topologies for all simulations since cache sizes remained constant. Due to time constraints, commit width was set to 128 (default in `rob.cfg`). With a normal width of 4, simulations took several days and did not complete, and the large default commit width would yield results in reasonable time for the given purpose.

Nine different reservation station (RS) entries across five benchmarks were swept, for a total of 45 simulations (see Table 1). The different configurations were simulated with three `splash2` benchmarks (`barnes`, `ocean.cont` and `radix` [3]) and two NAS parallel benchmark (`npb`) (`is` and `cg` [4])[1]. These were chosen for the range of simple to complex memory access patterns and parallel implementation. Two benchmarks from `nbp` were also included to show the effects of increasing ILP for applications that would benefit from more thread-level parallelism (TLP).

[1]These are additional changes from the original experiment design due to time constraints of running `npb-ua` and sweeping number of cores.

The workloads are briefly described as follows:

**splash2-barnes** : The `barnes` application implements the Barnes-Hut method to simulate interactions of systems of N-bodies (particles, galaxies, etc.) in 3D.

**splash2-ocean.cont** : The `ocean` suite of test studies large-scale ocean movements based on currents, and uses 4D array grids and a red-black Gauss-Seidel multigrid equation solver.

**splash2-radix** : The `radix` suite uses an iterative radix sort algorithm that generates histograms and has each processor permute array index keys, a process that depends on processors communicating in order to determine keys through writes.

**npb-is** : The NASA Advanced Supercomputing (NAS) Parallel Benchmarks (NPB) are a set of benchmarks tuned for highly parallel workloads. The `is` kernal performs a sorting operation that is important as "particle method" code (ex. simulations of mechanics (solid, fluid, etc.) as discrete "particles"), testing both integer computation speed and communication performance. This benchmark excludes floating point arithmetic.

**npb-cg** : This benchmark uses a conjugate gradient method that computes the smallest eigenvalue of a large, sparse symmetric, positive definite matrix. It tests irregular, long distance communication and employs unstructured matrix vector multiplication.

All the simulations ran concurrently using bash script(s) and GNU `parallel` shell tool [2], and post processing of the data were handled with python (v2.7) and bash scripts (included separately). Simulations ran on a python virtual environment and in a detached `tmux` session, due to long duration of the experiments. Sniper provided data processing tools used were: `gen_topology.py`, `cpi-stack.py`, and `mcpat.py`.

# 3 Results & Analysis

## 3.1 Performance Analysis

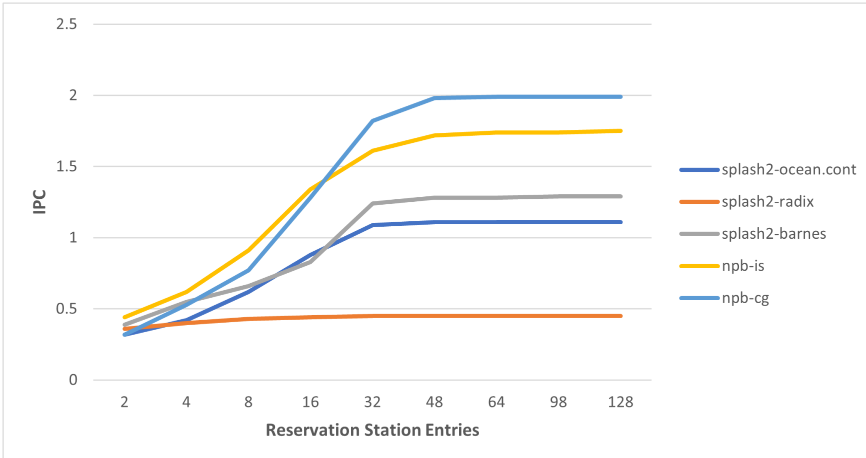



Figure 2: IPC across RS entry sweep for five benchmarks. IPC plateaus starting around 48 entries for all benchmarks, except for `splash2-radix`, where IPC remained largely consistent across the sweep. (*See Figure 6 for detailed data value table.*)

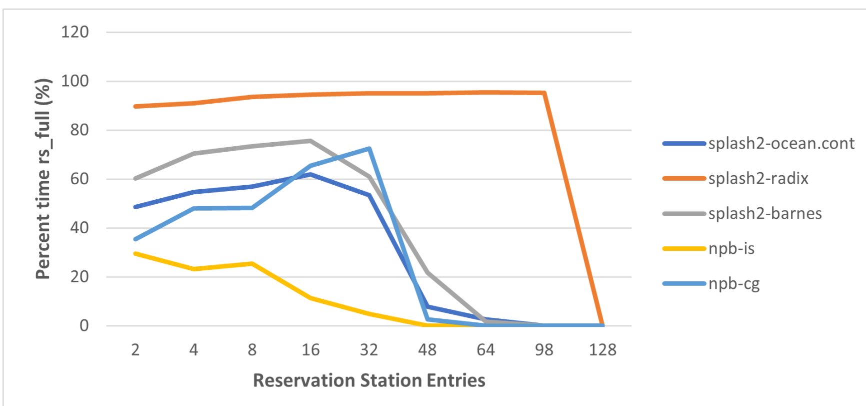



Figure 3: CPI Stack Result - Percent of time spent stalling where reservation stations were full. When a workload spends 0% of its time stalling when the RS's are full, this scenario is likely the result of instructions issuing and committing at a rate faster than the RS' could be filled, regardless of the time spent servicing misses OOO. (See Figure 10, 14, 18, 22, and 26 for correlating CPI stacks.)

**No ILP benefits from OOO:** For workloads likely to not have many dependencies and implemented with little to no parallelism, they see little to no benefits in increasing the number of RS'. `splash2-radix` (orange) is a radix sort algorithm and the simplest of the five workloads. For most of the RS sweep, most of its execution time is spent waiting due to the RS' being full (Figure 3), a structural hazard that stalls instruction issues [5]. Instructions are likely loading into the RS' without misses because of the lack of dependencies, meaning instructions were entering, executing, and committing in order, but still paying for the overhead of an OOO architecture. Figure 2 shows that for `splash2-radix`, IPC does not significantly change whether it is running with 2 or 128 RS'. So, such an application that does not utilize nor take advantage of OOO execution also does not see performance gains.

**Upper limit of exploiting ILP:** For the remaining four workloads, increasing RS entries improved performance, but only to a point. OOO techniques using RS' allow fetching and decoding those instructions following those instructions associated with a miss which are handled later, which can result in performance gains of about 20% over that of a perfect instruction cache [8]. In Figure 2, these performance gains are seen in the remaining four benchmarks. The two `npb` highly parallel workloads see the most improvement in IPC when increasing RS', despite the experiment running on a single core and not promoting thread-level parallelism, indicating that even exploiting some ILP positively impacts parallel applications and that the effects of varying RS entries on performance is application dependent.

Equally as evident is that the IPC for each application levels-off around 48 RS'. Attempting to exploit large amounts of ILP is known to fail [5], so no performance increase is seen after about 48 RS'. Notice that this is also around where these four applications spend 0% or close to 0% of their time stalling due to stalling with filled RS'. When not stalling, they may be dealing with a variety of other factors due to the burden of the hardware handling higher numbers of in-flight instructions, such as increased memory throttling and latency, executing instructions, serving misses, or stalling due to other resource conflicts. If more benchmarks were included and the experiment sweeps even more number of RS', it is possible to even see performance degrade for some workloads, as good results are usually seen at around 64 instructions in-flight [7]. These results show that an optimal number of RS entries for performance depends on the particular workloads.

## 3.2 Energy Consumption

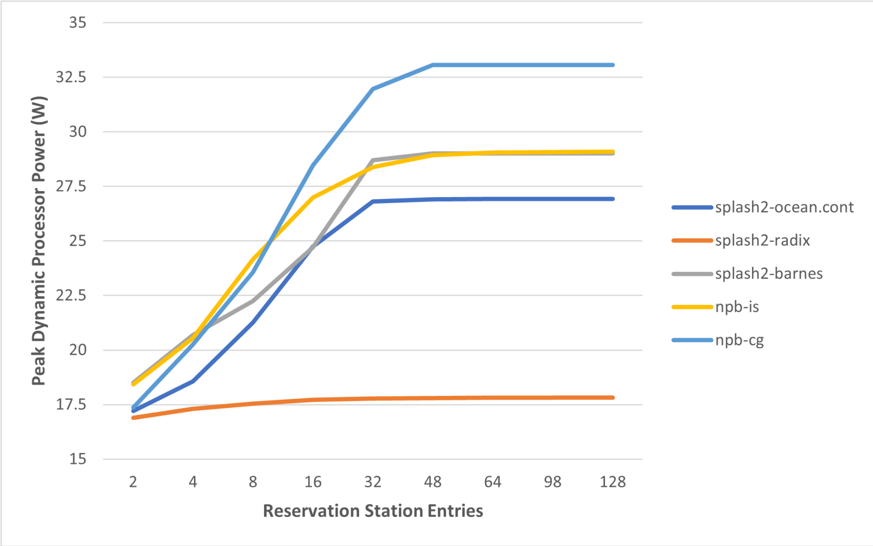



Figure 4: Peak dynamic processor power across RS entry sweep for five benchmarks. Peak dynamic power plateaus around 32 and 48 entries for most benchmarks, except for `splash2-radix`, where it remained consistent across the sweep. (*See Figure 7 for detailed data value table.*)

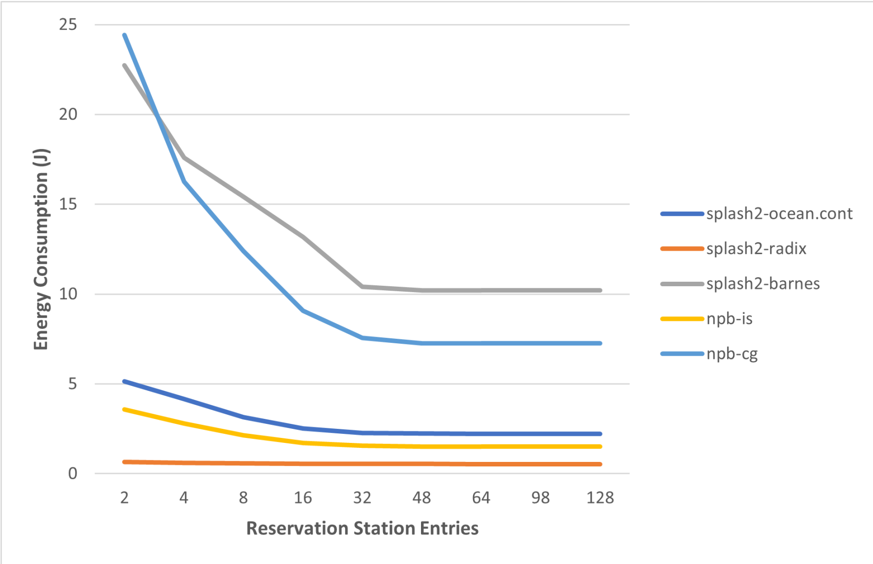


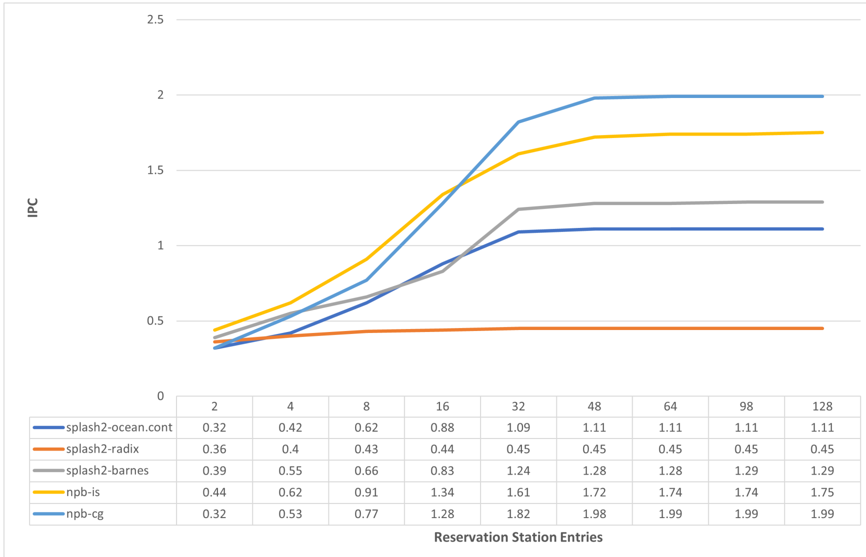

Figure 5: Total energy consumption across RS entry sweep for five benchmarks. Energy plateaus around 32-48 RS entries, and varies more widely for more complex workloads. (See Figure 8, 12, 16, 20, and 24 for correlating Power results.)

Much like how the IPC is seen to level-off (Section 3.1), peak dynamic processor power and total energy consumption also plateau around 32-48 RS entries (Figure 4 and 5, respectively) for similar reasons. Simple workloads that see no advantage in ILP like `splash2-radix` see little variation with either metrics. For the remaining four workloads more evidently affected by the number of RS', peak dynamic power is seen to increase with increasing RS'. This may have to do with the hardware architecture itself, as the common data bus (CDB) must broadcast operands to waiting units (register files, reservation stations, and store buffers) simultaneously when they become available. Figure 5 shows total energy consumption decreases until the plateau. Techniques for parallelism can potentially increase energy consumption if they degrade performance or increase execution time [5]. Since it is shown that performance improves somewhat in Section 3.1, increasing the RS entries improves energy efficiency until the "equilibrium" around 48 RS' when issuing, executing, and committing instructions see a consistent IPC. As mentioned previously, if the experiment sweeps additional workloads and continues increasing RS entries, it may show either these same results at 48 RS' or loss of efficiency and performance (i.e. decreasing IPC and increasing energy consumption)

# 4 Conclusion

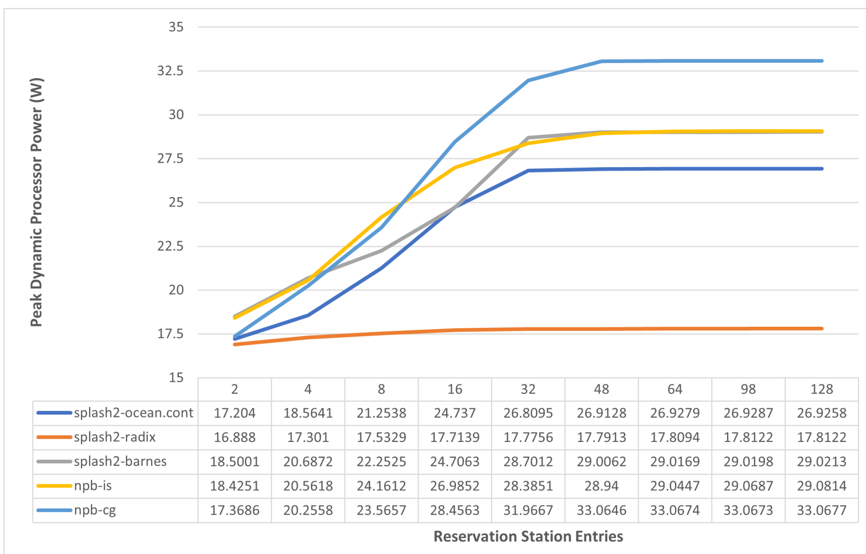
Sweeping RS entries show consistent results with what is known in the literature. For most of the workloads, the benefits of ILP are seen in the improved performance and reduced energy consumption. Due to limitations of how much ILP can be exploited, performance only increases to a point, then remains consistent afterward; likewise for the reduction in energy consumption. The results plateau at about 48 RS', but the "optimal" number appears to generally be somewhere between 32 and 64. For the least memory intensive and parallel workload, `splash2-radix`, the results remained consistent through the entire sweep. If time permitted, this experiment would benefit from a more fine-grain and wider sweep of the RS entries in order to find which number of RS entries are "optimal" for particular workloads. It should also include more benchmarks in order to see what applications become negatively impacted by higher number of RS' or if they yield other trends. In addition, other factors of interest to examine are how performance and energy will change for varying commit widths and the number of cores. To get the simulations to run within the appropriate time, the commit width is kept large here, but using smaller commit widths (2-8) would yield more realistic results. Likewise, most chips are multicores now, so seeing how results vary with the number of cores and increased TLP would give more interesting data, improve on the execution time for the highly parallel workloads, and show that the effect of RS entries on performance may also be architecture dependent.

# 5 Appendix: Detailed Result Values




| | 2 | 4 | 8 | 16 | 32 | 48 | 64 | 98 | 128 |
|---|---|---|---|---|---|---|---|---|---|
| splash2-ocean.cont | 0.32 | 0.42 | 0.62 | 0.88 | 1.09 | 1.11 | 1.11 | 1.11 | 1.11 |
| splash2-radix | 0.36 | 0.4 | 0.43 | 0.44 | 0.45 | 0.45 | 0.45 | 0.45 | 0.45 |
| splash2-barnes | 0.39 | 0.55 | 0.66 | 0.83 | 1.24 | 1.28 | 1.28 | 1.29 | 1.29 |
| npb-is | 0.44 | 0.62 | 0.91 | 1.34 | 1.61 | 1.72 | 1.74 | 1.74 | 1.75 |
| npb-cg | 0.32 | 0.53 | 0.77 | 1.28 | 1.82 | 1.98 | 1.99 | 1.99 | 1.99 |

Figure 6: IPC across RS entry sweep for five benchmarks that includes specific value at each sweep. See Figure 2 for discussion.



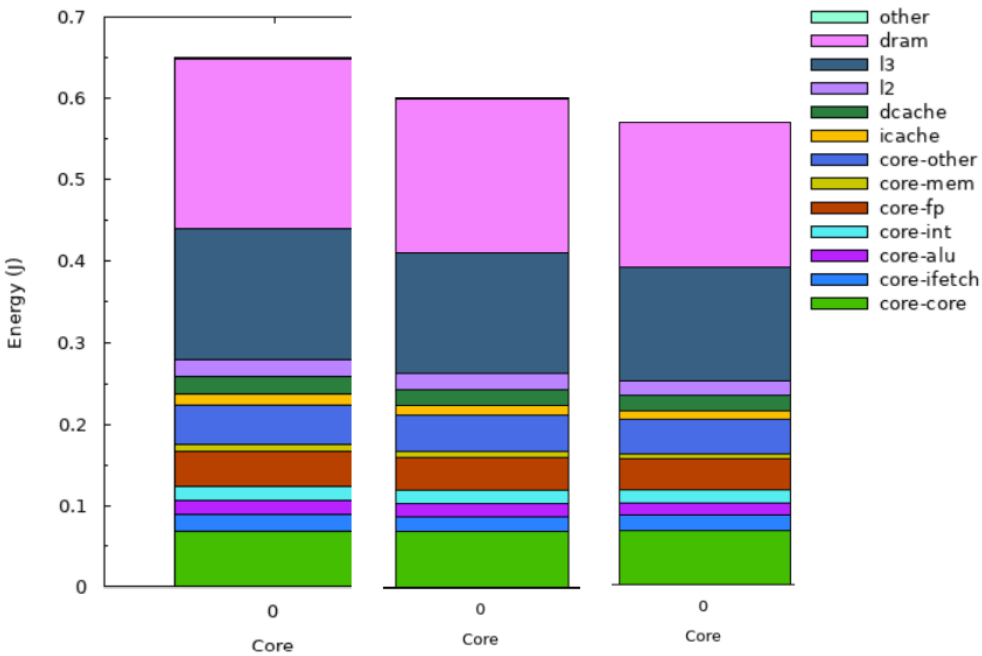

| | 2 | 4 | 8 | 16 | 32 | 48 | 64 | 98 | 128 |
|---|---|---|---|---|---|---|---|---|---|
| splash2-ocean.cont | 17.204 | 18.5641 | 21.2538 | 24.737 | 26.8095 | 26.9128 | 26.9279 | 26.9287 | 26.9258 |
| splash2-radix | 16.888 | 17.301 | 17.5329 | 17.7139 | 17.7756 | 17.7913 | 17.8094 | 17.8122 | 17.8122 |
| splash2-barnes | 18.5001 | 20.6872 | 22.2525 | 24.7063 | 28.7012 | 29.0062 | 29.0169 | 29.0198 | 29.0213 |
| npb-is | 18.4251 | 20.5618 | 24.1612 | 26.9852 | 28.3851 | 28.94 | 29.0447 | 29.0687 | 29.0814 |
| npb-cg | 17.3686 | 20.2558 | 23.5657 | 28.4563 | 31.9667 | 33.0646 | 33.0674 | 33.0673 | 33.0677 |

Figure 7: Peak dynamic processor power across RS entry sweep for five benchmarks that includes specific value at each sweep. See Figure 4 for discussion.

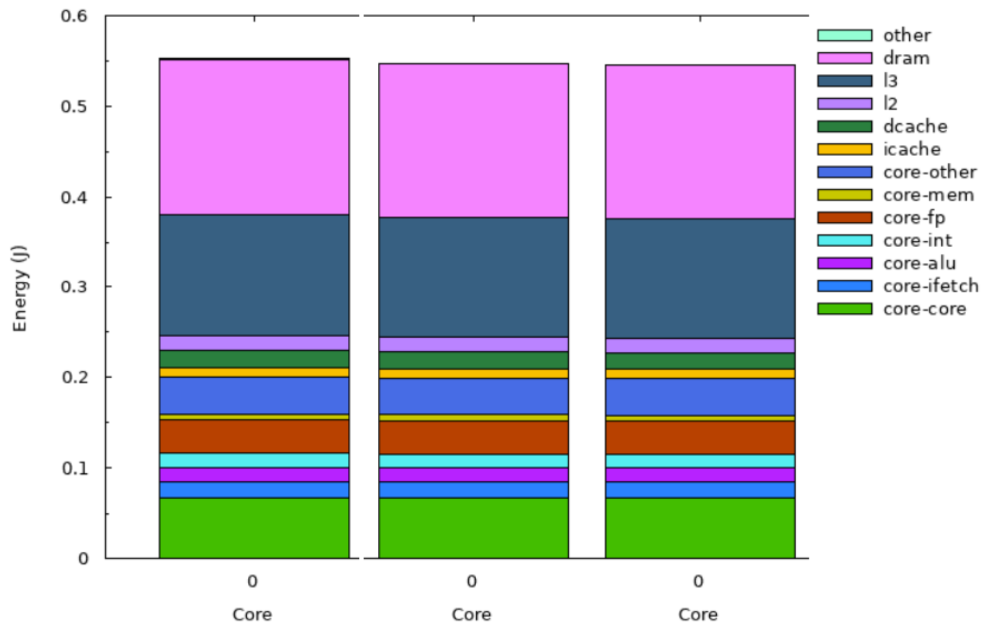
# 6 Appendix: Raw Post Processed Data

## 6.1 splash2-radix

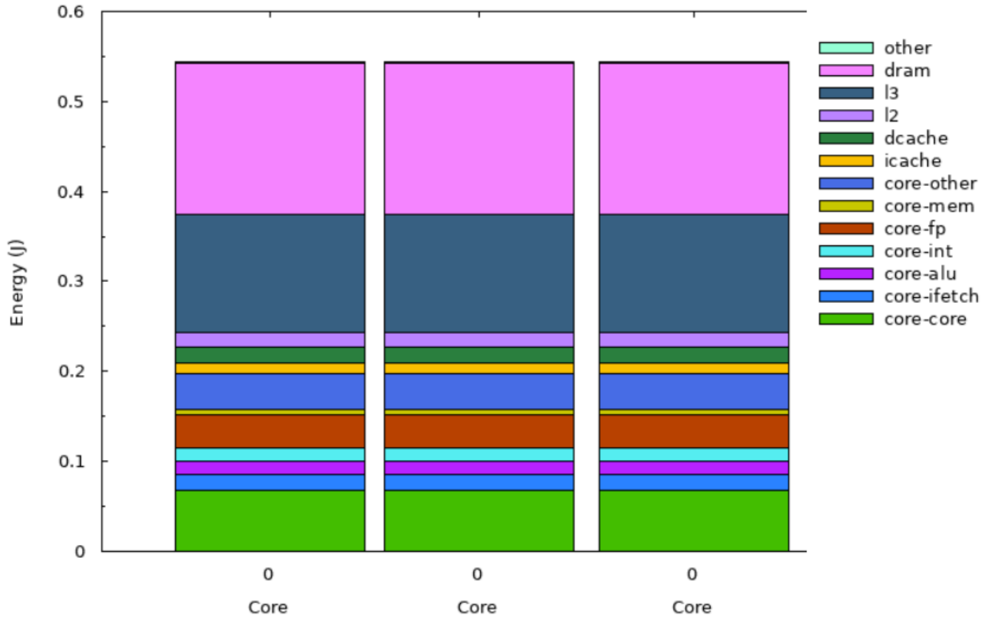
### 6.1.1 Power Results




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.




(d) 16 RS entries. (e) 32 RS entries. (f) 48 RS entries.



(g) 64 RS entries. (h) 98 RS entries. (i) 128 RS entries.

Figure 8: Processor power for various number of reservation station entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.44 W | 0.07 J | 10.69% |
| core-ifetch | 0.41 W | 0.02 J | 3.05% |
| core-alu | 0.36 W | 0.02 J | 2.68% |
| core-int | 0.36 W | 0.02 J | 2.70% |
| core-fp | 0.90 W | 0.04 J | 6.67% |
| core-mem | 0.15 W | 7.13 mJ | 1.10% |
| core-other | 1.03 W | 0.05 J | 7.63% |
| icache | 0.26 W | 0.01 J | 1.93% |
| dcache | 0.43 W | 0.02 J | 3.20% |
| l2 | 0.42 W | 0.02 J | 3.12% |
| l3 | 3.38 W | 0.16 J | 25.07% |
| dram | 4.31 W | 0.21 J | 31.96% |
| other | 0.03 W | 1.25 mJ | 0.19% |
| | | | |
| core | 4.66 W | 0.22 J | 34.53% |
| cache | 4.49 W | 0.22 J | 33.32% |
| total | 13.48 W | 0.65 J | 100.00% |

(a) 2 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.58 W | 0.07 J | 11.51% |
| core-ifetch | 0.43 W | 0.02 J | 3.13% |
| core-alu | 0.37 W | 0.02 J | 2.69% |
| core-int | 0.37 W | 0.02 J | 2.73% |
| core-fp | 0.92 W | 0.04 J | 6.69% |
| core-mem | 0.16 W | 6.78 mJ | 1.14% |
| core-other | 1.03 W | 0.04 J | 7.51% |
| icache | 0.27 W | 0.01 J | 1.94% |
| dcache | 0.45 W | 0.02 J | 3.26% |
| l2 | 0.42 W | 0.02 J | 3.07% |
| l3 | 3.38 W | 0.15 J | 24.67% |
| dram | 4.31 W | 0.19 J | 31.48% |
| other | 0.03 W | 1.13 mJ | 0.19% |
| | | | |
| core | 4.85 W | 0.21 J | 35.39% |
| cache | 4.51 W | 0.20 J | 32.94% |
| total | 13.71 W | 0.60 J | 100.00% |

(b) 4 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.65 W | 0.07 J | 11.96% |
| core-ifetch | 0.44 W | 0.02 J | 3.17% |
| core-alu | 0.37 W | 0.02 J | 2.70% |
| core-int | 0.38 W | 0.02 J | 2.74% |
| core-fp | 0.93 W | 0.04 J | 6.69% |
| core-mem | 0.16 W | 6.60 mJ | 1.16% |
| core-other | 1.03 W | 0.04 J | 7.44% |
| icache | 0.27 W | 0.01 J | 1.94% |
| dcache | 0.46 W | 0.02 J | 3.30% |
| l2 | 0.42 W | 0.02 J | 3.05% |
| l3 | 3.38 W | 0.14 J | 24.44% |
| dram | 4.32 W | 0.18 J | 31.22% |
| other | 0.03 W | 1.07 mJ | 0.19% |
| | | | |
| core | 4.96 W | 0.20 J | 35.86% |
| cache | 4.53 W | 0.19 J | 32.73% |
| total | 13.83 W | 0.57 J | 100.00% |

(c) 8 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.71 W | 0.07 J | 12.31% |
| core-ifetch | 0.45 W | 0.02 J | 3.21% |
| core-alu | 0.38 W | 0.01 J | 2.70% |
| core-int | 0.38 W | 0.02 J | 2.75% |
| core-fp | 0.93 W | 0.04 J | 6.70% |
| core-mem | 0.16 W | 6.48 mJ | 1.17% |
| core-other | 1.03 W | 0.04 J | 7.39% |
| icache | 0.27 W | 0.01 J | 1.95% |
| dcache | 0.46 W | 0.02 J | 3.33% |
| l2 | 0.42 W | 0.02 J | 3.03% |
| l3 | 3.38 W | 0.13 J | 24.28% |
| dram | 4.32 W | 0.17 J | 31.01% |
| other | 0.03 W | 1.03 mJ | 0.19% |
| | | | |
| core | 5.05 W | 0.20 J | 36.22% |
| cache | 4.54 W | 0.18 J | 32.57% |
| total | 13.93 W | 0.55 J | 100.00% |

(d) 16 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.73 W | 0.07 J | 12.43% |
| core-ifetch | 0.45 W | 0.02 J | 3.22% |
| core-alu | 0.38 W | 0.01 J | 2.70% |
| core-int | 0.38 W | 0.02 J | 2.75% |
| core-fp | 0.94 W | 0.04 J | 6.70% |
| core-mem | 0.16 W | 6.44 mJ | 1.18% |
| core-other | 1.03 W | 0.04 J | 7.37% |
| icache | 0.27 W | 0.01 J | 1.95% |
| dcache | 0.47 W | 0.02 J | 3.33% |
| l2 | 0.42 W | 0.02 J | 3.02% |
| l3 | 3.38 W | 0.13 J | 24.22% |
| dram | 4.32 W | 0.17 J | 30.95% |
| other | 0.03 W | 1.02 mJ | 0.19% |
| | | | |
| core | 5.08 W | 0.20 J | 36.35% |
| cache | 4.54 W | 0.18 J | 32.52% |
| total | 13.96 W | 0.55 J | 100.00% |

(e) 32 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.74 W | 0.07 J | 12.45% |
| core-ifetch | 0.45 W | 0.02 J | 3.22% |
| core-alu | 0.38 W | 0.01 J | 2.70% |
| core-int | 0.38 W | 0.02 J | 2.75% |
| core-fp | 0.94 W | 0.04 J | 6.70% |
| core-mem | 0.16 W | 6.43 mJ | 1.18% |
| core-other | 1.03 W | 0.04 J | 7.37% |
| icache | 0.27 W | 0.01 J | 1.95% |
| dcache | 0.47 W | 0.02 J | 3.34% |
| l2 | 0.42 W | 0.02 J | 3.02% |
| l3 | 3.38 W | 0.13 J | 24.20% |
| dram | 4.32 W | 0.17 J | 30.93% |
| other | 0.03 W | 1.01 mJ | 0.19% |
| | | | |
| core | 5.08 W | 0.20 J | 36.38% |
| cache | 4.54 W | 0.18 J | 32.51% |
| total | 13.97 W | 0.55 J | 100.00% |

(f) 48 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.75 W | 0.07 J | 12.49% |
| core-ifetch | 0.45 W | 0.02 J | 3.22% |
| core-alu | 0.38 W | 0.01 J | 2.70% |
| core-int | 0.39 W | 0.01 J | 2.75% |
| core-fp | 0.94 W | 0.04 J | 6.70% |
| core-mem | 0.16 W | 6.42 mJ | 1.18% |
| core-other | 1.03 W | 0.04 J | 7.36% |
| icache | 0.27 W | 0.01 J | 1.95% |
| dcache | 0.47 W | 0.02 J | 3.34% |
| l2 | 0.42 W | 0.02 J | 3.02% |
| l3 | 3.38 W | 0.13 J | 24.19% |
| dram | 4.32 W | 0.17 J | 30.91% |
| other | 0.03 W | 1.01 mJ | 0.19% |
| | | | |
| core | 5.09 W | 0.20 J | 36.41% |
| cache | 4.54 W | 0.18 J | 32.49% |
| total | 13.98 W | 0.54 J | 100.00% |

(g) 64 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.75 W | 0.07 J | 12.49% |
| core-ifetch | 0.45 W | 0.02 J | 3.22% |
| core-alu | 0.38 W | 0.01 J | 2.70% |
| core-int | 0.39 W | 0.01 J | 2.75% |
| core-fp | 0.94 W | 0.04 J | 6.70% |
| core-mem | 0.17 W | 6.42 mJ | 1.18% |
| core-other | 1.03 W | 0.04 J | 7.36% |
| icache | 0.27 W | 0.01 J | 1.95% |
| dcache | 0.47 W | 0.02 J | 3.34% |
| l2 | 0.42 W | 0.02 J | 3.02% |
| l3 | 3.38 W | 0.13 J | 24.18% |
| dram | 4.32 W | 0.17 J | 30.91% |
| other | 0.03 W | 1.01 mJ | 0.19% |
| | | | |
| core | 5.09 W | 0.20 J | 36.42% |
| cache | 4.54 W | 0.18 J | 32.49% |
| total | 13.98 W | 0.54 J | 100.00% |

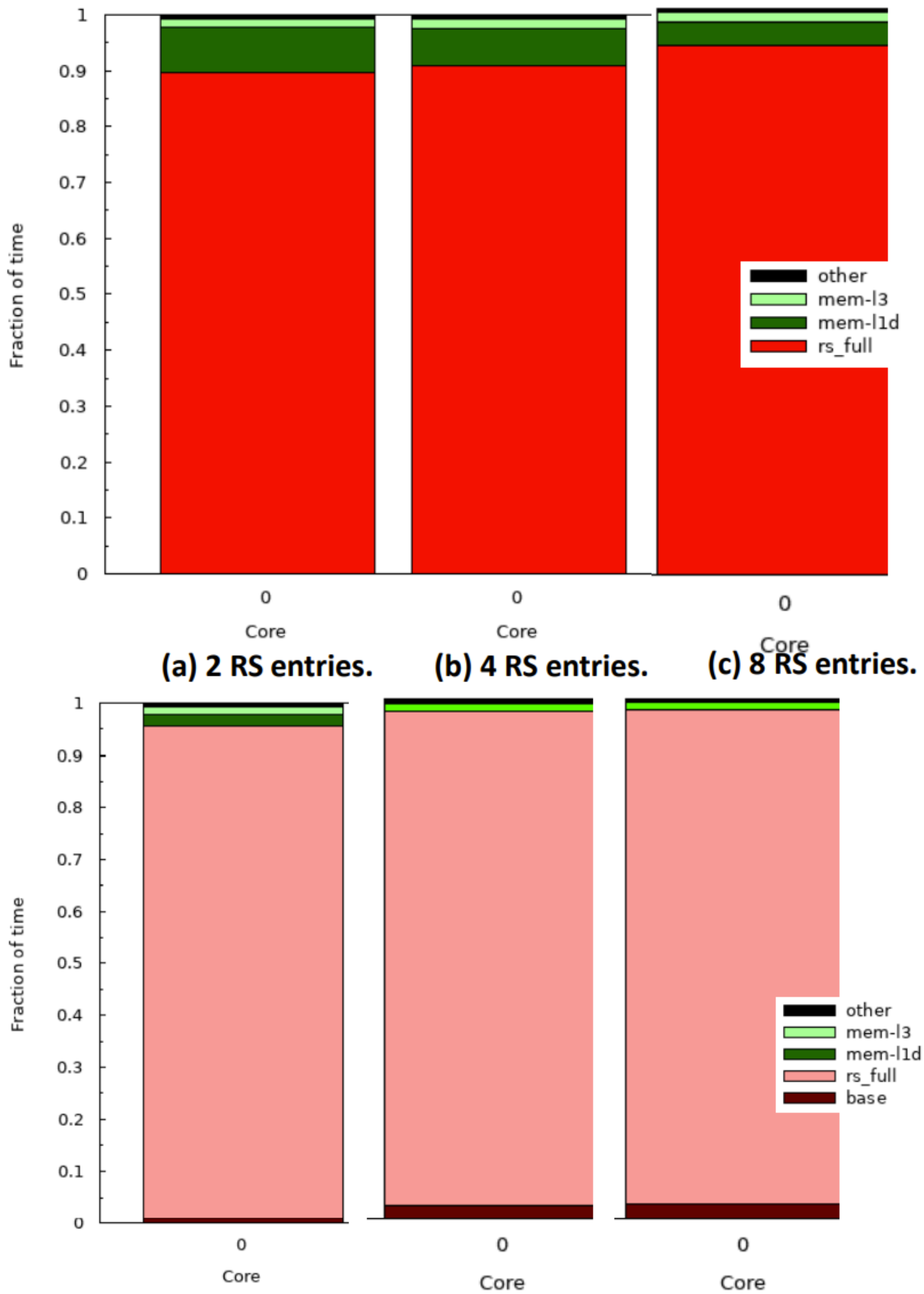
(h) 98 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.75 W | 0.07 J | 12.49% |
| core-ifetch | 0.45 W | 0.02 J | 3.22% |
| core-alu | 0.38 W | 0.01 J | 2.70% |
| core-int | 0.39 W | 0.01 J | 2.75% |
| core-fp | 0.94 W | 0.04 J | 6.70% |
| core-mem | 0.17 W | 6.42 mJ | 1.18% |
| core-other | 1.03 W | 0.04 J | 7.36% |
| icache | 0.27 W | 0.01 J | 1.95% |
| dcache | 0.47 W | 0.02 J | 3.34% |
| l2 | 0.42 W | 0.02 J | 3.02% |
| l3 | 3.38 W | 0.13 J | 24.18% |
| dram | 4.32 W | 0.17 J | 30.91% |
| other | 0.03 W | 1.01 mJ | 0.19% |
| | | | |
| core | 5.09 W | 0.20 J | 36.42% |
| cache | 4.54 W | 0.18 J | 32.49% |
| total | 13.98 W | 0.54 J | 100.00% |

(i) 128 RS entries.

Figure 9: Specific values for each components' power consumption.

### 6.1.2 CPI Stacks




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.

(d) 16 RS entries. (e) 32 RS entries. (f) 48 RS entries.

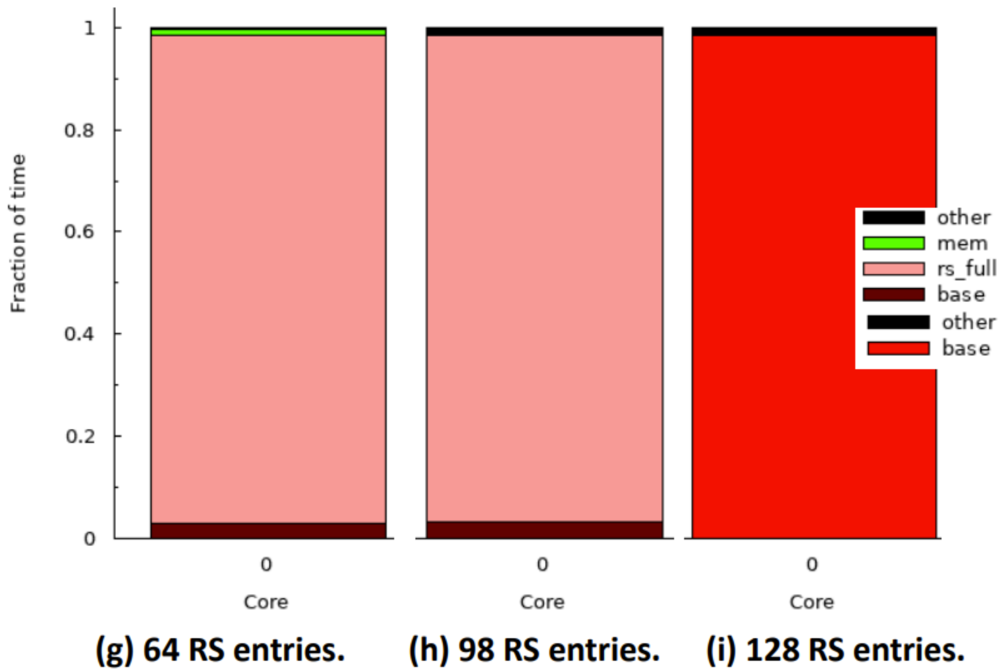



Figure 10: CPI stacks for various number of reservation station entries.

| | CPI | Time |
|---|---|---|
| rs_full | 2.46 | 89.60% |
| mem-l1d | 0.23 | 8.21% |
| mem-l3 | 0.04 | 1.51% |
| other | 0.02 | 0.68% |
| | | |
| total | 2.74 | 100.00% |

(a) 2 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 2.26 | 91.01% |
| mem-l1d | 0.16 | 6.63% |
| mem-l3 | 0.04 | 1.61% |
| other | 0.02 | 0.76% |
| | | |
| total | 2.48 | 100.00% |

(b) 4 RS entries.

```
                    CPI       Time
rs_full            2.20     93.51%
mem-l1d            0.10      4.17%
mem-l3             0.04      1.55%
other              0.02      0.77%

total              2.35    100.00%
```

(c) 8 RS entries.

```
                    CPI       Time
base               0.02      1.07%
rs_full            2.14     94.52%
mem-l1d            0.05      2.31%
mem-l3             0.03      1.34%
other              0.02      0.77%

total              2.26    100.00%
```

(d) 16 RS entries.

```
                    CPI       Time
base               0.06      2.54%
rs_full            2.12     95.05%
mem-l3             0.03      1.45%
other              0.02      0.97%

total              2.23    100.00%
```

(e) 32 RS entries.

```
                    CPI       Time
base               0.07      2.95%
rs_full            2.11     94.97%
mem-l3             0.03      1.31%
other              0.02      0.77%

total              2.22    100.00%
```

(f) 48 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.07 | 2.98% |
| rs_full | 2.11 | 95.36% |
| mem | 0.03 | 1.17% |
| other | 0.01 | 0.49% |
| total | 2.22 | 100.00% |

(g) 64 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.07 | 3.31% |
| rs_full | 2.11 | 95.28% |
| other | 0.03 | 1.41% |
| total | 2.21 | 100.00% |

(h) 98 RS entries.

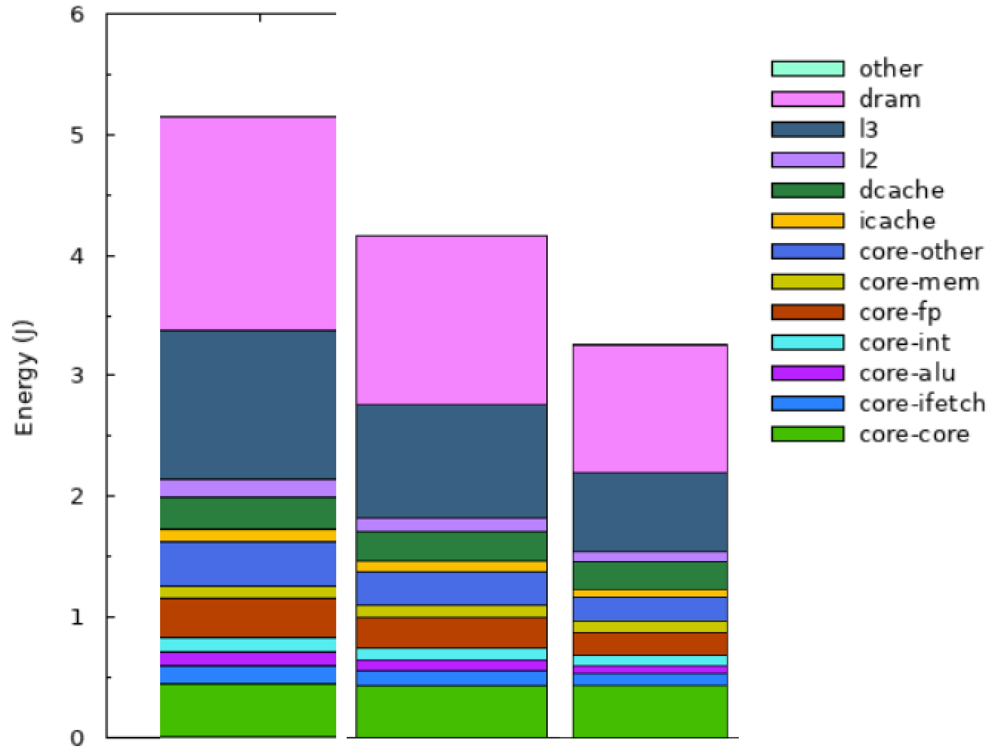
| | CPI | Time |
|---|---|---|
| base | 2.18 | 98.59% |
| other | 0.03 | 1.41% |
| total | 2.21 | 100.00% |

(i) 128 RS entries.

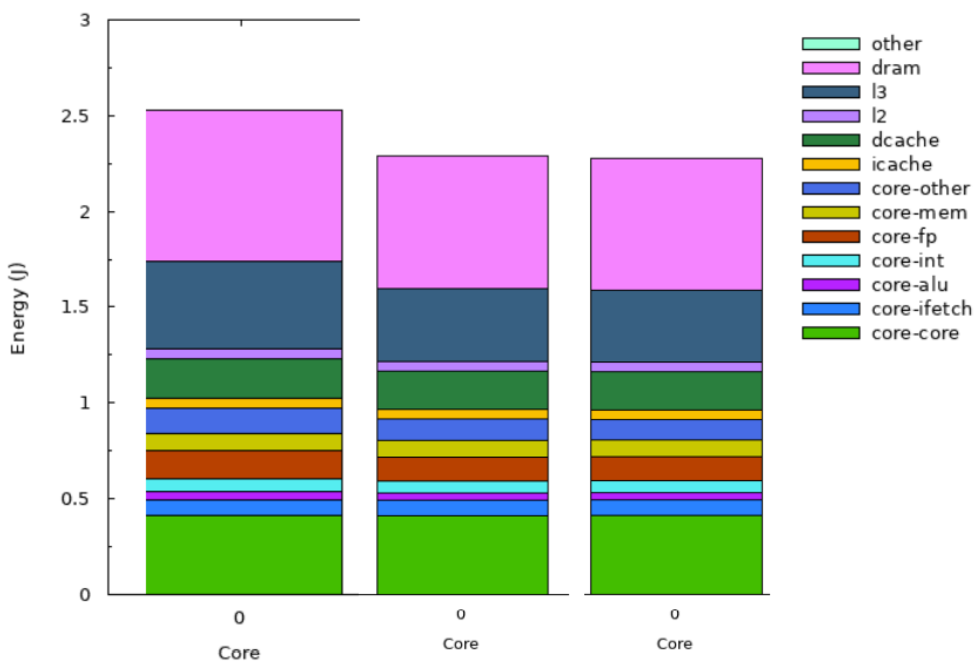
Figure 11: Specific values for each components' CPI stack.

## 6.2 splash2-ocean.cont

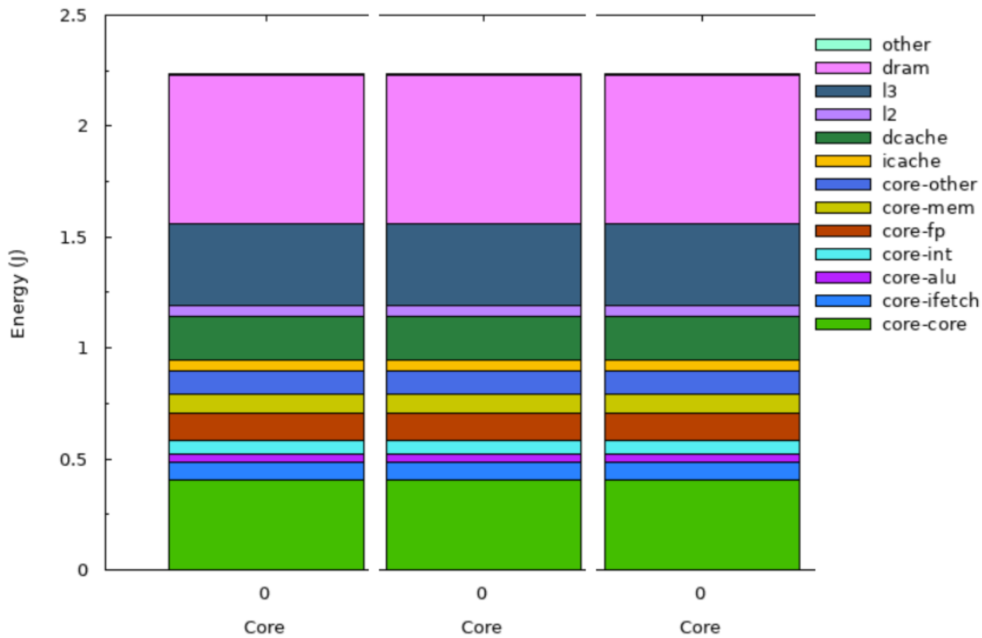
### 6.2.1 Power Results




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.




(d) 16 RS entries. (e) 32 RS entries. (f) 48 RS entries.




**(g) 64 RS entries.** **(h) 98 RS entries.** **(i) 128 RS entries.**

Figure 12: Processor power for various number of reservation station entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.25 W | 0.45 J | 8.72% |
| core-ifetch | 0.39 W | 0.14 J | 2.72% |
| core-alu | 0.32 W | 0.11 J | 2.21% |
| core-int | 0.36 W | 0.13 J | 2.50% |
| core-fp | 0.88 W | 0.31 J | 6.11% |
| core-mem | 0.30 W | 0.11 J | 2.06% |
| core-other | 1.03 W | 0.37 J | 7.15% |
| icache | 0.29 W | 0.10 J | 2.01% |
| dcache | 0.75 W | 0.27 J | 5.20% |
| l2 | 0.43 W | 0.15 J | 2.99% |
| l3 | 3.44 W | 1.23 J | 23.93% |
| dram | 4.93 W | 1.76 J | 34.23% |
| other | 0.03 W | 9.28 mJ | 0.18% |
| | | | |
| core | 4.53 W | 1.62 J | 31.47% |
| cache | 4.91 W | 1.76 J | 34.12% |
| total | 14.39 W | 5.15 J | 100.00% |

(a) 2 RS entries.

```
                 Power    Energy   Energy %
core-core       1.61 W    0.43  J    10.48%
core-ifetch     0.44 W    0.12  J     2.85%
core-alu        0.33 W    0.09  J     2.13%
core-int        0.39 W    0.10  J     2.51%
core-fp         0.92 W    0.25  J     6.00%
core-mem        0.37 W    0.10  J     2.40%
core-other      1.03 W    0.28  J     6.70%
icache          0.31 W    0.08  J     2.04%
dcache          0.90 W    0.24  J     5.86%
l2              0.43 W    0.12  J     2.82%
l3              3.47 W    0.94  J    22.56%
dram            5.14 W    1.39  J    33.48%
other           0.03 W    7.00 mJ     0.17%

core            5.08 W    1.37  J    33.07%
cache           5.11 W    1.38  J    33.28%
total          15.37 W    4.15  J   100.00%
```

(b) 4 RS entries.

```
                 Power    Energy   Energy %
core-core       2.31 W    0.42  J    13.37%
core-ifetch     0.53 W    0.10  J     3.07%
core-alu        0.34 W    0.06  J     1.99%
core-int        0.44 W    0.08  J     2.53%
core-fp         1.01 W    0.18  J     5.84%
core-mem        0.51 W    0.09  J     2.95%
core-other      1.03 W    0.19  J     5.95%
icache          0.36 W    0.07  J     2.11%
dcache          1.20 W    0.22  J     6.95%
l2              0.44 W    0.08  J     2.56%
l3              3.51 W    0.64  J    20.29%
dram            5.58 W    1.01  J    32.25%
other           0.03 W    4.72 mJ     0.15%

core            6.18 W    1.12  J    35.70%
cache           5.52 W    1.00  J    31.90%
total          17.30 W    3.14  J   100.00%
```

(c) 8 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 3.22 W | 0.41 J | 16.28% |
| core-ifetch | 0.65 W | 0.08 J | 3.29% |
| core-alu | 0.37 W | 0.05 J | 1.85% |
| core-int | 0.51 W | 0.06 J | 2.55% |
| core-fp | 1.12 W | 0.14 J | 5.67% |
| core-mem | 0.69 W | 0.09 J | 3.50% |
| core-other | 1.03 W | 0.13 J | 5.20% |
| icache | 0.43 W | 0.05 J | 2.17% |
| dcache | 1.59 W | 0.20 J | 8.04% |
| l2 | 0.45 W | 0.06 J | 2.29% |
| l3 | 3.57 W | 0.46 J | 18.03% |
| dram | 6.14 W | 0.78 J | 31.00% |
| other | 0.03 W | 3.31 mJ | 0.13% |
| | | | |
| core | 7.59 W | 0.97 J | 38.34% |
| cache | 6.04 W | 0.77 J | 30.52% |
| total | 19.80 W | 2.53 J | 100.00% |

(d) 16 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 3.93 W | 0.41 J | 18.08% |
| core-ifetch | 0.75 W | 0.08 J | 3.43% |
| core-alu | 0.38 W | 0.04 J | 1.77% |
| core-int | 0.56 W | 0.06 J | 2.56% |
| core-fp | 1.21 W | 0.13 J | 5.57% |
| core-mem | 0.84 W | 0.09 J | 3.84% |
| core-other | 1.03 W | 0.11 J | 4.73% |
| icache | 0.48 W | 0.05 J | 2.21% |
| dcache | 1.90 W | 0.20 J | 8.72% |
| l2 | 0.46 W | 0.05 J | 2.12% |
| l3 | 3.62 W | 0.37 J | 16.62% |
| dram | 6.58 W | 0.68 J | 30.24% |
| other | 0.03 W | 2.69 mJ | 0.12% |
| | | | |
| core | 8.70 W | 0.90 J | 39.98% |
| cache | 6.45 W | 0.67 J | 29.67% |
| total | 21.76 W | 2.26 J | 100.00% |

(e) 32 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 3.99 W | 0.41 J | 18.22% |
| core-ifetch | 0.75 W | 0.08 J | 3.44% |
| core-alu | 0.39 W | 0.04 J | 1.76% |
| core-int | 0.56 W | 0.06 J | 2.56% |
| core-fp | 1.22 W | 0.12 J | 5.56% |
| core-mem | 0.85 W | 0.09 J | 3.87% |
| core-other | 1.03 W | 0.11 J | 4.70% |
| icache | 0.48 W | 0.05 J | 2.21% |
| dcache | 1.92 W | 0.20 J | 8.77% |
| l2 | 0.46 W | 0.05 J | 2.11% |
| l3 | 3.62 W | 0.37 J | 16.51% |
| dram | 6.61 W | 0.68 J | 30.18% |
| other | 0.03 W | 2.65 mJ | 0.12% |
| | | | |
| core | 8.79 W | 0.90 J | 40.10% |
| cache | 6.49 W | 0.66 J | 29.60% |
| total | 21.92 W | 2.24 J | 100.00% |

(f) 48 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.00 W | 0.41 J | 18.24% |
| core-ifetch | 0.75 W | 0.08 J | 3.44% |
| core-alu | 0.39 W | 0.04 J | 1.76% |
| core-int | 0.56 W | 0.06 J | 2.56% |
| core-fp | 1.22 W | 0.12 J | 5.56% |
| core-mem | 0.85 W | 0.09 J | 3.87% |
| core-other | 1.03 W | 0.10 J | 4.69% |
| icache | 0.49 W | 0.05 J | 2.21% |
| dcache | 1.93 W | 0.20 J | 8.78% |
| l2 | 0.46 W | 0.05 J | 2.11% |
| l3 | 3.62 W | 0.37 J | 16.50% |
| dram | 6.62 W | 0.67 J | 30.16% |
| other | 0.03 W | 2.64 mJ | 0.12% |
| | | | |
| core | 8.80 W | 0.90 J | 40.12% |
| cache | 6.49 W | 0.66 J | 29.59% |
| total | 21.94 W | 2.23 J | 100.00% |

(g) 64 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.00 W | 0.41 J | 18.24% |
| core-ifetch | 0.75 W | 0.08 J | 3.44% |
| core-alu | 0.39 W | 0.04 J | 1.76% |
| core-int | 0.56 W | 0.06 J | 2.56% |
| core-fp | 1.22 W | 0.12 J | 5.56% |
| core-mem | 0.85 W | 0.09 J | 3.87% |
| core-other | 1.03 W | 0.10 J | 4.69% |
| icache | 0.49 W | 0.05 J | 2.21% |
| dcache | 1.93 W | 0.20 J | 8.78% |
| l2 | 0.46 W | 0.05 J | 2.11% |
| l3 | 3.62 W | 0.37 J | 16.50% |
| dram | 6.62 W | 0.67 J | 30.16% |
| other | 0.03 W | 2.64 mJ | 0.12% |
| | | | |
| core | 8.80 W | 0.90 J | 40.12% |
| cache | 6.49 W | 0.66 J | 29.59% |
| total | 21.94 W | 2.23 J | 100.00% |

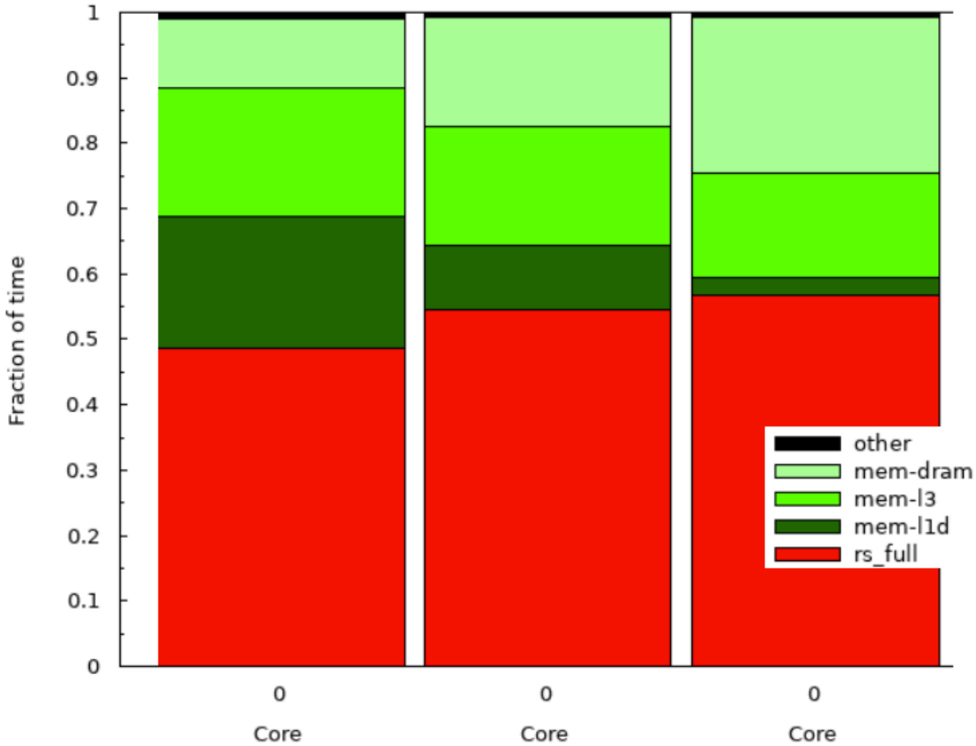
(h) 98 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.00 W | 0.41 J | 18.23% |
| core-ifetch | 0.75 W | 0.08 J | 3.44% |
| core-alu | 0.39 W | 0.04 J | 1.76% |
| core-int | 0.56 W | 0.06 J | 2.56% |
| core-fp | 1.22 W | 0.12 J | 5.56% |
| core-mem | 0.85 W | 0.09 J | 3.87% |
| core-other | 1.03 W | 0.10 J | 4.69% |
| icache | 0.49 W | 0.05 J | 2.21% |
| dcache | 1.92 W | 0.20 J | 8.77% |
| l2 | 0.46 W | 0.05 J | 2.11% |
| l3 | 3.62 W | 0.37 J | 16.50% |
| dram | 6.62 W | 0.67 J | 30.18% |
| other | 0.03 W | 2.64 mJ | 0.12% |
| | | | |
| core | 8.80 W | 0.90 J | 40.11% |
| cache | 6.49 W | 0.66 J | 29.59% |
| total | 21.94 W | 2.23 J | 100.00% |

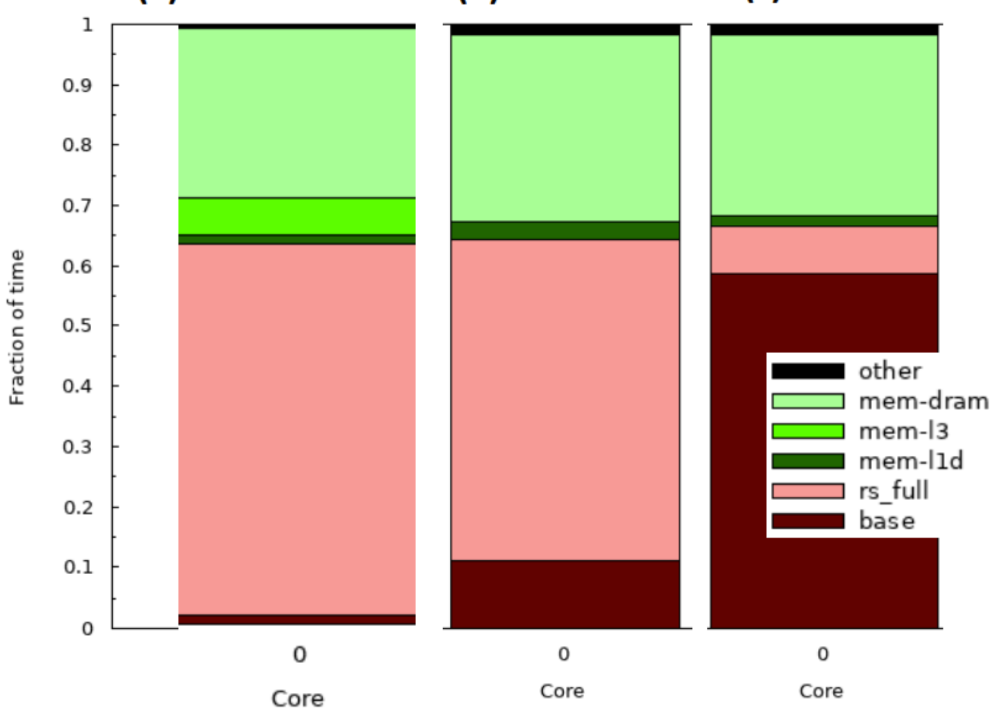
(i) 128 RS entries.

Figure 13: Specific values for each components' power consumption.

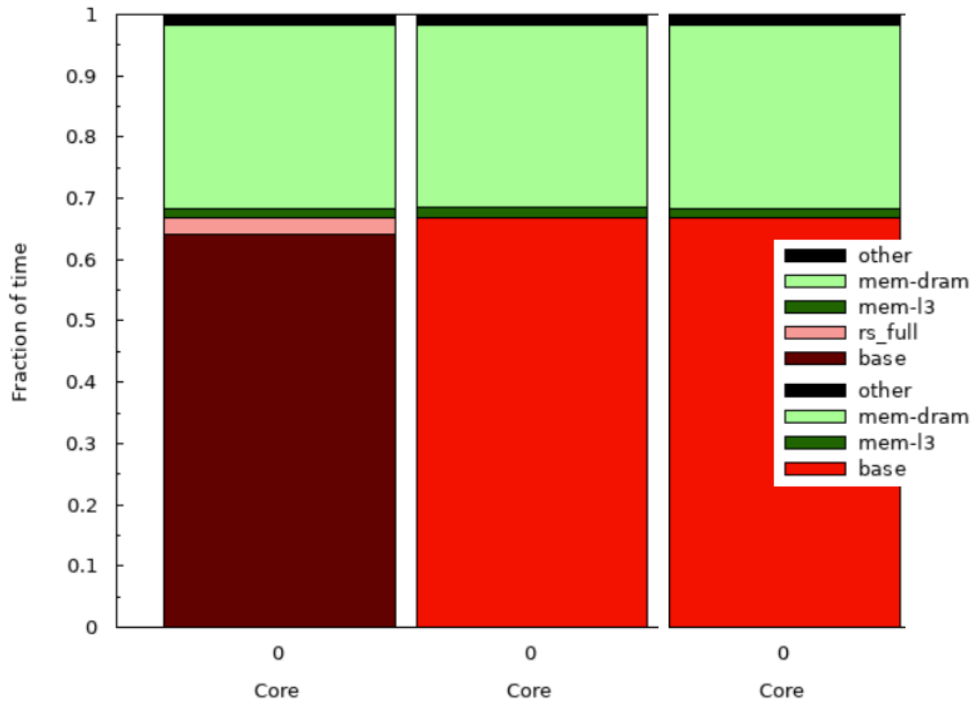
### 6.2.2 CPI Stacks




**(a) 2 RS entries.** **(b) 4 RS entries.** **(c) 8 RS entries.**




**(d) 16 RS entries.** **(e) 32 RS entries.** **(f) 48 RS entries.**




**(g) 64 RS entries.** **(h) 98 RS entries.** **(i) 128 RS entries.**

Figure 14: CPI stacks for various number of reservation station entries.

| | CPI | Time |
|---|---|---|
| rs_full | 1.54 | 48.61% |
| mem-l1d | 0.64 | 20.30% |
| mem-l3 | 0.62 | 19.48% |
| mem-dram | 0.34 | 10.63% |
| other | 0.03 | 0.99% |
| total | 3.17 | 100.00% |

(a) 2 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 1.30 | 54.57% |
| mem-l1d | 0.23 | 9.82% |
| mem-l3 | 0.43 | 18.11% |
| mem-dram | 0.40 | 16.68% |
| other | 0.02 | 0.82% |
| total | 2.39 | 100.00% |

(b) 4 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 0.91 | 56.82% |
| mem-l1d | 0.04 | 2.55% |
| mem-l3 | 0.26 | 16.10% |
| mem-dram | 0.38 | 23.86% |
| other | 0.01 | 0.67% |
| | | |
| total | 1.61 | 100.00% |

(c) 8 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.02 | 1.60% |
| rs_full | 0.70 | 61.92% |
| mem-l1d | 0.02 | 1.44% |
| mem-l3 | 0.07 | 6.08% |
| mem-dram | 0.32 | 28.21% |
| other | 0.01 | 0.75% |
| | | |
| total | 1.13 | 100.00% |

(d) 16 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.10 | 11.05% |
| rs_full | 0.49 | 53.39% |
| mem-l3 | 0.03 | 2.88% |
| mem-dram | 0.28 | 30.99% |
| other | 0.02 | 1.68% |
| | | |
| total | 0.92 | 100.00% |

(e) 32 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.53 | 58.60% |
| rs_full | 0.07 | 7.90% |
| mem-l3 | 0.02 | 1.84% |
| mem-dram | 0.27 | 29.92% |
| other | 0.02 | 1.74% |
| | | |
| total | 0.90 | 100.00% |

(f) 48 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.58 | 64.03% |
| rs_full | 0.02 | 2.72% |
| mem-l3 | 0.01 | 1.61% |
| mem-dram | 0.27 | 29.89% |
| other | 0.02 | 1.75% |
| | | |
| total | 0.90 | 100.00% |

(g) 64 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.60 | 66.88% |
| mem-l3 | 0.01 | 1.58% |
| mem-dram | 0.27 | 29.82% |
| other | 0.02 | 1.73% |
| | | |
| total | 0.90 | 100.00% |

(h) 98 RS entries.

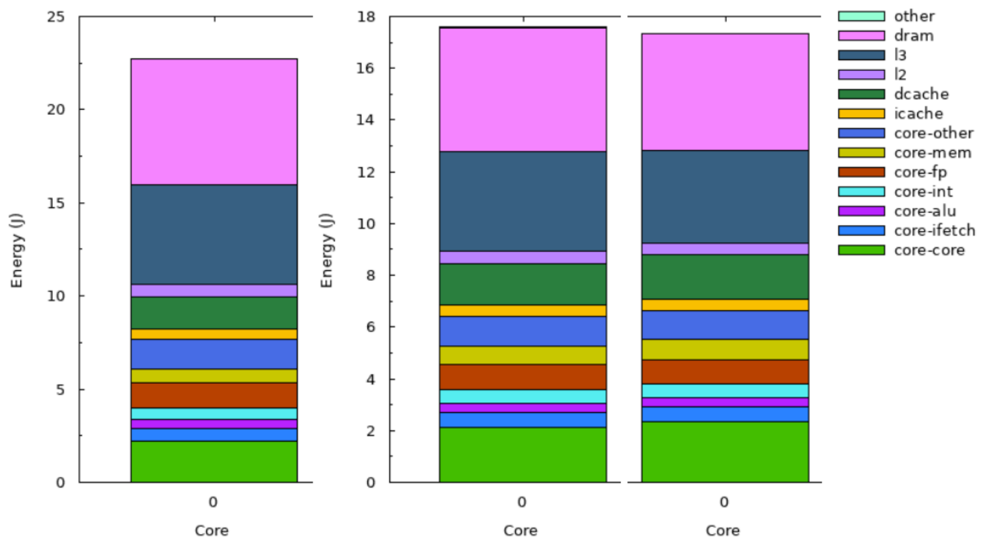
| | CPI | Time |
|---|---|---|
| base | 0.60 | 66.86% |
| mem-l3 | 0.01 | 1.56% |
| mem-dram | 0.27 | 29.86% |
| other | 0.02 | 1.72% |
| | | |
| total | 0.90 | 100.00% |

(i) 128 RS entries.

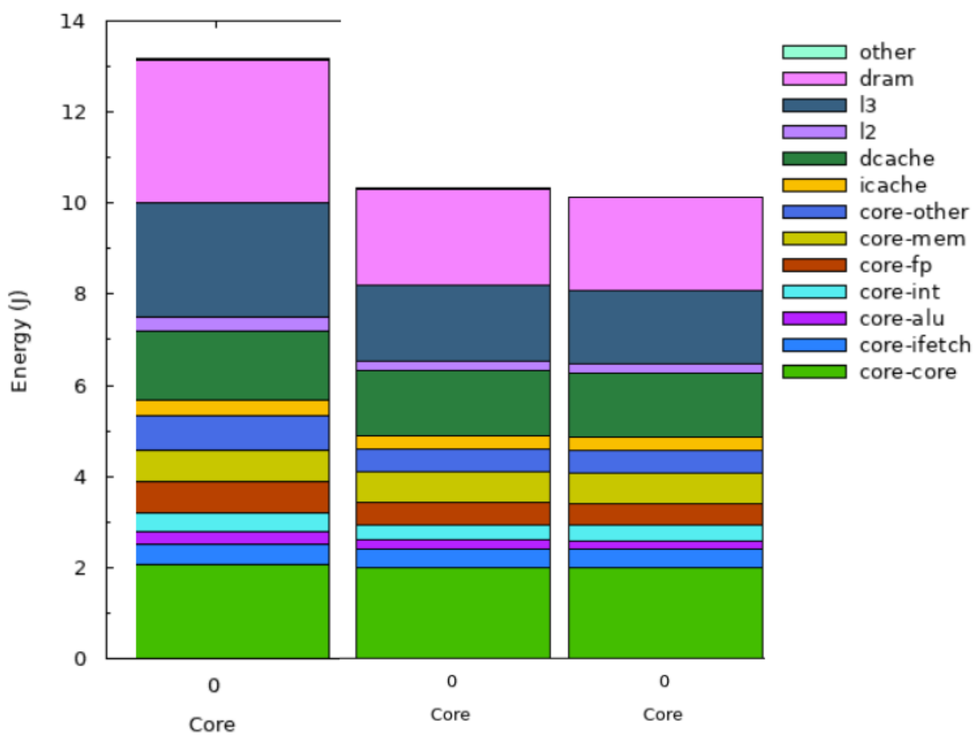
Figure 15: Specific values for each components' CPI stack.

## 6.3 splash2-barnes

### 6.3.1 Power Results




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.




(d) 16 RS entries. (f) 48 RS entries.

(e) 32 RS entries.

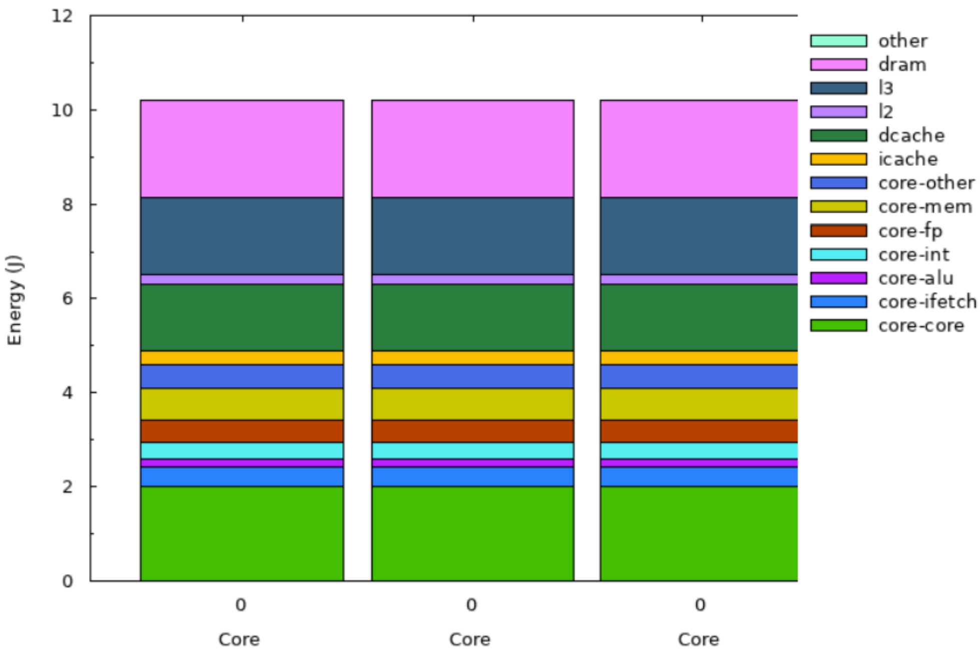



Figure 16: Processor power for various number of reservation station entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.38 W | 2.19 J | 9.61% |
| core-ifetch | 0.43 W | 0.68 J | 2.99% |
| core-alu | 0.32 W | 0.51 J | 2.23% |
| core-int | 0.40 W | 0.64 J | 2.81% |
| core-fp | 0.83 W | 1.32 J | 5.78% |
| core-mem | 0.47 W | 0.75 J | 3.29% |
| core-other | 1.03 W | 1.63 J | 7.16% |
| icache | 0.33 W | 0.52 J | 2.30% |
| dcache | 1.10 W | 1.74 J | 7.65% |
| l2 | 0.42 W | 0.67 J | 2.93% |
| l3 | 3.37 W | 5.34 J | 23.47% |
| dram | 4.26 W | 6.73 J | 29.60% |
| other | 0.03 W | 0.04 J | 0.18% |
| | | | |
| core | 4.87 W | 7.70 J | 33.88% |
| cache | 5.22 W | 8.26 J | 36.34% |
| total | 14.38 W | 22.74 J | 100.00% |

(a) 2 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.87 W | 2.11 J | 12.01% |
| core-ifetch | 0.50 W | 0.57 J | 3.24% |
| core-alu | 0.33 W | 0.38 J | 2.13% |
| core-int | 0.45 W | 0.51 J | 2.91% |
| core-fp | 0.87 W | 0.98 J | 5.57% |
| core-mem | 0.63 W | 0.71 J | 4.05% |
| core-other | 1.03 W | 1.16 J | 6.61% |
| icache | 0.38 W | 0.43 J | 2.43% |
| dcache | 1.43 W | 1.61 J | 9.16% |
| l2 | 0.42 W | 0.48 J | 2.71% |
| l3 | 3.37 W | 3.81 J | 21.67% |
| dram | 4.26 W | 4.81 J | 27.34% |
| other | 0.03 W | 0.03 J | 0.17% |
| | | | |
| core | 5.69 W | 6.43 J | 36.52% |
| cache | 5.60 W | 6.33 J | 35.98% |
| total | 15.57 W | 17.60 J | 100.00% |

(b) 4 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 2.22 W | 2.08 J | 13.50% |
| core-ifetch | 0.56 W | 0.52 J | 3.39% |
| core-alu | 0.34 W | 0.32 J | 2.07% |
| core-int | 0.49 W | 0.46 J | 2.98% |
| core-fp | 0.89 W | 0.84 J | 5.43% |
| core-mem | 0.74 W | 0.70 J | 4.53% |
| core-other | 1.03 W | 0.97 J | 6.27% |
| icache | 0.41 W | 0.39 J | 2.51% |
| dcache | 1.66 W | 1.56 J | 10.11% |
| l2 | 0.42 W | 0.40 J | 2.58% |
| l3 | 3.38 W | 3.17 J | 20.55% |
| dram | 4.26 W | 4.00 J | 25.92% |
| other | 0.03 W | 0.02 J | 0.16% |
| | | | |
| core | 6.27 W | 5.89 J | 38.17% |
| cache | 5.87 W | 5.51 J | 35.75% |
| total | 16.43 W | 15.42 J | 100.00% |

(c) 8 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 2.77 W | 2.05 J | 15.56% |
| core-ifetch | 0.64 W | 0.47 J | 3.60% |
| core-alu | 0.35 W | 0.26 J | 1.99% |
| core-int | 0.54 W | 0.40 J | 3.07% |
| core-fp | 0.93 W | 0.69 J | 5.25% |
| core-mem | 0.92 W | 0.68 J | 5.19% |
| core-other | 1.03 W | 0.76 J | 5.79% |
| icache | 0.47 W | 0.35 J | 2.62% |
| dcache | 2.03 W | 1.50 J | 11.42% |
| l2 | 0.43 W | 0.32 J | 2.40% |
| l3 | 3.38 W | 2.50 J | 19.00% |
| dram | 4.26 W | 3.16 J | 23.97% |
| other | 0.03 W | 0.02 J | 0.15% |
| | | | |
| core | 7.19 W | 5.33 J | 40.44% |
| cache | 6.30 W | 4.67 J | 35.44% |
| total | 17.77 W | 13.17 J | 100.00% |

(d) 16 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.04 W | 2.01 J | 19.33% |
| core-ifetch | 0.83 W | 0.41 J | 3.98% |
| core-alu | 0.38 W | 0.19 J | 1.84% |
| core-int | 0.67 W | 0.34 J | 3.23% |
| core-fp | 1.02 W | 0.51 J | 4.91% |
| core-mem | 1.33 W | 0.66 J | 6.39% |
| core-other | 1.03 W | 0.51 J | 4.93% |
| icache | 0.59 W | 0.29 J | 2.83% |
| dcache | 2.88 W | 1.44 J | 13.80% |
| l2 | 0.43 W | 0.21 J | 2.06% |
| l3 | 3.38 W | 1.68 J | 16.18% |
| dram | 4.26 W | 2.12 J | 20.41% |
| other | 0.03 W | 0.01 J | 0.12% |
| | | | |
| core | 9.31 W | 4.64 J | 44.60% |
| cache | 7.28 W | 3.63 J | 34.87% |
| total | 20.88 W | 10.41 J | 100.00% |

(e) 32 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.17 W | 2.01 J | 19.67% |
| core-ifetch | 0.85 W | 0.41 J | 4.01% |
| core-alu | 0.39 W | 0.19 J | 1.83% |
| core-int | 0.69 W | 0.33 J | 3.24% |
| core-fp | 1.03 W | 0.50 J | 4.87% |
| core-mem | 1.38 W | 0.66 J | 6.50% |
| core-other | 1.03 W | 0.50 J | 4.85% |
| icache | 0.60 W | 0.29 J | 2.85% |
| dcache | 2.98 W | 1.43 J | 14.02% |
| l2 | 0.43 W | 0.21 J | 2.03% |
| l3 | 3.38 W | 1.63 J | 15.92% |
| dram | 4.26 W | 2.05 J | 20.08% |
| other | 0.03 W | 0.01 J | 0.12% |
| | | | |
| core | 9.55 W | 4.59 J | 44.98% |
| cache | 7.39 W | 3.55 J | 34.82% |
| total | 21.22 W | 10.21 J | 100.00% |

(f) 48 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.18 W | 2.01 J | 19.68% |
| core-ifetch | 0.85 W | 0.41 J | 4.01% |
| core-alu | 0.39 W | 0.19 J | 1.83% |
| core-int | 0.69 W | 0.33 J | 3.24% |
| core-fp | 1.03 W | 0.50 J | 4.87% |
| core-mem | 1.38 W | 0.66 J | 6.50% |
| core-other | 1.03 W | 0.49 J | 4.85% |
| icache | 0.61 W | 0.29 J | 2.85% |
| dcache | 2.98 W | 1.43 J | 14.03% |
| l2 | 0.43 W | 0.21 J | 2.03% |
| l3 | 3.38 W | 1.62 J | 15.91% |
| dram | 4.26 W | 2.05 J | 20.07% |
| other | 0.03 W | 0.01 J | 0.12% |
| | | | |
| core | 9.55 W | 4.59 J | 44.99% |
| cache | 7.39 W | 3.55 J | 34.82% |
| total | 21.24 W | 10.20 J | 100.00% |

(g) 64 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.18 W | 2.01 J | 19.68% |
| core-ifetch | 0.85 W | 0.41 J | 4.01% |
| core-alu | 0.39 W | 0.19 J | 1.83% |
| core-int | 0.69 W | 0.33 J | 3.25% |
| core-fp | 1.04 W | 0.50 J | 4.87% |
| core-mem | 1.38 W | 0.66 J | 6.50% |
| core-other | 1.03 W | 0.49 J | 4.85% |
| icache | 0.61 W | 0.29 J | 2.85% |
| dcache | 2.98 W | 1.43 J | 14.03% |
| l2 | 0.43 W | 0.21 J | 2.03% |
| l3 | 3.38 W | 1.62 J | 15.91% |
| dram | 4.26 W | 2.05 J | 20.07% |
| other | 0.03 W | 0.01 J | 0.12% |
| | | | |
| core | 9.56 W | 4.59 J | 44.99% |
| cache | 7.39 W | 3.55 J | 34.82% |
| total | 21.24 W | 10.20 J | 100.00% |

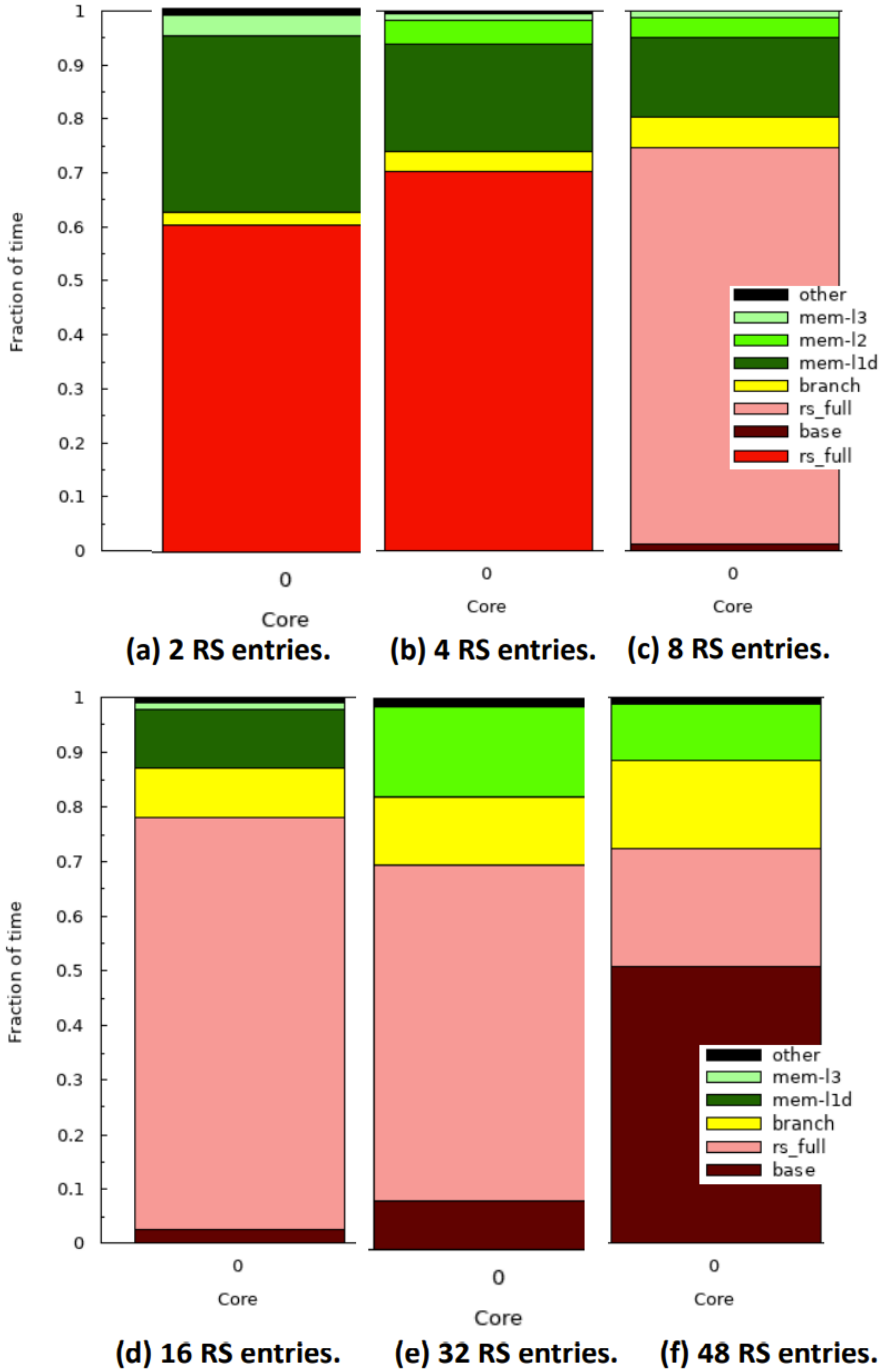
(h) 98 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.18 W | 2.01 J | 19.69% |
| core-ifetch | 0.85 W | 0.41 J | 4.01% |
| core-alu | 0.39 W | 0.19 J | 1.83% |
| core-int | 0.69 W | 0.33 J | 3.25% |
| core-fp | 1.04 W | 0.50 J | 4.87% |
| core-mem | 1.38 W | 0.66 J | 6.50% |
| core-other | 1.03 W | 0.49 J | 4.85% |
| icache | 0.61 W | 0.29 J | 2.85% |
| dcache | 2.98 W | 1.43 J | 14.03% |
| l2 | 0.43 W | 0.21 J | 2.03% |
| l3 | 3.38 W | 1.62 J | 15.91% |
| dram | 4.26 W | 2.05 J | 20.07% |
| other | 0.03 W | 0.01 J | 0.12% |
| | | | |
| core | 9.56 W | 4.59 J | 44.99% |
| cache | 7.39 W | 3.55 J | 34.82% |
| total | 21.24 W | 10.20 J | 100.00% |

(i) 128 RS entries.

Figure 17: Specific values for each components' power consumption.

### 6.3.2 CPI Stacks




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.

(d) 16 RS entries. (e) 32 RS entries. (f) 48 RS entries.

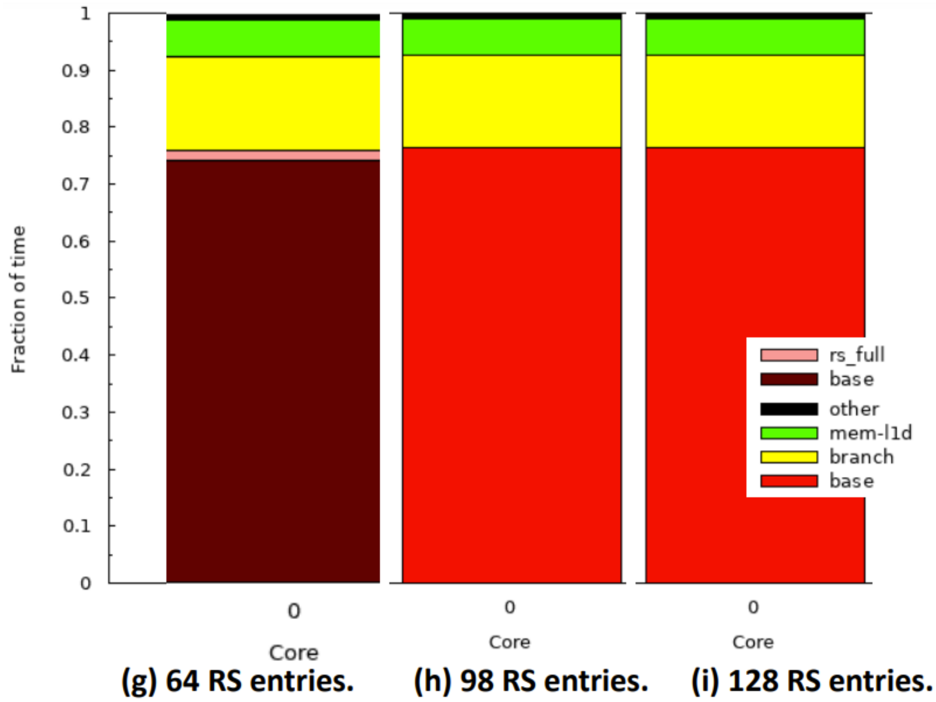



Figure 18: CPI stacks for various number of reservation station entries.

| | CPI | Time |
|---|---|---|
| rs_full | 1.54 | 60.18% |
| branch | 0.06 | 2.20% |
| mem-l1d | 0.84 | 32.70% |
| mem-l2 | 0.10 | 3.78% |
| other | 0.03 | 1.14% |
| | | |
| total | 2.56 | 100.00% |

(a) 2 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 1.29 | 70.32% |
| branch | 0.07 | 3.60% |
| mem-l1d | 0.36 | 19.93% |
| mem-l2 | 0.08 | 4.49% |
| mem-l3 | 0.02 | 1.04% |
| other | 0.01 | 0.61% |
| | | |
| total | 1.83 | 100.00% |

(b) 4 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.02 | 1.26% |
| rs_full | 1.12 | 73.35% |
| branch | 0.09 | 5.73% |
| mem-l1d | 0.23 | 14.85% |
| mem-l2 | 0.05 | 3.55% |
| mem-l3 | 0.02 | 1.15% |
| other | 0.00 | 0.11% |
| | | |
| total | 1.52 | 100.00% |

(c) 8 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.03 | 2.49% |
| rs_full | 0.91 | 75.64% |
| branch | 0.11 | 9.19% |
| mem-l1d | 0.13 | 10.57% |
| mem-l3 | 0.01 | 1.04% |
| other | 0.01 | 1.07% |
| | | |
| total | 1.20 | 100.00% |

(d) 16 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.07 | 8.94% |
| rs_full | 0.49 | 61.02% |
| branch | 0.10 | 12.39% |
| mem-l1d | 0.13 | 16.13% |
| other | 0.01 | 1.52% |
| | | |
| total | 0.81 | 100.00% |

(e) 32 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.40 | 50.84% |
| rs_full | 0.17 | 21.71% |
| branch | 0.12 | 16.01% |
| mem-l1d | 0.08 | 10.30% |
| other | 0.01 | 1.14% |
| | | |
| total | 0.78 | 100.00% |

(f) 48 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.58 | 74.41% |
| rs_full | 0.01 | 1.69% |
| branch | 0.13 | 16.34% |
| mem-l1d | 0.05 | 6.49% |
| other | 0.01 | 1.06% |
| | | |
| total | 0.78 | 100.00% |

(g) 64 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.59 | 76.30% |
| branch | 0.13 | 16.37% |
| mem-l1d | 0.05 | 6.36% |
| other | 0.01 | 0.97% |
| | | |
| total | 0.78 | 100.00% |

(h) 98 RS entries.

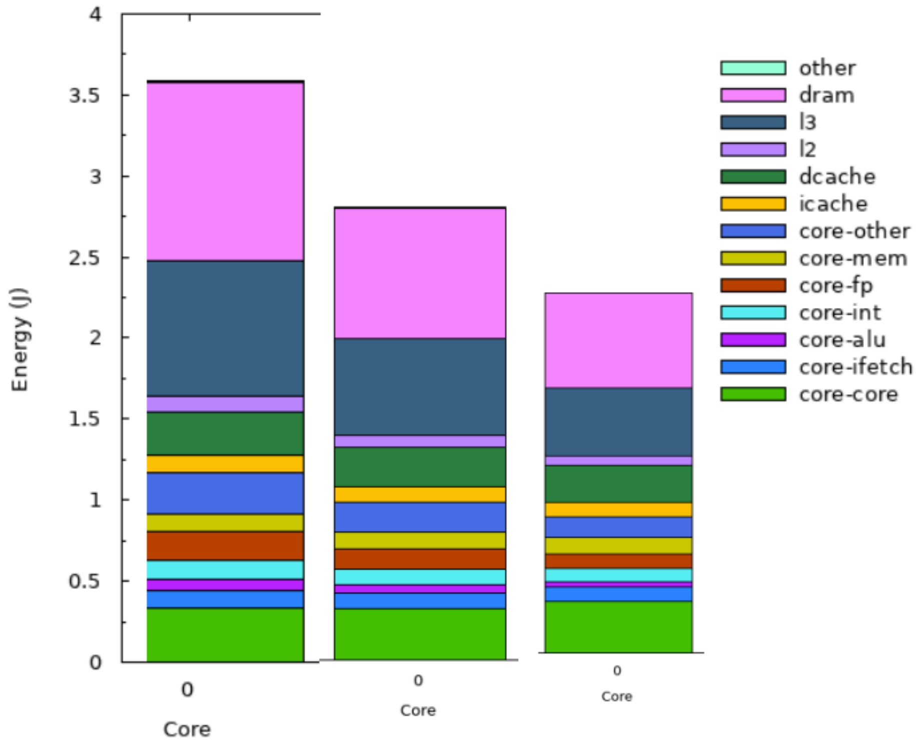
| | CPI | Time |
|---|---|---|
| base | 0.59 | 76.36% |
| branch | 0.13 | 16.37% |
| mem-l1d | 0.05 | 6.33% |
| other | 0.01 | 0.93% |
| | | |
| total | 0.78 | 100.00% |

(i) 128 RS entries.

Figure 19: Specific values for each components' CPI stack.

## 6.4 npb-is

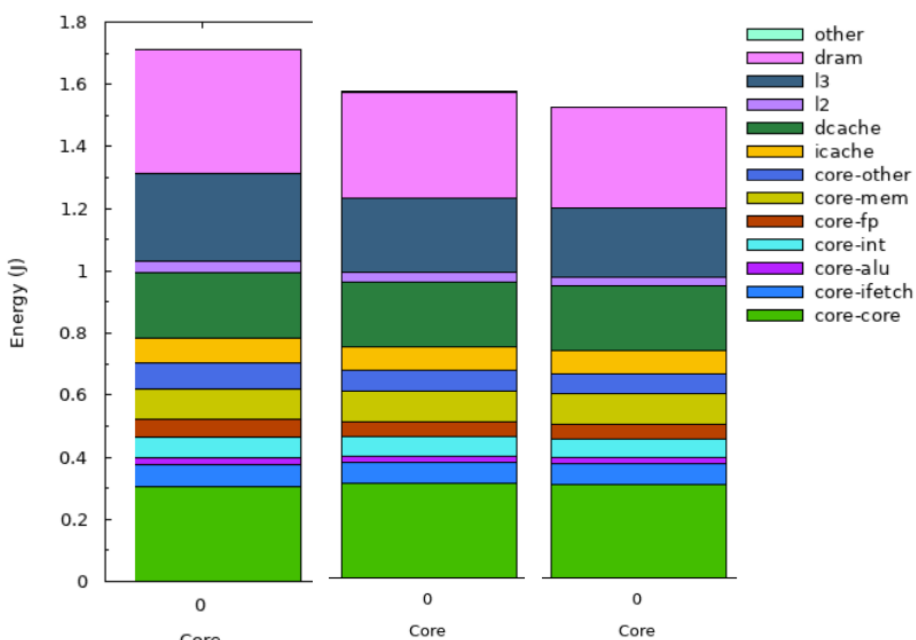
### 6.4.1 Power Results




(a) 2 RS entries.

(c) 8 RS entries.

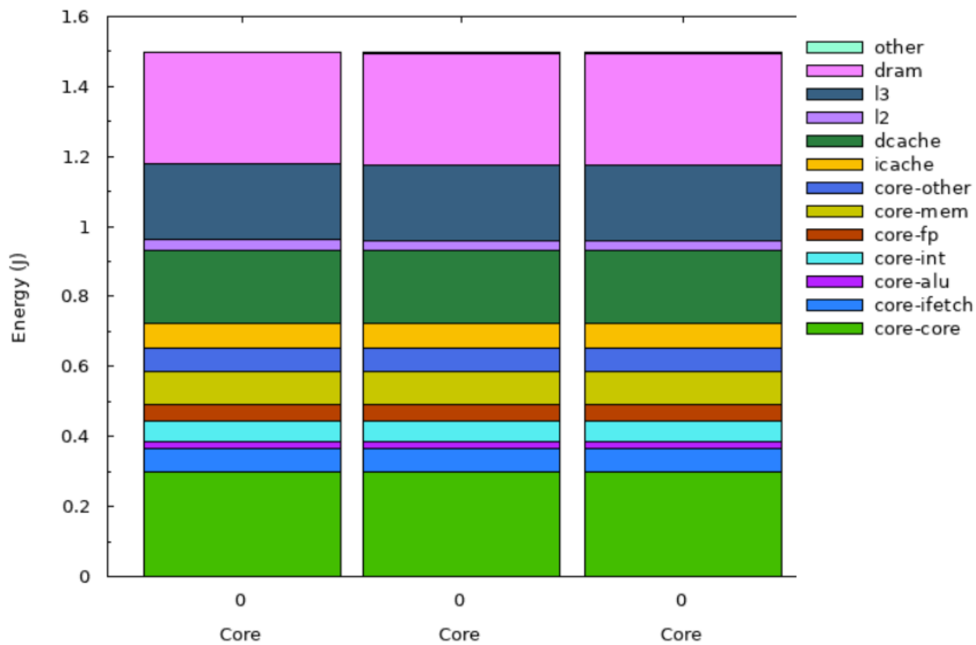
(b) 4 RS entries.




(d) 16 RS entries.

(f) 48 RS entries.

(e) 32 RS entries.




**(g) 64 RS entries.** **(h) 98 RS entries.** **(i) 128 RS entries.**

Figure 20: Processor power for various number of reservation station entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.34 W | 0.33 J | 9.21% |
| core-ifetch | 0.45 W | 0.11 J | 3.11% |
| core-alu | 0.29 W | 0.07 J | 2.00% |
| core-int | 0.45 W | 0.11 J | 3.11% |
| core-fp | 0.74 W | 0.18 J | 5.09% |
| core-mem | 0.45 W | 0.11 J | 3.07% |
| core-other | 1.03 W | 0.25 J | 7.05% |
| icache | 0.45 W | 0.11 J | 3.09% |
| dcache | 1.06 W | 0.26 J | 7.23% |
| l2 | 0.43 W | 0.11 J | 2.95% |
| l3 | 3.40 W | 0.83 J | 23.27% |
| dram | 4.48 W | 1.10 J | 30.65% |
| other | 0.03 W | 6.37 mJ | 0.18% |
| | | | |
| core | 4.76 W | 1.17 J | 32.63% |
| cache | 5.34 W | 1.31 J | 36.54% |
| total | 14.60 W | 3.58 J | 100.00% |

(a) 2 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.81 W | 0.32 J | 11.42% |
| core-ifetch | 0.54 W | 0.09 J | 3.38% |
| core-alu | 0.29 W | 0.05 J | 1.84% |
| core-int | 0.52 W | 0.09 J | 3.30% |
| core-fp | 0.74 W | 0.13 J | 4.68% |
| core-mem | 0.59 W | 0.10 J | 3.75% |
| core-other | 1.03 W | 0.18 J | 6.48% |
| icache | 0.55 W | 0.10 J | 3.44% |
| dcache | 1.36 W | 0.24 J | 8.59% |
| l2 | 0.44 W | 0.08 J | 2.75% |
| l3 | 3.41 W | 0.60 J | 21.47% |
| dram | 4.57 W | 0.80 J | 28.75% |
| other | 0.03 W | 4.56 mJ | 0.16% |
| | | | |
| core | 5.53 W | 0.97 J | 34.84% |
| cache | 5.76 W | 1.01 J | 36.25% |
| total | 15.88 W | 2.79 J | 100.00% |

(b) 4 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 2.60 W | 0.31 J | 14.44% |
| core-ifetch | 0.68 W | 0.08 J | 3.75% |
| core-alu | 0.29 W | 0.03 J | 1.62% |
| core-int | 0.64 W | 0.08 J | 3.55% |
| core-fp | 0.74 W | 0.09 J | 4.12% |
| core-mem | 0.84 W | 0.10 J | 4.67% |
| core-other | 1.03 W | 0.12 J | 5.71% |
| icache | 0.71 W | 0.08 J | 3.92% |
| dcache | 1.88 W | 0.22 J | 10.44% |
| l2 | 0.45 W | 0.05 J | 2.48% |
| l3 | 3.43 W | 0.41 J | 19.02% |
| dram | 4.71 W | 0.56 J | 26.14% |
| other | 0.03 W | 3.09 mJ | 0.14% |
| | | | |
| core | 6.82 W | 0.81 J | 37.86% |
| cache | 6.46 W | 0.77 J | 35.86% |
| total | 18.02 W | 2.15 J | 100.00% |

(c) 8 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 3.74 W | 0.30 J | 17.72% |
| core-ifetch | 0.88 W | 0.07 J | 4.15% |
| core-alu | 0.29 W | 0.02 J | 1.38% |
| core-int | 0.81 W | 0.07 J | 3.83% |
| core-fp | 0.74 W | 0.06 J | 3.51% |
| core-mem | 1.20 W | 0.10 J | 5.68% |
| core-other | 1.03 W | 0.08 J | 4.87% |
| icache | 0.94 W | 0.08 J | 4.44% |
| dcache | 2.63 W | 0.21 J | 12.46% |
| l2 | 0.46 W | 0.04 J | 2.18% |
| l3 | 3.45 W | 0.28 J | 16.33% |
| dram | 4.93 W | 0.40 J | 23.33% |
| other | 0.03 W | 2.10 mJ | 0.12% |
| | | | |
| core | 8.69 W | 0.70 J | 41.14% |
| cache | 7.48 W | 0.61 J | 35.41% |
| total | 21.14 W | 1.71 J | 100.00% |

(d) 16 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.48 W | 0.30 J | 19.36% |
| core-ifetch | 1.01 W | 0.07 J | 4.35% |
| core-alu | 0.29 W | 0.02 J | 1.26% |
| core-int | 0.92 W | 0.06 J | 3.97% |
| core-fp | 0.74 W | 0.05 J | 3.21% |
| core-mem | 1.43 W | 0.10 J | 6.18% |
| core-other | 1.03 W | 0.07 J | 4.45% |
| icache | 1.09 W | 0.07 J | 4.70% |
| dcache | 3.12 W | 0.21 J | 13.47% |
| l2 | 0.47 W | 0.03 J | 2.03% |
| l3 | 3.47 W | 0.23 J | 14.98% |
| dram | 5.08 W | 0.34 J | 21.93% |
| other | 0.03 W | 1.74 mJ | 0.11% |
| | | | |
| core | 9.90 W | 0.67 J | 42.78% |
| cache | 8.14 W | 0.55 J | 35.18% |
| total | 23.14 W | 1.56 J | 100.00% |

(e) 32 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.77 W | 0.30 J | 19.94% |
| core-ifetch | 1.06 W | 0.07 J | 4.42% |
| core-alu | 0.29 W | 0.02 J | 1.22% |
| core-int | 0.96 W | 0.06 J | 4.02% |
| core-fp | 0.74 W | 0.05 J | 3.10% |
| core-mem | 1.52 W | 0.10 J | 6.36% |
| core-other | 1.03 W | 0.06 J | 4.30% |
| icache | 1.15 W | 0.07 J | 4.80% |
| dcache | 3.31 W | 0.21 J | 13.82% |
| l2 | 0.47 W | 0.03 J | 1.98% |
| l3 | 3.47 W | 0.22 J | 14.52% |
| dram | 5.13 W | 0.32 J | 21.42% |
| other | 0.03 W | 1.63 mJ | 0.11% |
| | | | |
| core | 10.38 W | 0.65 J | 43.36% |
| cache | 8.40 W | 0.53 J | 35.11% |
| total | 23.93 W | 1.51 J | 100.00% |

(f) 48 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.83 W | 0.30 J | 20.04% |
| core-ifetch | 1.07 W | 0.07 J | 4.43% |
| core-alu | 0.29 W | 0.02 J | 1.21% |
| core-int | 0.97 W | 0.06 J | 4.03% |
| core-fp | 0.74 W | 0.05 J | 3.08% |
| core-mem | 1.54 W | 0.10 J | 6.39% |
| core-other | 1.03 W | 0.06 J | 4.27% |
| icache | 1.16 W | 0.07 J | 4.81% |
| dcache | 3.34 W | 0.21 J | 13.89% |
| l2 | 0.47 W | 0.03 J | 1.97% |
| l3 | 3.48 W | 0.22 J | 14.43% |
| dram | 5.14 W | 0.32 J | 21.34% |
| other | 0.03 W | 1.62 mJ | 0.11% |
| | | | |
| core | 10.47 W | 0.65 J | 43.46% |
| cache | 8.45 W | 0.53 J | 35.09% |
| total | 24.09 W | 1.50 J | 100.00% |

(g) 64 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.84 W | 0.30 J | 20.07% |
| core-ifetch | 1.07 W | 0.07 J | 4.43% |
| core-alu | 0.29 W | 0.02 J | 1.21% |
| core-int | 0.97 W | 0.06 J | 4.03% |
| core-fp | 0.74 W | 0.05 J | 3.08% |
| core-mem | 1.54 W | 0.10 J | 6.40% |
| core-other | 1.03 W | 0.06 J | 4.27% |
| icache | 1.16 W | 0.07 J | 4.82% |
| dcache | 3.35 W | 0.21 J | 13.90% |
| l2 | 0.47 W | 0.03 J | 1.96% |
| l3 | 3.48 W | 0.22 J | 14.41% |
| dram | 5.14 W | 0.32 J | 21.30% |
| other | 0.03 W | 1.61 mJ | 0.11% |
| | | | |
| core | 10.49 W | 0.65 J | 43.49% |
| cache | 8.46 W | 0.53 J | 35.10% |
| total | 24.12 W | 1.50 J | 100.00% |

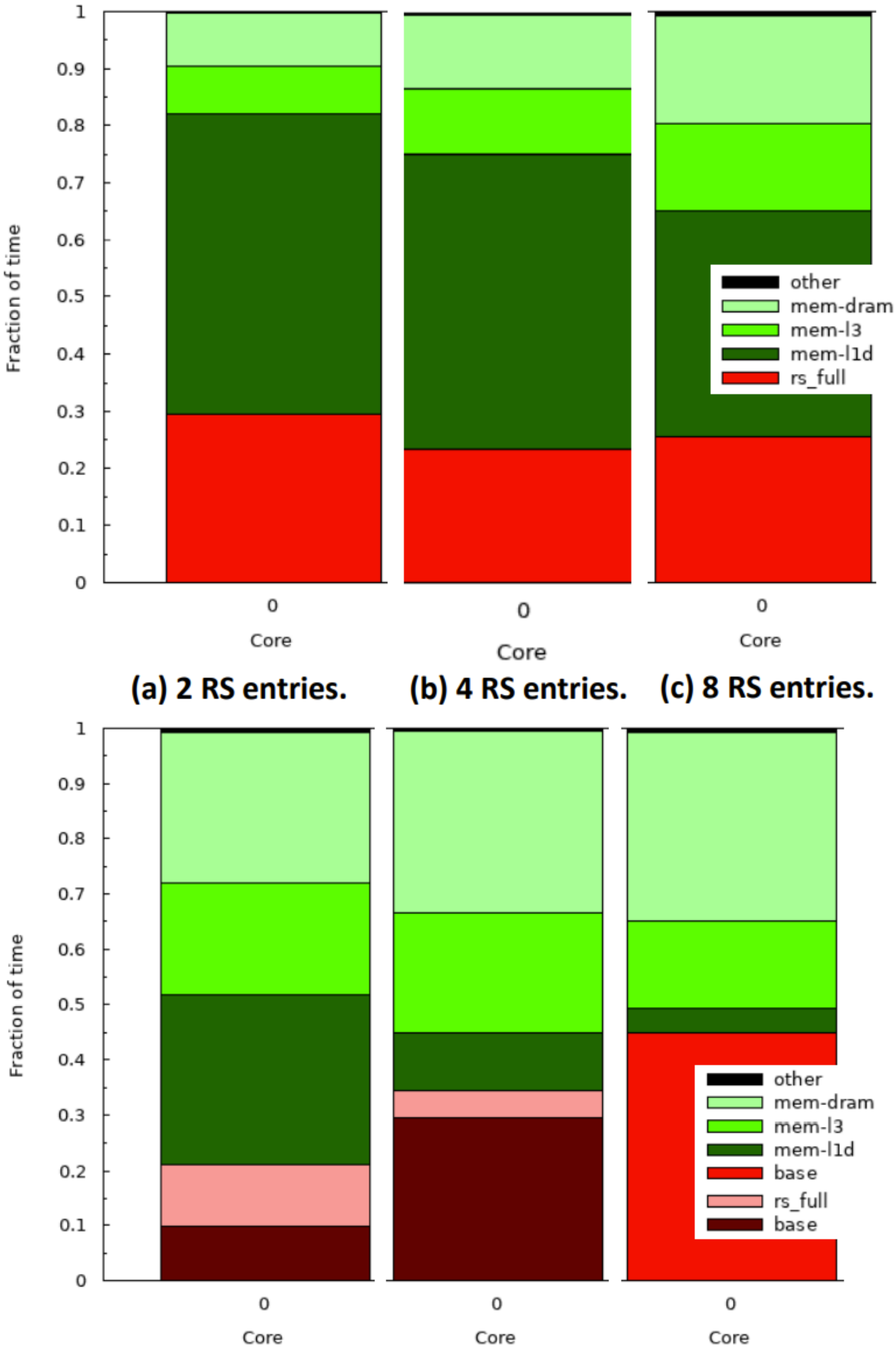
(h) 98 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.85 W | 0.30 J | 20.08% |
| core-ifetch | 1.07 W | 0.07 J | 4.44% |
| core-alu | 0.29 W | 0.02 J | 1.21% |
| core-int | 0.97 W | 0.06 J | 4.03% |
| core-fp | 0.74 W | 0.05 J | 3.08% |
| core-mem | 1.55 W | 0.10 J | 6.41% |
| core-other | 1.03 W | 0.06 J | 4.27% |
| icache | 1.16 W | 0.07 J | 4.82% |
| dcache | 3.36 W | 0.21 J | 13.91% |
| l2 | 0.47 W | 0.03 J | 1.96% |
| l3 | 3.48 W | 0.22 J | 14.41% |
| dram | 5.13 W | 0.32 J | 21.28% |
| other | 0.03 W | 1.61 mJ | 0.11% |
| | | | |
| core | 10.50 W | 0.65 J | 43.51% |
| cache | 8.47 W | 0.53 J | 35.10% |
| total | 24.13 W | 1.50 J | 100.00% |

(i) 128 RS entries.

Figure 21: Specific values for each components' power consumption.

### 6.4.2 CPI Stacks




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.

(d) 16 RS entries. (e) 32 RS entries. (f) 48 RS entries.

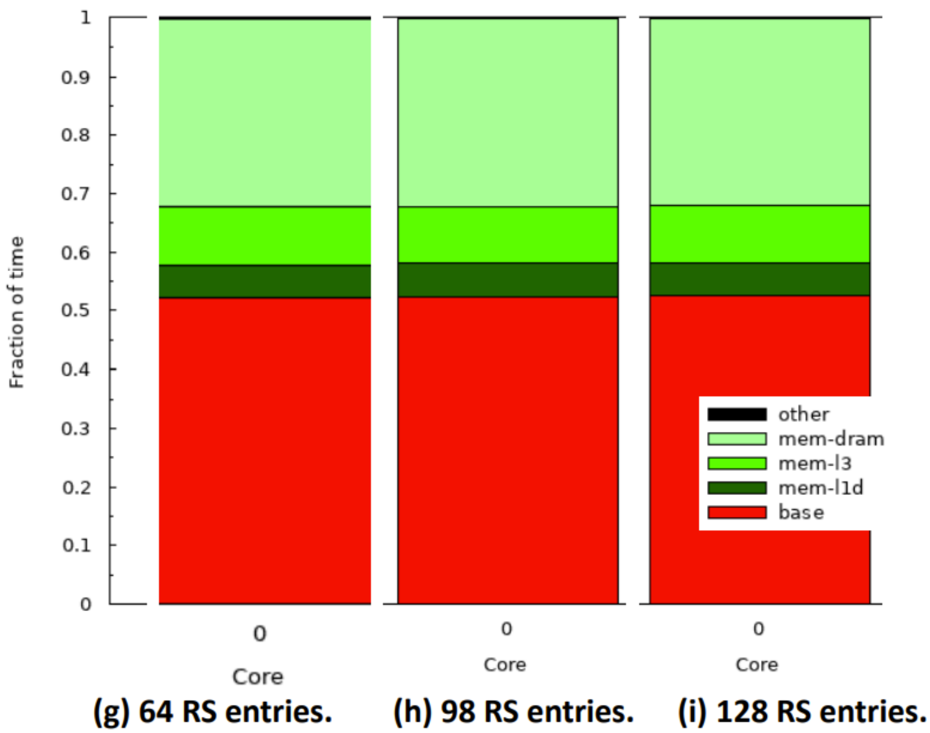



Figure 22: CPI stacks for various number of reservation station entries.

| | CPI | Time |
|---|---|---|
| rs_full | 0.67 | 29.44% |
| mem-l1d | 1.19 | 52.57% |
| mem-l3 | 0.19 | 8.30% |
| mem-dram | 0.21 | 9.44% |
| other | 0.01 | 0.24% |
| | | |
| total | 2.27 | 100.00% |

(a) 2 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 0.38 | 23.16% |
| mem-l1d | 0.85 | 52.09% |
| mem-l3 | 0.18 | 11.32% |
| mem-dram | 0.21 | 13.12% |
| other | 0.01 | 0.31% |
| | | |
| total | 1.63 | 100.00% |

(b) 4 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 0.28 | 25.46% |
| mem-l1d | 0.44 | 39.60% |
| mem-l3 | 0.17 | 15.29% |
| mem-dram | 0.21 | 18.91% |
| other | 0.01 | 0.73% |
| total | 1.10 | 100.00% |

(c) 8 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.07 | 9.94% |
| rs_full | 0.08 | 11.27% |
| mem-l1d | 0.23 | 30.60% |
| mem-l3 | 0.15 | 20.08% |
| mem-dram | 0.20 | 27.31% |
| other | 0.01 | 0.80% |
| total | 0.75 | 100.00% |

(d) 16 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.18 | 29.47% |
| rs_full | 0.03 | 4.86% |
| mem-l1d | 0.07 | 10.72% |
| mem-l3 | 0.13 | 21.64% |
| mem-dram | 0.20 | 32.72% |
| other | 0.00 | 0.59% |
| total | 0.62 | 100.00% |

(e) 32 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.26 | 44.97% |
| mem-l1d | 0.03 | 4.34% |
| mem-l3 | 0.09 | 15.80% |
| mem-dram | 0.20 | 34.07% |
| other | 0.00 | 0.82% |
| total | 0.58 | 100.00% |

(f) 48 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.30 | 52.18% |
| mem-l1d | 0.03 | 5.64% |
| mem-l3 | 0.06 | 9.88% |
| mem-dram | 0.18 | 31.90% |
| other | 0.00 | 0.39% |
| | | |
| total | 0.58 | 100.00% |

(g) 64 RS entries.

| | CPI | Time |
|---|---|---|
| base | 0.30 | 52.44% |
| mem-l1d | 0.03 | 5.69% |
| mem-l3 | 0.06 | 9.79% |
| mem-dram | 0.18 | 31.71% |
| other | 0.00 | 0.37% |
| | | |
| total | 0.57 | 100.00% |

(h) 98 RS entries.

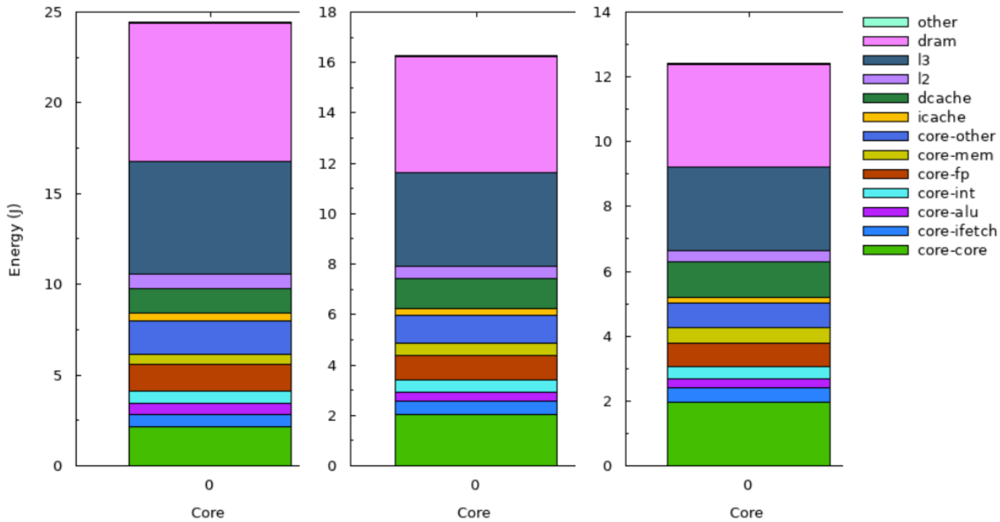
| | CPI | Time |
|---|---|---|
| base | 0.30 | 52.51% |
| mem-l1d | 0.03 | 5.70% |
| mem-l3 | 0.06 | 9.82% |
| mem-dram | 0.18 | 31.61% |
| other | 0.00 | 0.36% |
| | | |
| total | 0.57 | 100.00% |

(i) 128 RS entries.

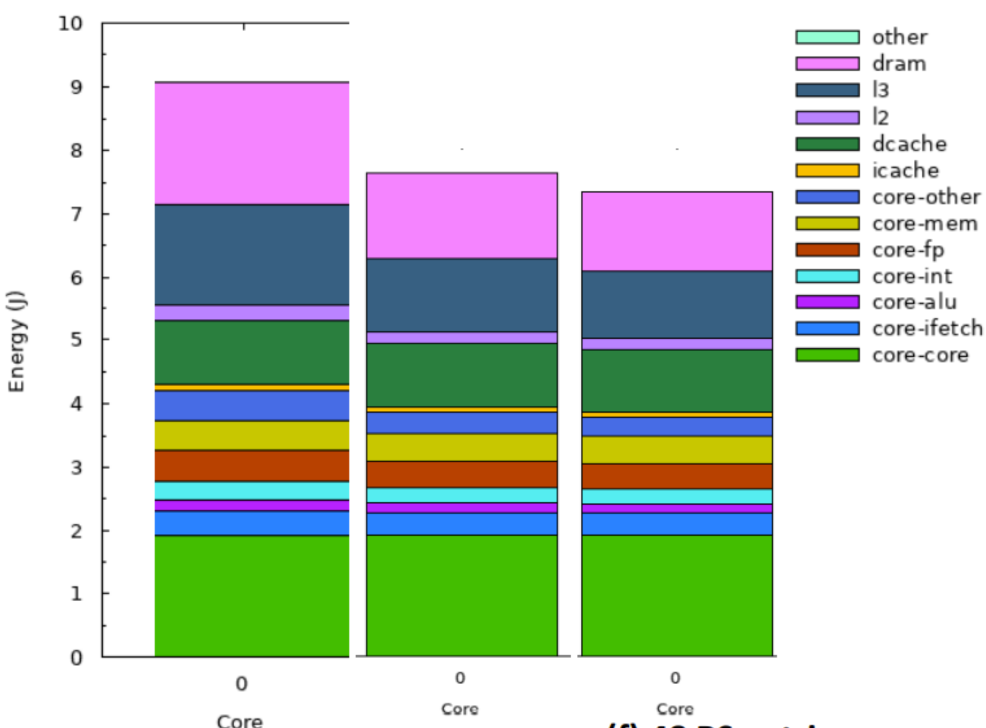
Figure 23: Specific values for each components' CPI stack.

## 6.5 npb-cg

### 6.5.1 Power Results

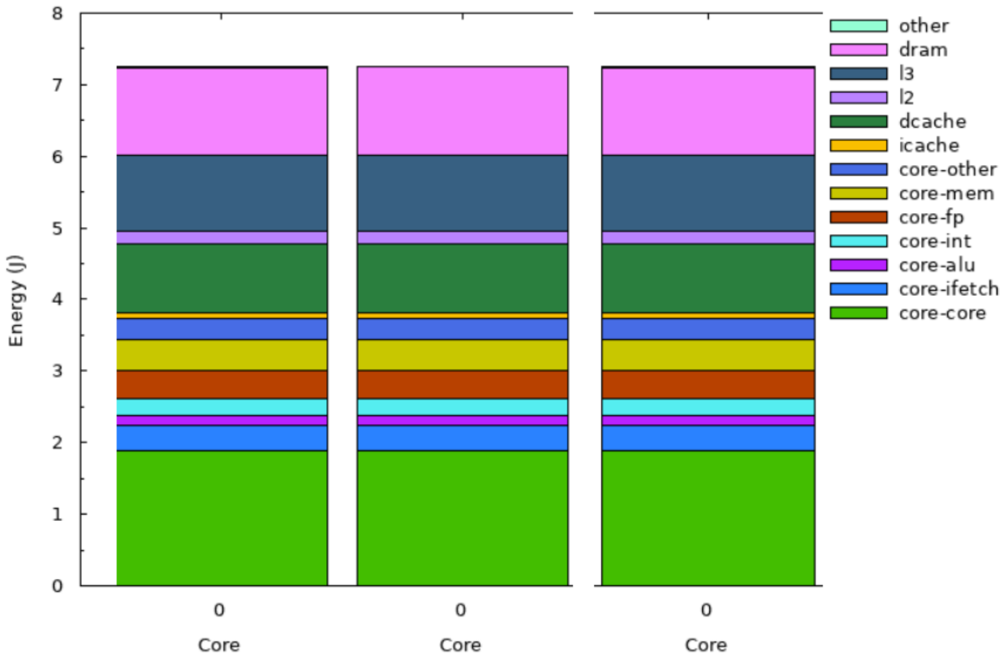



(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.




(d) 16 RS entries. (f) 48 RS entries.

(e) 32 RS entries.



**(g) 64 RS entries.** **(h) 98 RS entries.** **(i) 128 RS entries.**

Figure 24: Processor power for various number of reservation station entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.19 W | 2.13 J | 8.74% |
| core-ifetch | 0.40 W | 0.72 J | 2.93% |
| core-alu | 0.32 W | 0.58 J | 2.38% |
| core-int | 0.36 W | 0.65 J | 2.68% |
| core-fp | 0.84 W | 1.51 J | 6.19% |
| core-mem | 0.31 W | 0.55 J | 2.26% |
| core-other | 1.03 W | 1.85 J | 7.57% |
| icache | 0.22 W | 0.39 J | 1.61% |
| dcache | 0.77 W | 1.39 J | 5.70% |
| l2 | 0.44 W | 0.79 J | 3.25% |
| l3 | 3.43 W | 6.16 J | 25.21% |
| dram | 4.25 W | 7.64 J | 31.29% |
| other | 0.03 W | 0.05 J | 0.19% |
| | | | |
| core | 4.45 W | 8.00 J | 32.76% |
| cache | 4.86 W | 8.74 J | 35.77% |
| total | 13.59 W | 24.43 J | 100.00% |

(a) 2 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 1.87 W | 2.02 J | 12.41% |
| core-ifetch | 0.50 W | 0.54 J | 3.32% |
| core-alu | 0.35 W | 0.37 J | 2.30% |
| core-int | 0.42 W | 0.45 J | 2.79% |
| core-fp | 0.91 W | 0.98 J | 6.02% |
| core-mem | 0.46 W | 0.50 J | 3.06% |
| core-other | 1.03 W | 1.11 J | 6.84% |
| icache | 0.22 W | 0.24 J | 1.49% |
| dcache | 1.10 W | 1.19 J | 7.33% |
| l2 | 0.46 W | 0.49 J | 3.04% |
| l3 | 3.46 W | 3.74 J | 22.99% |
| dram | 4.25 W | 4.59 J | 28.24% |
| other | 0.03 W | 0.03 J | 0.17% |
| | | | |
| core | 5.53 W | 5.97 J | 36.73% |
| cache | 5.25 W | 5.67 J | 34.85% |
| total | 15.06 W | 16.26 J | 100.00% |

(b) 4 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 2.65 W | 1.96 J | 15.83% |
| core-ifetch | 0.62 W | 0.46 J | 3.68% |
| core-alu | 0.37 W | 0.27 J | 2.21% |
| core-int | 0.49 W | 0.36 J | 2.90% |
| core-fp | 0.98 W | 0.73 J | 5.86% |
| core-mem | 0.64 W | 0.47 J | 3.80% |
| core-other | 1.03 W | 0.76 J | 6.15% |
| icache | 0.23 W | 0.17 J | 1.38% |
| dcache | 1.48 W | 1.10 J | 8.85% |
| l2 | 0.48 W | 0.35 J | 2.85% |
| l3 | 3.50 W | 2.60 J | 20.93% |
| dram | 4.25 W | 3.15 J | 25.40% |
| other | 0.03 W | 0.02 J | 0.16% |
| | | | |
| core | 6.77 W | 5.02 J | 40.44% |
| cache | 5.69 W | 4.22 J | 34.01% |
| total | 16.74 W | 12.40 J | 100.00% |

(c) 8 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 4.27 W | 1.92 J | 21.11% |
| core-ifetch | 0.86 W | 0.38 J | 4.24% |
| core-alu | 0.42 W | 0.19 J | 2.09% |
| core-int | 0.62 W | 0.28 J | 3.06% |
| core-fp | 1.14 W | 0.51 J | 5.61% |
| core-mem | 1.00 W | 0.45 J | 4.95% |
| core-other | 1.03 W | 0.46 J | 5.09% |
| icache | 0.24 W | 0.11 J | 1.21% |
| dcache | 2.26 W | 1.02 J | 11.20% |
| l2 | 0.52 W | 0.23 J | 2.55% |
| l3 | 3.59 W | 1.61 J | 17.74% |
| dram | 4.25 W | 1.91 J | 21.03% |
| other | 0.03 W | 0.01 J | 0.13% |
| | | | |
| core | 9.33 W | 4.19 J | 46.15% |
| cache | 6.61 W | 2.97 J | 32.70% |
| total | 20.22 W | 9.08 J | 100.00% |

(d) 16 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 6.01 W | 1.89 J | 25.07% |
| core-ifetch | 1.12 W | 0.35 J | 4.65% |
| core-alu | 0.48 W | 0.15 J | 1.99% |
| core-int | 0.76 W | 0.24 J | 3.19% |
| core-fp | 1.30 W | 0.41 J | 5.43% |
| core-mem | 1.39 W | 0.44 J | 5.81% |
| core-other | 1.03 W | 0.32 J | 4.29% |
| icache | 0.26 W | 0.08 J | 1.08% |
| dcache | 3.11 W | 0.98 J | 12.96% |
| l2 | 0.56 W | 0.18 J | 2.33% |
| l3 | 3.68 W | 1.16 J | 15.35% |
| dram | 4.25 W | 1.34 J | 17.74% |
| other | 0.03 W | 8.18 mJ | 0.11% |
| | | | |
| core | 12.09 W | 3.81 J | 50.43% |
| cache | 7.60 W | 2.40 J | 31.72% |
| total | 23.97 W | 7.56 J | 100.00% |

(e) 32 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 6.55 W | 1.89 J | 26.07% |
| core-ifetch | 1.20 W | 0.35 J | 4.76% |
| core-alu | 0.50 W | 0.14 J | 1.97% |
| core-int | 0.81 W | 0.23 J | 3.22% |
| core-fp | 1.35 W | 0.39 J | 5.38% |
| core-mem | 1.51 W | 0.44 J | 6.02% |
| core-other | 1.03 W | 0.30 J | 4.09% |
| icache | 0.26 W | 0.08 J | 1.05% |
| dcache | 3.37 W | 0.97 J | 13.40% |
| l2 | 0.57 W | 0.16 J | 2.27% |
| l3 | 3.71 W | 1.07 J | 14.75% |
| dram | 4.25 W | 1.23 J | 16.91% |
| other | 0.03 W | 7.48 mJ | 0.10% |
| | | | |
| core | 12.95 W | 3.74 J | 51.51% |
| cache | 7.91 W | 2.28 J | 31.47% |
| total | 25.14 W | 7.25 J | 100.00% |

(f) 48 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 6.56 W | 1.89 J | 26.07% |
| core-ifetch | 1.20 W | 0.34 J | 4.76% |
| core-alu | 0.50 W | 0.14 J | 1.97% |
| core-int | 0.81 W | 0.23 J | 3.22% |
| core-fp | 1.35 W | 0.39 J | 5.38% |
| core-mem | 1.51 W | 0.44 J | 6.02% |
| core-other | 1.03 W | 0.30 J | 4.09% |
| icache | 0.26 W | 0.08 J | 1.05% |
| dcache | 3.37 W | 0.97 J | 13.40% |
| l2 | 0.57 W | 0.16 J | 2.27% |
| l3 | 3.71 W | 1.07 J | 14.75% |
| dram | 4.25 W | 1.23 J | 16.91% |
| other | 0.03 W | 7.48 mJ | 0.10% |
| | | | |
| core | 12.96 W | 3.74 J | 51.52% |
| cache | 7.91 W | 2.28 J | 31.47% |
| total | 25.15 W | 7.25 J | 100.00% |

(g) 64 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 6.56 W | 1.89 J | 26.07% |
| core-ifetch | 1.20 W | 0.34 J | 4.76% |
| core-alu | 0.50 W | 0.14 J | 1.97% |
| core-int | 0.81 W | 0.23 J | 3.22% |
| core-fp | 1.35 W | 0.39 J | 5.38% |
| core-mem | 1.51 W | 0.44 J | 6.02% |
| core-other | 1.03 W | 0.30 J | 4.09% |
| icache | 0.26 W | 0.08 J | 1.05% |
| dcache | 3.37 W | 0.97 J | 13.40% |
| l2 | 0.57 W | 0.16 J | 2.27% |
| l3 | 3.71 W | 1.07 J | 14.75% |
| dram | 4.25 W | 1.23 J | 16.91% |
| other | 0.03 W | 7.48 mJ | 0.10% |
| | | | |
| core | 12.96 W | 3.74 J | 51.52% |
| cache | 7.91 W | 2.28 J | 31.47% |
| total | 25.15 W | 7.25 J | 100.00% |

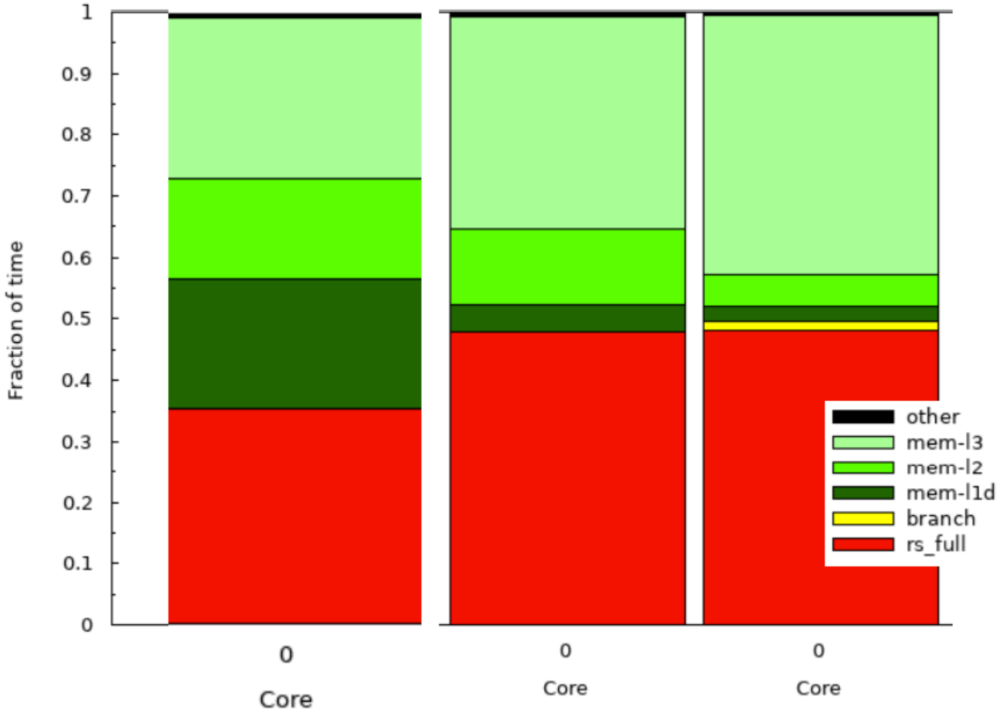
(h) 98 RS entries.

| | Power | Energy | Energy % |
|---|---|---|---|
| core-core | 6.56 W | 1.89 J | 26.07% |
| core-ifetch | 1.20 W | 0.34 J | 4.76% |
| core-alu | 0.50 W | 0.14 J | 1.97% |
| core-int | 0.81 W | 0.23 J | 3.22% |
| core-fp | 1.35 W | 0.39 J | 5.38% |
| core-mem | 1.51 W | 0.44 J | 6.02% |
| core-other | 1.03 W | 0.30 J | 4.09% |
| icache | 0.26 W | 0.08 J | 1.05% |
| dcache | 3.37 W | 0.97 J | 13.40% |
| l2 | 0.57 W | 0.16 J | 2.27% |
| l3 | 3.71 W | 1.07 J | 14.75% |
| dram | 4.25 W | 1.23 J | 16.91% |
| other | 0.03 W | 7.48 mJ | 0.10% |
| | | | |
| core | 12.96 W | 3.74 J | 51.52% |
| cache | 7.91 W | 2.28 J | 31.47% |
| total | 25.15 W | 7.25 J | 100.00% |

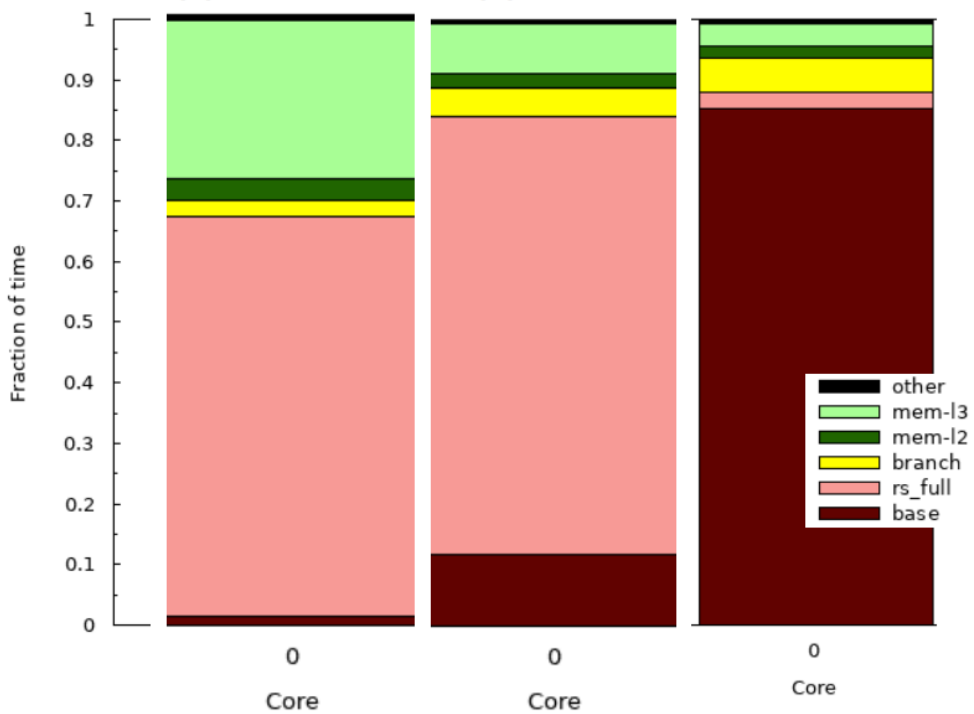
(i) 128 RS entries.

Figure 25: Specific values for each components' power consumption.

### 6.5.2 CPI Stacks




(a) 2 RS entries. (b) 4 RS entries. (c) 8 RS entries.




(d) 16 RS entries. (e) 32 RS entries. (f) 48 RS entries.

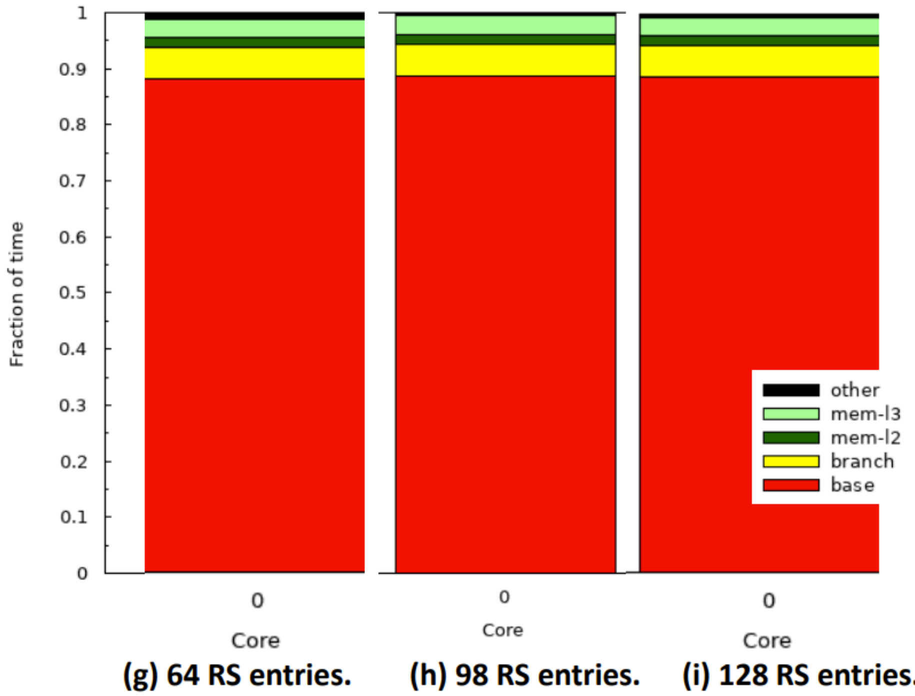



Figure 26: CPI stacks for various number of reservation station entries.

| | CPI | Time |
|---|---|---|
| rs_full | 1.11 | 35.38% |
| mem-l1d | 0.66 | 21.16% |
| mem-l2 | 0.51 | 16.22% |
| mem-l3 | 0.83 | 26.56% |
| other | 0.02 | 0.68% |
| | | |
| total | 3.14 | 100.00% |

(a) 2 RS entries.

| | CPI | Time |
|---|---|---|
| rs_full | 0.91 | 47.98% |
| mem-l1d | 0.08 | 4.28% |
| mem-l2 | 0.23 | 12.43% |
| mem-l3 | 0.65 | 34.46% |
| other | 0.02 | 0.85% |
| | | |
| total | 1.89 | 100.00% |

(b) 4 RS entries.

```
                    CPI      Time
rs_full             0.62    48.24%
branch              0.02     1.32%
mem-l1d             0.03     2.48%
mem-l2              0.07     5.29%
mem-l3              0.55    42.22%
other               0.01     0.44%

total               1.29   100.00%
```

(c) 8 RS entries.

```
                    CPI      Time
base                0.01     1.52%
rs_full             0.51    65.46%
branch              0.02     2.61%
mem-l2              0.03     3.42%
mem-l3              0.20    26.06%
other               0.01     0.92%

total               0.78   100.00%
```

(d) 16 RS entries.

```
                    CPI      Time
base                0.06    11.66%
rs_full             0.40    72.45%
branch              0.03     4.73%
mem-l2              0.01     2.14%
mem-l3              0.05     8.32%
other               0.00     0.70%

total               0.55   100.00%
```

(e) 32 RS entries.

```
                    CPI      Time
base                0.43    85.30%
rs_full             0.01     2.62%
branch              0.03     5.61%
mem-l2              0.01     2.07%
mem-l3              0.02     3.72%
other               0.00     0.69%

total               0.50   100.00%
```

(f) 48 RS entries.

```
                    CPI      Time
base                0.44    88.11%
branch              0.03     5.62%
mem-l2              0.01     1.86%
mem-l3              0.02     3.26%
other               0.01     1.14%

total               0.50   100.00%
```

(g) 64 RS entries.

```
                    CPI      Time
base                0.45    88.67%
branch              0.03     5.62%
mem-l2              0.01     1.86%
mem-l3              0.02     3.26%
other               0.00     0.58%

total               0.50   100.00%
```

(h) 98 RS entries.

```
                    CPI      Time
base                0.45    88.68%
branch              0.03     5.62%
mem-l2              0.01     1.86%
mem-l3              0.02     3.26%
other               0.00     0.58%

total               0.50   100.00%
```

(i) 128 RS entries.

Figure 27: Specific values for each components' CPI stack.