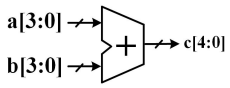
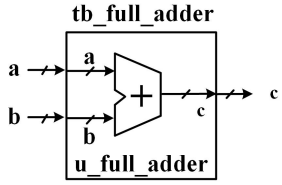
PBL 6: Four-bit Full-adder

1) Design a four-bit full adder using the arithmetic operator "+". Fig. 5.8(a) shows the design block diagram, including the four-bit input signals "a" and "b" and five-bit output "c".



(a) Design Block Diagram of four-bit Adder.



(b) Testbench of four-bit Adder.

FIGURE 5.8
Design and Simulation Specification of four-bit Adder.

2) Create a testbench to simulate the design using all possible input combinations of "a" and "b" in hexadecimal, from 4'h0 to 4'hf. There are 256 possible combinations, which can be fed into the design using a repeated loop in a bus functional model. Similarly, use a repeated loop in a monitor to check the results automatically.

The testbench shown in Fig. 5.8(b) connects the four-bit signals "a" and "b" to the design inputs, and the five-bit signal "c" to the design output to monitor the results.

PBL 7: Combinational Circuit Design and Simulation

1) Design a combinational circuit named "com_and_or" with an AND gate and two OR gates as shown in Fig 5.9. The module should have single-bit input and output signals.

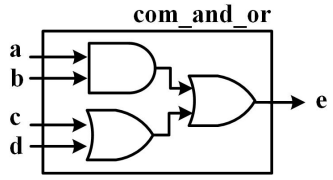


FIGURE 5.9
Combinational AND-OR Circuit.

2) Create a testbench to simulate the designed circuit using all possible input combinations of "a-d", totaling 16 combinations. You can use a repeated loop in a bus functional model to feed in all the data and in a monitor to automatically check the results.

PBL 8: Sequential Circuit Design and Simulation

1) Using the project in Fig. 5.9 as a submodule, design a sequential circuit that includes an instantiation of the submodule and a flip-flop, as shown in Fig 5.10. The name of the design module is "seq_and_or", and all the IOs are single-bit signals. The flip-flop can be triggered by a falling reset edge and a rising clock edge.

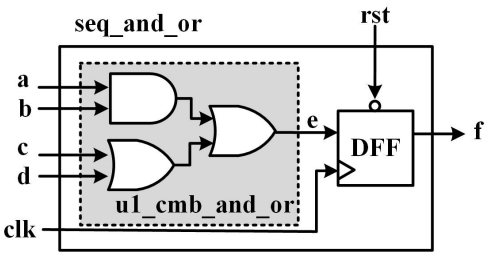


FIGURE 5.10
Sequential AND-OR Circuit.

2) Design a testbench to simulate the design with all possible combinations of the four inputs, "a" through "d". The testbench should include 16 possible input combinations. Use a repeated loop in a bus functional model to feed in all the data. Similarly, use a repeated loop in a monitor to automatically check the results. For the flip-flop simulation, you will need a clock and reset generator.

PBL 9: Sequential Circuit Instantiation and Simulation

1) Design a sequential circuit named "seq_inst_and_or" using the project shown in Fig. 5.9 as a submodule. The circuit should include two submodule instantiations, each consisting of a combinational AND-OR circuit, a single-bit adder, and three flip-flops as depicted in Fig 5.10. All inputs and outputs of the module should be single-bit signals. The flip-flops should be triggered by rising clock edges and falling reset edges.

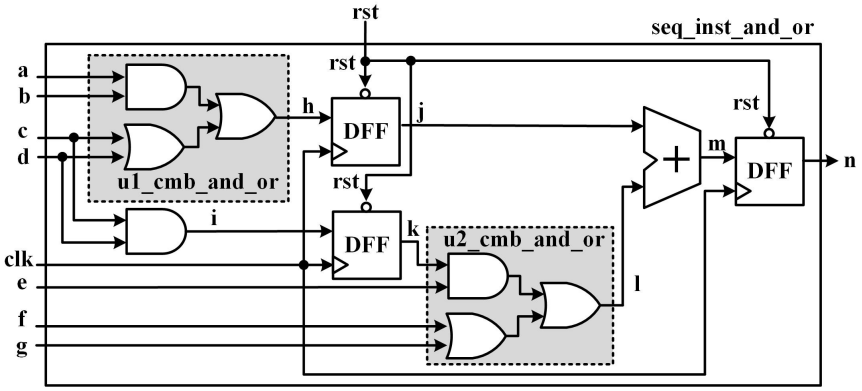


FIGURE 5.11
Sequential Circuit Instantiation.

2) Design a testbench to simulate the new design module with all the possible seven inputs "a-g". This should include $2^7 = 128$ possible combinations of inputs. Use a repeated loop in a bus functional model to feed in all the data. Similarly, you could use a repeated loop in a monitor to automatically check the results. To simulate the flip-flops, you will need a clock and reset generator.