PBL# 5 Report: SEQUENTIAL CIRCUIT DESIGN AND SIMULATION

Name: Ruben Ramirez

ID: 0432694

# Introduction

In this report, we will explore the creation of a sequential circuit according to the design in figure 1. Our design incorporates two submodules of an and or gate design, an adder, and three Flip-Flop register with a falling edge reset and rising edge clock signal. The circuit will be designed to feature single-bit input ports denoted as a, b, c, d,e,f, g an asynchronous reset signal rst, a clock signal clk, and an output f.

A diagram of a block diagram

Description automatically generated

Figure : Sequential Circuit Instantiation

# Verilog HDL Design Code

See attached files for verilog

# Simulation Waveform

# A screen shot of a computer screen Description automatically generated

Figure : Waveform of Design testbench

# Comments

This circuit behaved as expected with regards to the sequential circuit design in figure 1.