

# ECE 527 SoC Design Machine Problem 1

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## 1. INTRODUCTION

This MP was designed to become familiar with the Xilinx tools. We set up the development environment on a lightweight ubuntu distribution and interfaced with the ZedBoard. We walked through the compilation process as well as practiced incorporating the Zynq hard IP core into the design by generating a Board Support Package and writing software in the Xilinx SDK.

## 2. Part A

### 2.1. Description

For the first part of the MP we had to write a small verilog module for the programmable logic fabric portion of the Xilinx Zynq 7000 chip. This module needs to read the positions of the 8 on board switches and display the switch position on the 8 user LEDs. The switch status was displayed on the LEDs after 3 clock cycles and the center button was used as a reset.

### 2.2. Assumptions

We did not have to make any assumptions for this part of the MP as the directions were very straight forward.

### 2.3. System Configuration

The part A of the machine problem was very simple so we only needed one module in the programmable logic fabric. This module took in inputs from the switches, a single input from the reset button, and a clock. The module output a vector to the LEDs containing information on the switch state. The module contained three buffering registers to ensure that the switch state appeared on the LEDs after exactly 3 clock cycles. The module is shown in figure 1.

### 2.4. Entities

Entity	Description
basic_i_o	Hardware top level, contains pipeline

### 2.5. Design

When designing we only considered one solution. Using a pipeline to transfer switch state information to

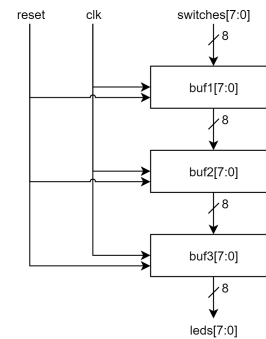


Figure 1. Block Diagram for Part A

the LEDs. This would ensure that the LEDs were updated with switch information after exactly 3 cycles for every change in the switches. Had we used a counter or other option it would have more complex logic and been harder to guarantee the LEDs were updated after 3 cycles.

### 2.6. Performance

This was a very small design and it took up very little resources on the Zynq 7000. The usage is shown in the table below. Figure 2 shows how the design was implemented on the device.

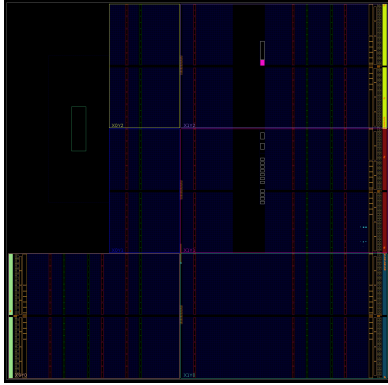
Table 1. Resource Usage Part A

Resource	Utilization	Available	Utilization %
LUT	1	53200	0.01
FF	24	106400	0.02
IO	18	200	9.00
BUFG	1	32	3.13

Because this design used minimal logic most of the power consumed by the device was static power. As the transistors were mostly sitting idle across the programmable logic fabric.

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**Figure 2. Device Mapping for Part A**

**Table 2. Resource Usage Part A**

Type	Power
Static	0.122 W
Dynamic	0.007 W
<b>Total</b>	<b>0.129 W</b>

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$$\alpha + \beta = \chi \quad (1)$$

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**Table 3. An Example of a Table**

One	Two
Three	Four



**Figure 3. Inductance of oscillation winding on amorphous magnetic core versus DC bias magnetic field**

Figure Labels: Use 8 point Times New Roman for Figure labels. Use words rather than symbols or abbreviations when writing Figure axis labels to avoid confusing the reader. As an example, write the quantity Magnetization, or Magnetization, M, not just M. If including units in the label, present them within parentheses. Do not label axes only with units. In the example, write Magnetization (A/m) or Magnetization A[m(1)], not just A/m. Do not label axes with a ratio of quantities and units. For example, write Temperature (K), not Temperature/K.

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## APPENDIX

Appendices should appear before the acknowledgment.

## ACKNOWLEDGMENT

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References are important to the reader; therefore, each citation must be complete and correct. If at all possible, references should be commonly available publications.

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