ECE 527 SoC Design Machine Problem 1

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1. INTRODUCTION

This MP was designed to become familiar with the Xilinx tools. We set up the development environment on a lightweight ubuntu distribution and interfaced with the ZedBoard. We walked through the compilation process as well as practiced incorporating the Zynq hard IP core into the design by generating a Board Support Package and writing software in the Xilinx SDK.

2. Part A

2.1. Description

For the first part of the MP we had to write a small verilog module for the programmable logic fabric portion of the Xilinx Zinq 7000 chip. This module needs to read the positions of the 8 on board switches and display the switch position on the 8 user LEDs. The switch status was displayed on the LEDs after 3 clock cycles and the center button was used as a reset.

2.2. Assumptions

We did not have to make any assumptions for this part of the MP as the directions were very straight forward.

2.3. System Configuration

The part A of the machine problem was very simple so we only needed one module in the programmable logic fabric. This module took in inputs from the switches, a single input from the reset button, and a clock. The module output a vector to the LEDs containing information on the switch state. The module contained three buffering registers to ensure that the switch state appeared on the LEDs after exactly 3 clock cycles. The module is shown in figure 1.

2.4. Entities

Entity	Description
basic_i_o	Hardware top level, contains pipeline

2.5. Design

When designing we only considered one solution. Using a pipeline to transfer switch state information to the LEDs. This would ensure that the LEDs were updated with switch information after exactly 3 cycles for every change in the switches. Had we used a counter or other option it would have more complex logic and been harder to guarantee the LEDs were updated after 3 cycles.

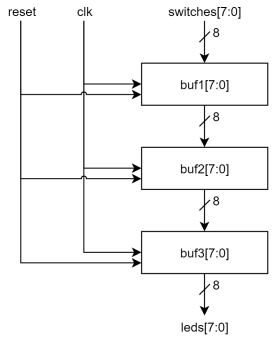

Figure 1. Block Diagram for Part A

2.6. Performance

This was a very small design and it took up very little resources on the Zinq 7000. The usage is shown in the table below. Figure 2 shows how the design was implemented on the device.

Table 1. Resource Usage Part A

Resource	Utilization	Available	Utilization %
LUT	1	53200	0.01
FF	24	106400	0.02
IO	18	200	9.00
BUFG	1	32	3.13

Because this design used minimal logic most of the power consumed by the device was static power. As the transistors were mostly siting idle across the programmable logic fabric.

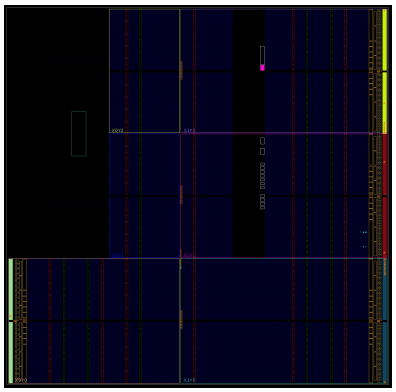

Figure 2. Device Mapping for Part A

Table 2. Resource Usage Part A

Type	Power
Static	0.122 W
Dynamic	0.007 W
Total	**0.129 W**

Due to the design small size the router did not have a problem satisfying the timing constraints of the clock. Shown below is some of the timing information from the timing report.

Table 3. Timing Report Part A

Type	Time
Worst Hold Slack	0.104 ns
Worst Negative Slack	8.442 ns

2.7. Difficulties/Bugs

The only difficulty encountered in this section was just being unfamiliar with the Xilinx design suite.

3. Part C

3.1. Description

For the third part of the MP we had to interface the embedded ARM core with the switches and LEDs through the AXI bus and imitating the behavior of part B in software. The objective of this part was to familiarize ourselves with the process creating custom IP modules and writing software to interface with them.

3.2. Assumptions

The one assumption we made for this part of the MP is that during the modes a change in the switches will be reflected in the LEDs.

3.3. System Configuration

The Zynq 7000's integrated ARM cores interface with the switches and LEDs through a GPIO AXI port. The AXI interface block has two 8 bit channels and are directly connected to the switches and the LEDs. The block diagram of the configuration is shown in figure 3. When the GPIO module is created the Xilinx toolkit will automatically connect the modules for you and instantiate some supporting hardware. The toolkit automatically instantiated a system reset block so that the cores can be reset, as well as an AXI interconnect to allow for multiple AXI modules to be connected.

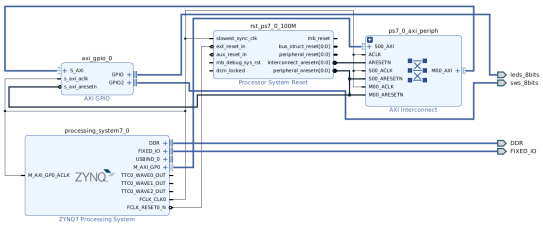

Figure 3. Block Diagram for Part C

A board support package, or BSP, is then generated from our hardware configuration. This allows the software development kit to understand what hardware it has access to and what memory locations the modules are located at. The software then interfaces through memory mapped I/O.

3.4. Entities

Entity	Description
Zinq7	Main ARM core with interconnect and cache
AXI GPIO	GPIO AXI module to interface with switches
System Reset	Resets processor and connected devices
AXI Interconnect	Interconnect fabric for multiple AXI modules

3.5. Design

The other than instantiating a GPIO AXI module, the entire MP was done in software. The program looped through four distinct states spending about 1 second in each state. Within a state, the program sampled the state of the switches through DiscreteRead of the switch channel (channel 0) and then applied the operation for that state to the switch data. The data was then displayed on the LEDs though a DiscreteWrite to the LED channel (channel 1). The modes performed the same functions as Part B and the software flow chart is shown in figure .

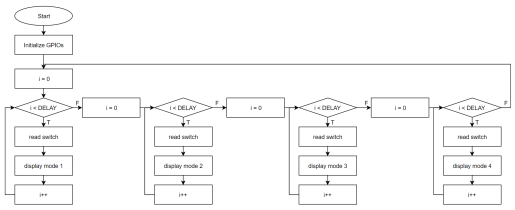

Figure 4. Program Flow for Part C

We settled on a delay iterations number just by trial and error.

3.6. Performance

This a comparably larger design than the other two parts. The AXI GPIO module resided on the Programmable Logic fabric and that contained a lot of logic and registers. The AXI interface is a complex module so it occupied a lot of space after place and route (Figure).

Table 4. Resource Usage Part C

Resource	Utilization	Available	Utilization %
LUT	423	53200	0.80
LUTRAM	63	17400	0.36
FF	648	106400	0.61
IO	16	200	8.00
BUFG	1	32	3.13

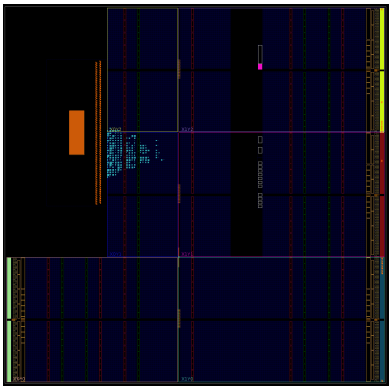

Figure 5. Device Mapping for Part C

This design incorporates the PS7 core which will constantly be consuming dynamic power as it loops through the program which is why the dynamic power is dramatically larger than the static power consumed. This desing is also larger than the others using more on chip resources which is also a reason the power has dramatically increased.

Table 5. Resource Usage Part C

Type	Power
Static	0.154 W
Dynamic	1.535 W
Total	**1.689 W**

Again the design was very small so the place and route tool had no problem meeting the timing constraints. There are very reasonable worst setup and hold times for our design.

Table 6. Timing Report Part C

Type	Time
Worst Hold Slack	0.045 ns
Worst Negative Slack	4.292 ns
Worst Pulse Width Slack	4.020 ns

3.7. Difficulties/Bugs

The only difficulty encountered in this section was generating board support packages and making sure the package was up to date with the hardware. We had ran into issues where the BSP did not match the hardware that was loaded on the FPGA.