Quad ATM User-to-Network Interface and Forwarding

Functional Specification Document

Version 1.0

Disclaimer

This specification is intended as a exercise in functional verification only. The design described herein may not be fit for use in an actual product. There are no warranties expressed or implied.

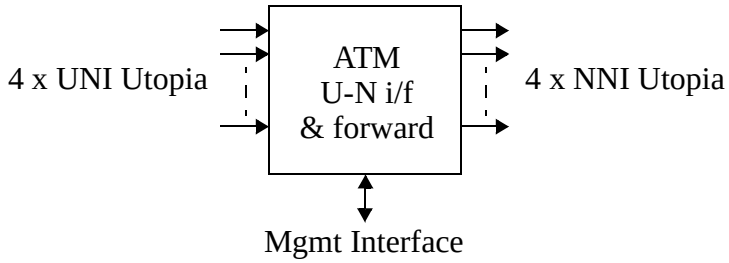
1. Introduction

This document describes the requirements for a Quad ATM user-to-network interface and forwarding node (SQUAT). The objective is to describe the intended functionality of the design. All implementation and physical-level specifications are not available at this time.

1.1 Functional Overview

Figure 1 shows an overview of the design. UNI ATM cells received on four input interfaces are reformatted as NNI cells, then routed to the appropriate output interfaces. The rewriting and forwarding information is maintained by the host processor in an internal register file.The total number of ATM cells dropped due to output interface congestion is continuously reported in an internal status register.

Figure 1.
Overview diagram



1.2 Standards Compliance

The ATM interfaces are compliant with Version 2.01 of the Level 1 Utopia Specification[1], later ammended in Version 1.0 of the Level 2 Utopia Specification[2].

The management interface is compliant with the parallel management interface described in section A2.4 of the Level 2 Utopia Specification. It supports both Intel-compatible and Motorol-compatible modes.

1. ATM Forum Technical Committe, *UTOPIA Specification Level 1*, Version 2.01, Document af-phy-0017.000, March 21, 1994. Available at ftp://ftp.atmforum.com/pub/approved-specs/af-phy-0017.000.pdf
2. ATM Forum Technical Committe, *UTOPIA Level 2*, Version 1.0, Document af-phy-0039.000, June 1995. Available at ftp://ftp.atmforum.com/pub/approved-specs/af-phy-0039.000.pdf

1.3 Performance

The Utopia interfaces operate at the maximum 25MHz transmit and receive clock frequency specified by the standard.

1.4 Packaging Information

The design is packaged as a full-functional model, available in both Verilog and VHDL. The models may not be clock-cycle accurate with each other or with an eventual synthesizable implementation. It is not believed that clock-cycle accuracy is functionally relevant for this design.

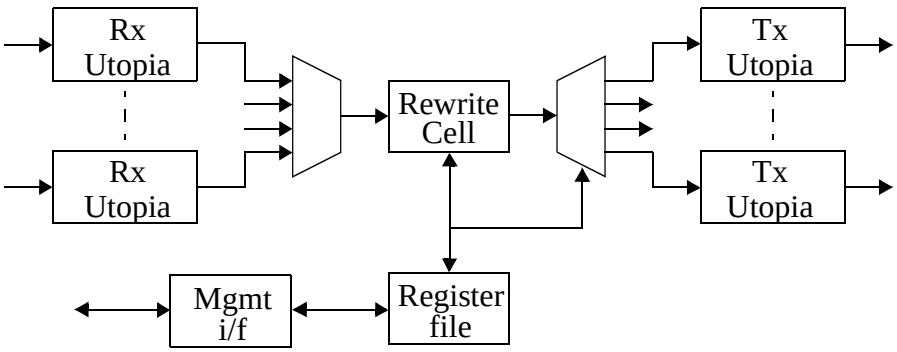
2. System/Logic Description

This section describes the user-to-network interfacing and forwarding process performed by the design. It does not imply any implementation.

2.1 Structural Diagram

The diagram shown Figure 2 in is intended only to show how the information flows within the design. It may correspond to the final implementation structure but that is not a requirement.

Figure 2.
Structural diagram



2.2 Functional Description

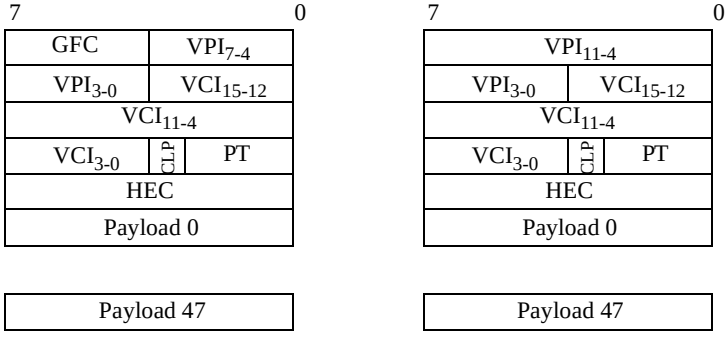
2.2.1 Reset

After a hardware reset, the device's internal state is reset, including the register file. After a reset of the design and of the register file, the device will not forward any cells.

2.2.2 Cell Formats

The design translate cells from the UNI format, as shown in Figure 3(a), to the NNI format, as shown in Figure 3(b). The only fields used by the design are the VPI and HEC fields in the incoming cell. The only fields modified by the design are the GFC and VPI fields in the incoming cells which are replaced with the VPI value of the outgoing cell and the HEC field of the outgoing cell which is recomputed.

Figure 3. UNI and NI cell formats



2.2.3 Cell Rewriting and Forwarding Configuration

The register file contains 256 16-bit values containing the rewriting and forwarding information for each UNI VPI value, from 0x00 to 0xFF. The 16-bit rewriting and forwarding configuration for a given VPI has the following format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Forwarding				NNI-format VPI value											
3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0

The most-significant nibble is the forward mask. It is used to forward cells with a UNI VPI value corresponding to that configuration register to the speci-

fied output ports (after rewriting). A forward value of 0xf will forward cells to all output ports. A forward value of 0x4 will forward cells to output port #2 only. Depending on input traffic patterns, it is possible to create congestion on one or more output ports if many VPIs are configured to be forwarded to the same output ports.

The remaining bits in the configuration register contain the NNI VPI value corresponding to the incoming cell's UNI VPI value. It replaces the GFC and VPI fields of the incoming cell. It is possible for different incoming UNI VPI values to map to the same NNI VPI values.

2.2.4 Rewriting and Forwarding Process

When a cell is received, it is first checked for integrity using the HEC byte. If the cell is errored, it is dropped.

For each non-errored cells received with a non-zero VPI, the configuration information for that cell's VPI is looked up. The cell is then rewritten, replacing the first 12 bits with the NNI VPI value.

The rewritten cell is then replicated on each output port identified in the forward mask. If the output port cannot accept the cell immediately, it will stop the flow of incoming cells from that input port. The cell flow on that input port will resume when the output port is able to accept the new cell in its buffer.

Each output port transmits cells from their output cell buffer.

2.3 Interfaces

The following interfaces are available on the design.

2.3.1 ATM Utopia

The design as four input and four output 8-bit Utopia interfaces.

The design is an ATM-layer device expecting a cell-level flow control.

2.3.1.1 Pins

The signals on the input interfaces are prefixed with "Rx" and are detailed in Table 1. The signals on the output interfaces are prefixed with "Tx" and are

detailed in Table 2. Signals are postfixed with "*_n*" where "*n*" is the interface number, between 0 and 3.

Table 1. Utopia Interface Pin Names for input interfaces.

Name	Width	Direction	Description
Rx_clk_*n*	1	Output	Inputs sampled and outputs produced at the rising edge of this synchronization signal.
Rx_data_*n*	[7:0]	Input	Byte-wide data. Bit [7] is the MSB.
Rx_soc_*n*	1	Input	Active-high start of cell indicator. When asserted, Rx_data contains the first valid byte of a cell
Rx_en_*n*	1	Output	Active-low enable. When asserted, Rx_data and Rx_soc will be sampled by the design at the end of the next cycle.
Rx_clav_*n*	1	Input	Active-high cell-level flow-control indicating, when asserted, there is a complete cell available for transfer to the design.

Table 2. Utopia Interface Pin Names for output interfaces.

Name	Width	Direction	Description
Tx_clk_*n*	1	Output	Inputs sampled and outputs produced at the rising edge of this synchronization signal.
Tx_data_*n*	[7:0]	Output	Byte-wide data. Bit [7] is the MSB.
Tx_soc_*n*	1	Output	Active-high start of cell indicator. When asserted, Tx_data contains the first valid byte of a cell
Tx_en_*n*	1	Output	Active-low enable. When asserted, Tx_data and Tx_soc contain valid cell data.
Tx_clav_*n*	1	Input	Active-high cell-level flow-control indicating, when asserted, a entire cell can be transfered from the design.

2.3.1.2 Protocol

The ATM cell interfaces will be compliant with version 2.01 of the Level 1 specification, ATM Forum document *af-phy-0017.000, ,* later ammended in Version 1.0 of the Level 2 Utopia Specification, ATM Forum document *af-phy-0039.000*. The interface is 8-bit wide and implements cell-level control-flow. The optional parity and reference signals are not implemented.

2.3.1.3 Timing

Refer to ATM Forum documents *af-phy-0017.000* and *af-phy-0039.000* for applicable timing diagrams.

2.3.1.4 Electrical Characteristics

Not applicable

2.3.2 Miscellaneous

The miscellaneous pins are used to implement the design and do not pertain to a specific interface.

2.3.2.1 Pins

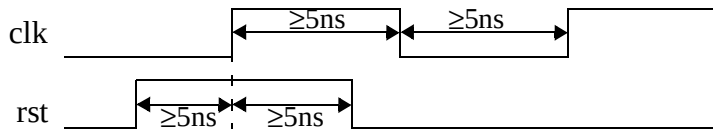
They are described in detailed in Table 3.

Table 3. Miscellaneous pins.

Name	Width	Direction	Description
clk	1	Input	100 MHz system clock.
rst	1	Input	Active-high synchronous reset.

2.3.2.2 Timing

Figure 4. System clock and synchronous reset



2.3.3 Management Interface

The management interface is compliant with the parallel interface, as specified in section A2.4 of the Utopia level 2 specification, ATM Forum document *af-phy-0039.000*.

The cell rewriting and forwarding configuration registers are mapped within the processor address space. Little-endian byte ordering is used, where bits 15 through 8 are located at address 2*VPI + 1 and bits 7 through 0 are located at address 2*VPI.

2.3.3.1 Pins

The host processor interface signals are named to be consistent with the management interface naming convention. They are described in detailed in Table 4.

Table 4. Host processor interface pins.

Name	Width	Direction	Description
BusMode	1	input	Select Intel or Motorola compatibility
Addr	[8:0]	input	Address
Data	[7:0]	Inout	Bi-directional data.
Sel	1	Input	Active-low device select signal. When asserted, indicates that a valid address is present on the address input.
Rd_DS	1	Input	When asserted low: Intel: indicates read cycle Motorola: strobe data
Wr_RW	1	Input	When asserted low Intel: indicates write cycle Motorola: indicates read or write cycle
Rdy_DTACK	1	Output	When asserted low, indicates the completion of the transfer over the data bus. Tristated when device is not selected.

2.3.3.2 Timing

Refer to ATM Forum document *af-phy-0039.000* for applicable timing diagrams.

2.3.3.3 Memory Map

Table 5 shows the address of all 8-bit registers accessible by the host processor. Section 2.3.3.4 describes the content of each register in details.

Table 5. Memory map.

Address	Name	Description
0x000	VPI 0 Configuration	Bits 7 through 0 of the configuration register for VPI 0
0x001	VPI 0 Configuration	Bits 15 through 8 of the configuration register for VPI 0
0x003	VPI 1 Configuration	Bits 7 through 0 of the configuration register for VPI 1
0x003	VPI 1 Configuration	Bits 15 through 8 of the configuration register for VPI 1
...	...	...
0x1FE	VPI 255 Configuration	Bits 7 through 0 of the configuration register for VPI 255
0x1FF	VPI 255 Configuration	Bits 15 through 8 of the configuration register for VPI 255

2.3.3.4 Register Descriptions

Each register is described in details, with the most-significant bit shown on the left. Each bit field is identified with a name. The reset value and access mode are shown below.

VPI n Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Forwarding				NNI-format VPI value											
0b0000				0x000											
Read-Write				Read-WRite											

Forwarding

The output ports on which to forward a cell with the corresponding UNI VPI value. If bit *n* of the forward mask is set, the cell is forwarded to the output port *n*. See Section 2.2.3 for more details.

NNI-format VPI value

The VPI value of the rewritten cell in NNI format. See Section 2.2.3 for more details.