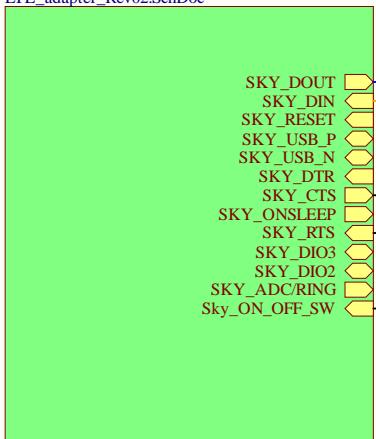
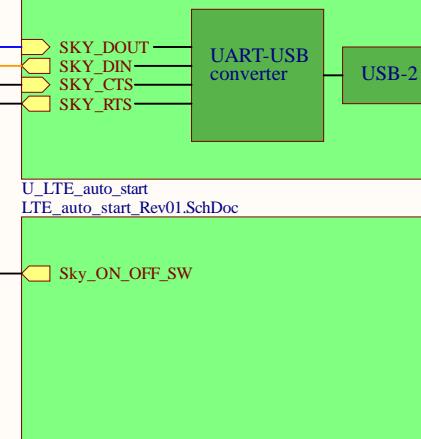


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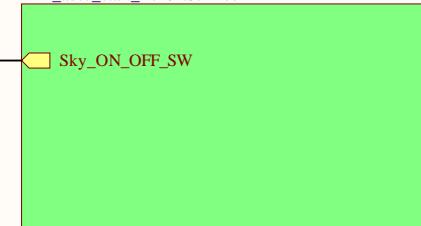
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LTE\_adapter\_Rev02.SchDoc



**U\_LTE\_UART\_USB\_adapter**  
LTE\_UART\_USB\_adapter.SchDoc



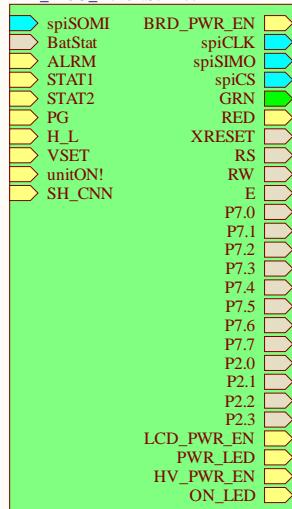
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LTE\_auto\_start\_Rev01.SchDoc



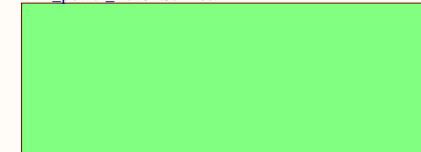
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**U\_LTE MCU Rev01**  
LTE MCU\_Rev01.SchDoc



**U\_LTE\_power**  
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C

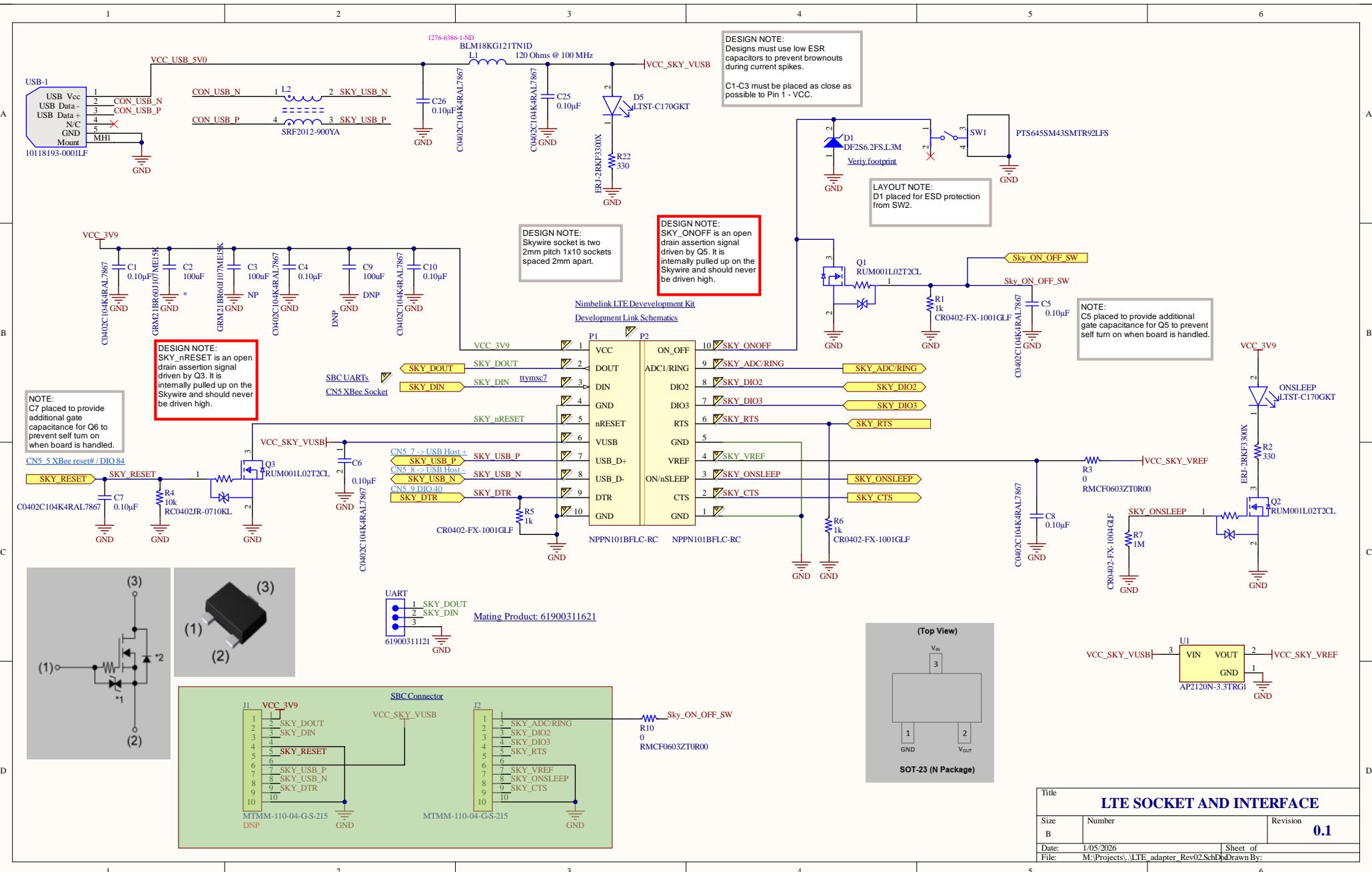
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D

C

D

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Letter		Revision
Date:	1/05/2026	Sheet of
File:	M:\Projects\LTE_block_diagram.SchDoc	Drawn By:
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A

B

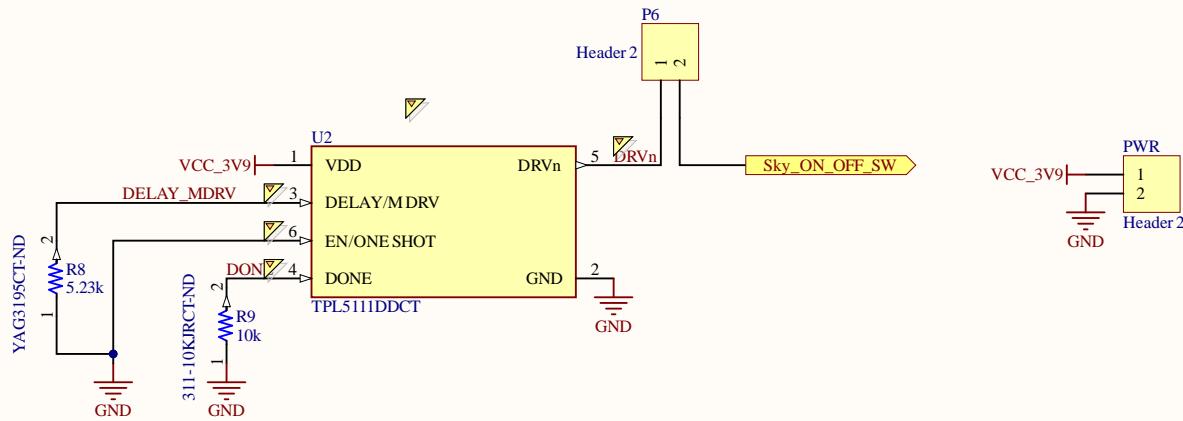
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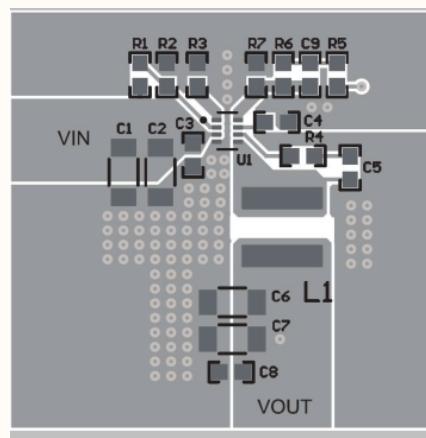
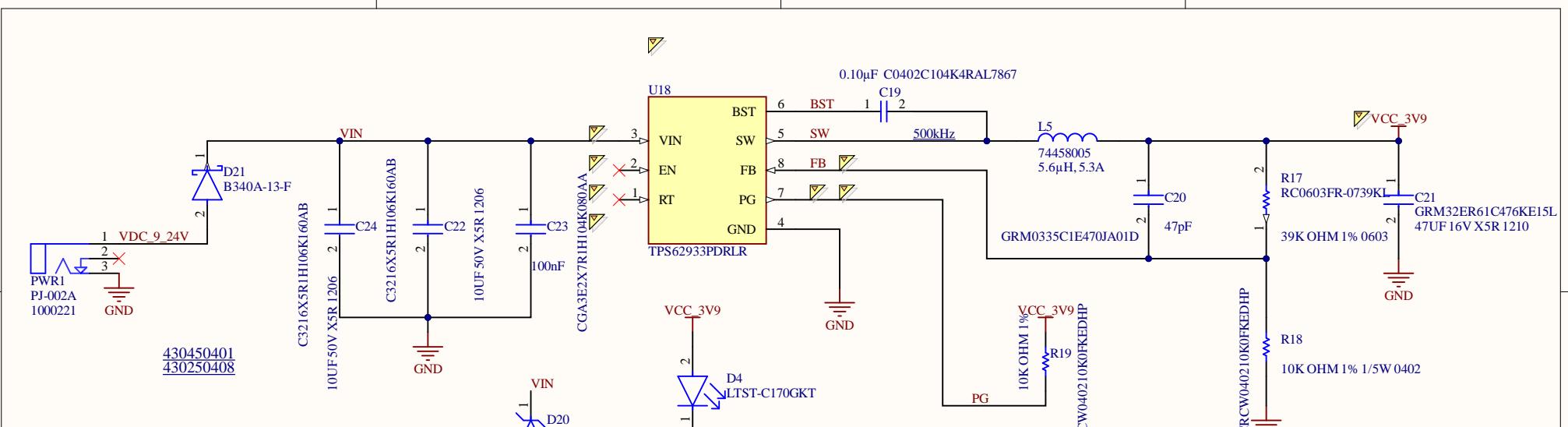
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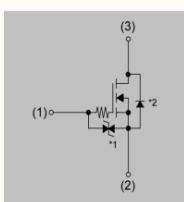
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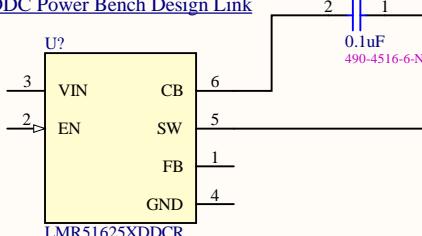
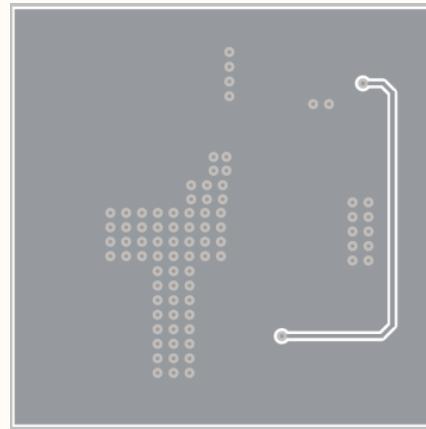
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**Figure 12-2. TPS62933 Top Layout Example**



**Figure 12-3. TPS62933 Bottom Layout Example**



## Title LTE BOARD POWER 9-24VDC to 3.9VDC

Size Letter	Number	Revision
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File:	M:\Projects\LTE_power Rev01 SchDoc	Drawn By:

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A

B

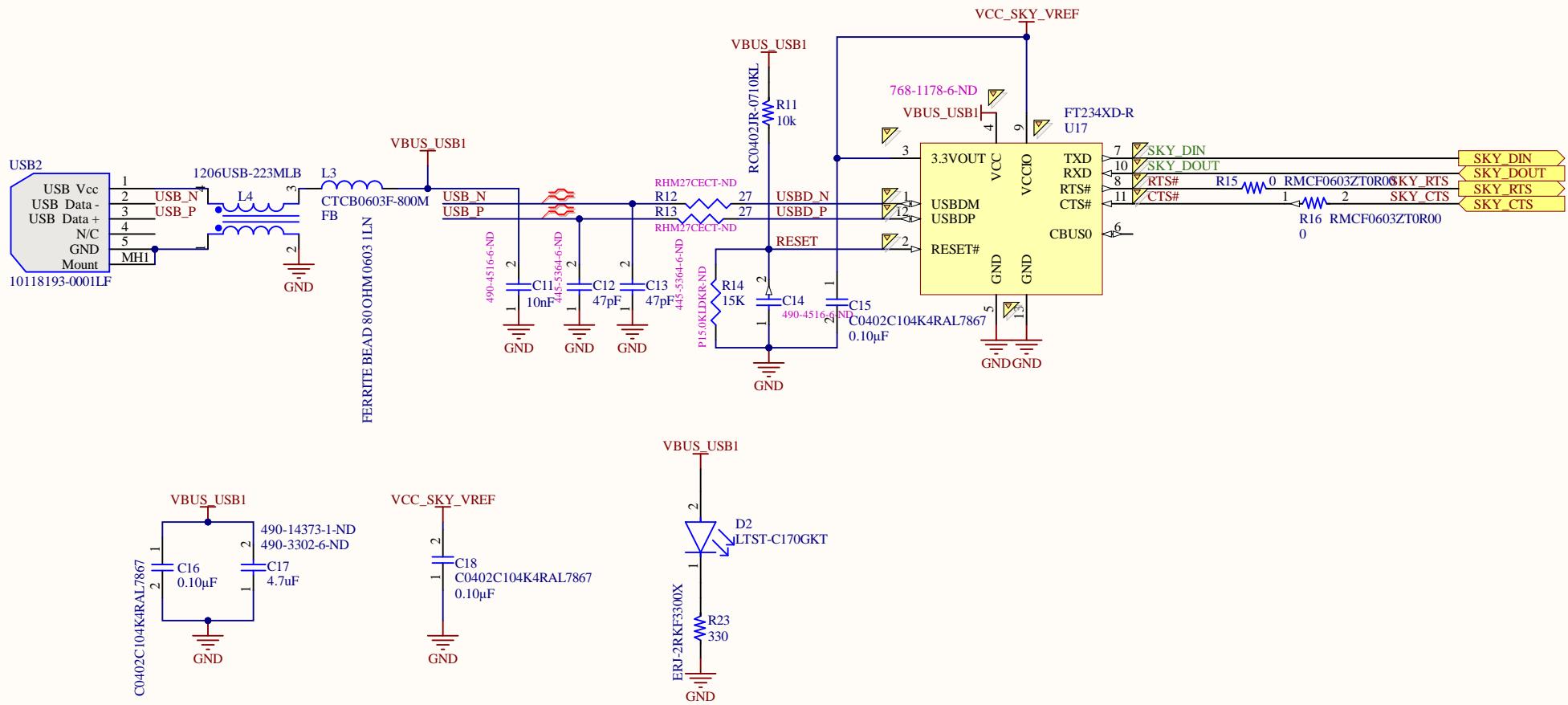
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D

D



Title

**LTE USB-UART**

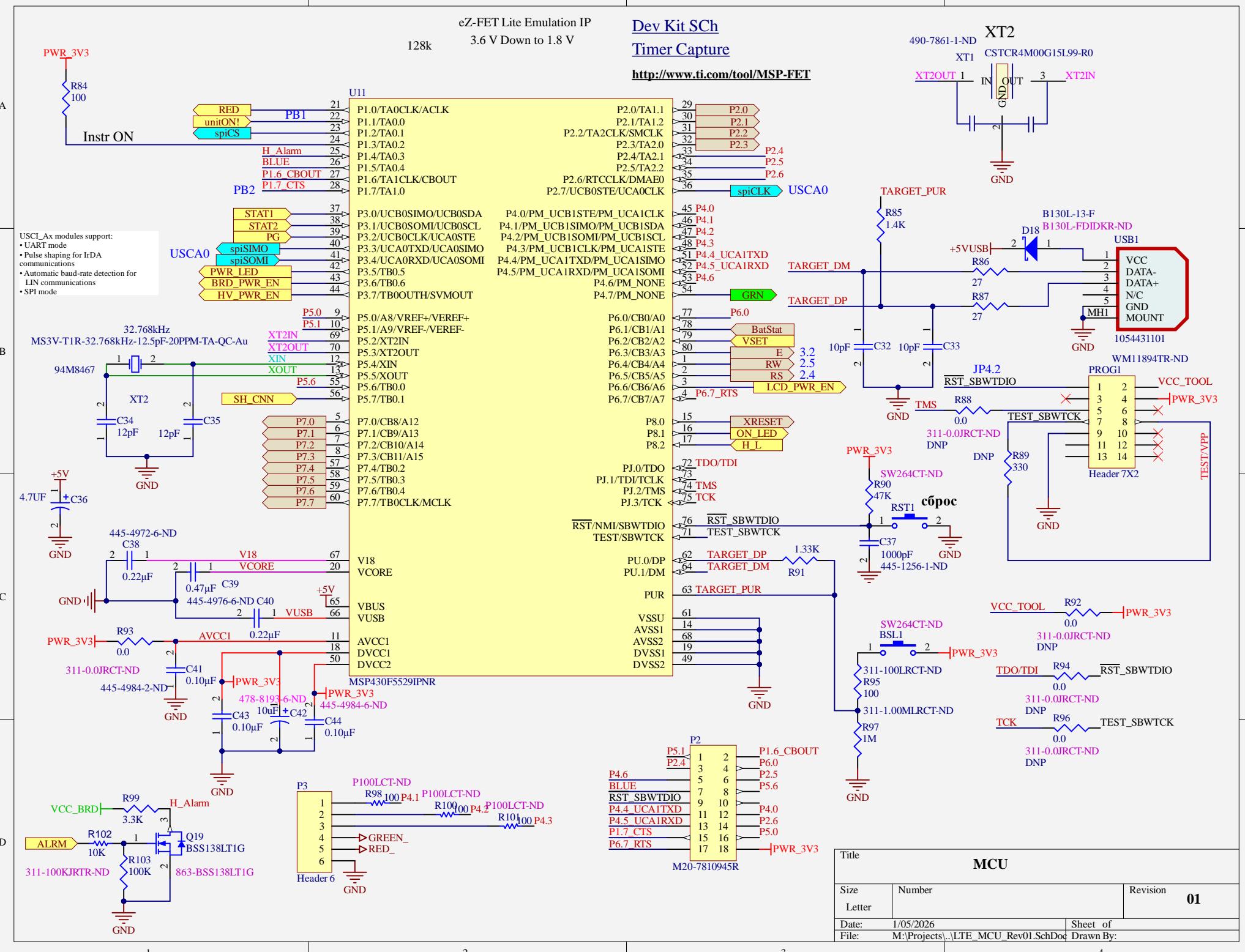
Size Letter	Number	Revision
		<b>01</b>

Date: 1/05/2026

Sheet of

File: M:\Projects\LTE\_UART\_USB\_adapter\

Created By:



1 2 3 4 5 6

NOTES:

- 1/ The vendor shall be UL approved to a minimum category of 94v2.  
The vendor ID. shall be silkscreened on the top side of the board.
2. The UL marking shall appear in copper or silkscreen
3. BOARD MUST BE IDENTIFIED WITH APPROPRIATE VENDOR UL IDENTIFICATION MARK, DATE CODE
4. PCB MATERIAL UL FLAMMABILITY RATING(94V-0 MINIMUM)
5. ALL DIMENSION TOLERANCE AS BELOW UNLESS OTHERWISE SPECIFIED.

6. PCB LAYERS : 4 LAYERS

7. PCB THICKNESS : 62 mil +/-10%

8. TRACE WIDTHS TO BE FINISHED SIZES+/-1MIL

9. TOP SIDE SILKSCREEN : WHITE

BOTTOM SIDE SILKSCREEN: WHITE

10. SOLDER MASK : GREEN, BOTH SIDES

11. MATERIAL : HF\_Fr4 TG: 150 CELSIUS

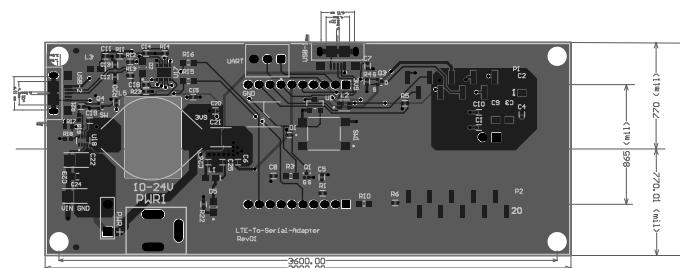
12. PLATING : IMMERSION GOLD (ENIG)

13. PCB Outline Dimension Tol: ROUTING : +/- 0.13mm

14. Fabricate per IPC-6012A CLASS 2

Template	
ENGINEER: Roman Chak	TITLE: PCBA, UVDI-360 LTE ADAPTER BOARD
ENGINEER: XXXXXXXX PHONE:XXX-XXXX-XXXX	PART NO.: 29-9020
FILE NAME: LTE-To-Serial-Adapter.PcbDoc	
LAYER: Top Layer	
MATERIAL: FR4	
DATE: 1/5/2026	

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	CF-004	1.38mil		
	Dielectric 1	PP-017	5.10mil	4.3	
	Dielectric 1A	PP-016	4.60mil	4.4	
2	Mid Layer 1 Sig	CF-004	1.38mil		
	Core	FR-4	39.00mil	4.8	
3	Mid Layer 2 GND	CF-004	1.38mil		
	Dielectric 4	PP-016	4.60mil	4.4	
	Dielectric 2	PP-017	5.10mil	4.3	
4	Bottom Layer	CF-004	1.38mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				



1/5/2026  
11:35:03 AM

1/5/2026  
11:35:03 AM

M:\Projects\Github\IoT-dev\IoT\_Dev\_v0.00\LTE-To-Serial-Adapter.PcbDoc

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DESIGNED FOR: .PRJ_Customer	
FILE NAME: LTE-To-Serial-Adapter.PcbDoc	
ENGINEER: .PRJ_Engineer	SCALE: 1.00
	ALTIUM DESIGNER VERSION: 25.6.2.33

1 2 3 4 5 6 WO # : 307464-7462-D

