Multiple Output SMPS with Improved Input Power Quality

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Abstract—**Personal Computers (PC) and embedded system based control applications require power supplies with multiple outputs delivering stiffly regulated and isolated DC voltages at different levels such as ±5 V, +3.3 V and ± 12 V. At present, most of the commercially available multiple output Switched Mode Power Supplies (SMPS) use multiple number of DC-DC converters that increase the cost and complexity of the system and reduce reliability. In this work, the use of a single DC-DC converter for a multiple output SMPS is proposed and the employability of various DC-DC converters is investigated for a 175 W SMPS. Such an SMPS is designed, modeled and simulated in PSIM with different DC-DC converters such as flyback converter, forward converter, SEPIC and Cuk converter. The performance comparison of these DC-DC converters for a multiple output SMPS is brought out in terms of the output voltage regulation it can offer, response time, Total Harmonic Distortion (THD) of the input current and power factor at the single phase ac mains. The results highlight the merits and demerits of one converter configuration over the others for the SMPS application.**

Keywords-SMPS; Input power quality; Output voltage regulation; Cuk converter; Flyback converter; Forward converter; SEPIC converter.

I. INTRODUCTION

SMPS are rapidly replacing linear regulated power supplies in most of the consumer electronic applications due to their advantages like higher efficiency, better output voltage regulation, compact size and capability to provide isolation between multiple outputs [1-2]. Linear power supply basically consists of a mains transformer and a dissipative series regulator. This means a large and heavy 50/60 Hz transformer is used at the front end that increases the cost, size and weight of the power supply. The efficiency of a linear power supply is very poor and is of the order of 30%-60%. SMPS typically uses switching frequencies of the order of a few tens of kHz and hence the size of associated filtering components and the transformer is reduced drastically. Personal Computers and embedded system based control applications require power supplies with multiple outputs delivering stiffly regulated and isolated DC voltages at different levels such as ±5 V, +3.3 V and ± 12 V. If there are 'n' outputs in an SMPS, it normally uses 'n+1' dc-dc converters to obtain individual control of all the outputs [3-4]. So, the cost of whole system increases and reliability is reduced due to use of many components in the system. Many of these SMPS also use a simple and rugged single-phase diode rectifier (DBR) at the front end. However, the diode rectifiers with capacitor filters cause severe power quality problems when especially such SMPS are used in large numbers. Various power factor correction (PFC) techniques are employed to overcome these power quality problems [5-7]. In a few research papers [8-9], efforts have been made to design a multiple output SMPS with a single DC-DC converter. In this paper, various DC-DC converter topologies such as flyback, forward, Cuk and SEPIC are employed in a multiple output SMPS of 175 W rating, which is typically used in a PC. Models are developed for these circuits in PSIM [10] environment and simulations are performed under similar operating conditions. Based on the results obtained, a comparison of their performances is presented in terms of their voltage regulation capability, response time during starting and load changes and input power quality.

II. INPUT POWER QUALITY IMPROVEMENT IN SMPS

Input power quality becomes a matter of concern in any multiple output SMPS especially if it is being used in large numbers. Some IEEE and IEC standards such as IEEE 519 and IEC 61000 [11-12] have set some limits on the harmonics and unbalance caused by any electrical equipment. In SMPS, normally the switches are turned ON and OFF at a very high frequency. This causes energy transfer from the source to the load to take place in a controlled manner by means of intervening inductors and capacitors. Different control techniques are employed for controlling the energy transfer and also to improve the output voltage regulation and input power quality. Some of them are peak current control, average current control, non-linear carrier control and charge control strategies. The non-linear behaviour of the DC-DC converters causes distortions in the input current and deterioration of power factor. This increases the reactive power drawn by the converter and hence the performance parameters like power factor, distortion factor, and THD deteriorate. The problem has emerged to be so significant that the International Electrotechnical Commission (IEC) has drafted a standard for PFC and harmonic contamination of the AC line [11]. The standard IEC 555-2 used for low power

equipment enforces a minimum power factor value to be achieved by these equipment. In the present work, average current control technique is used to improve the input power quality.

III. OUTPUT VOLTAGE REGULATION

The output voltage is to be stiffly regulated in most of the SMPS circuits irrespective of line and load variations. If it is a multiple output case, they are to be isolated from each other too. In the present work, a weighted error approach has been adopted to achieve regulation of all the outputs irrespective load variation in any of the outputs. Fig. 1 shows the schematic diagram of weighted error approach. In this approach, weightages are assigned for each output such that the energy stored in the transformer is distributed among the different outputs depending on the loads in each output. The voltage delivered at any output is affected by the changes in the demand of power in the other outputs and therefore the duty ratio has to be changed to regulate the affected output.

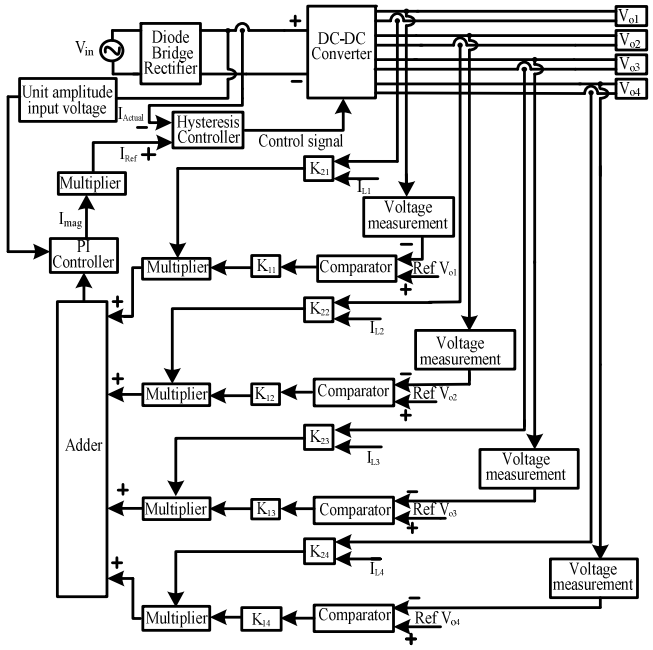

Figure 1. Schematic diagram of weighted error approach

As depicted in Fig.1, the voltage error from each output (V_{o1}, V_{o2}, V_{o3}, V_{o4}) of the converter is individually multiplied by two factors K_1 and K_2 that are specified for each of the outputs separately as follows: K_1 is the ratio of rating of that particular output to the total rating of the SMPS and K_2 is the ratio of the present load on that output to the rating of that particular output. After multiplying by these two factors K_1 and K_2, the individual output voltage errors are added together which is passed through a PI (Proportional & Integral) controller to determine the reference current magnitude I_{mag}. This I_{mag} is multiplied by a unit amplitude sine wave in phase with the mains voltage. This reference current signal I_{Ref} and actual current I_{Actual} are compared in a hysteresis current controller to develop the switching pattern for the converter device ensuring that the actual input current follows the reference current at unity power factor.

IV. MULTIPLE OUTPUT SMPS DESIGN

The design of multiple output SMPS has been done such that the output voltages obtained in open loop are at the required levels when the power supplies are delivering full-load. Closed loop control is employed to achieve good power quality at the utility interface irrespective of line and load variations. The multiple output SMPS considered here is rated approximately at 175 W having four outputs with the following specifications: 5 V/18 A; 12 V/6 A;-5 V/0.3 A;-12 V/0.8 A as given in Table I.

Switching frequency is decided based on the turn-off time of the switching device, operating voltage and maximum allowable switching losses. In the circuit configuration here, a MOSFET is used as the switching device. The duty ratio of the DC-DC converter works out to be small as the input voltage is of the order of 300 V whereas the output voltage is very small. This calls for ripple filters at the input. Similarly, the output voltage regulation requirements are stringent and hence output also requires a large filtering capacitor (C_o) as shown in Fig.2. An output inductor (L_o) may be inserted before the output capacitor that would limit the inductor peak-to-peak current ripple within a specified value for a given switching frequency. The design of a multiple output case is done in the same line as that of a single output case [13-14]. However, the design of the transformer in the multiple output case with multiple secondary windings and the corresponding output filters is more involved. The following sections describe the design of individual DC-DC converters like flyback, forward, Cuk and SEPIC and their performances. Fig.2 shows the circuit configuration of each of these converters in a multiple output case.

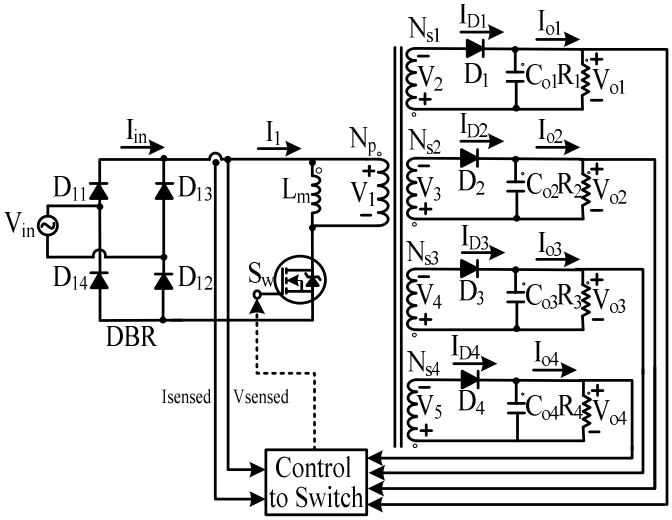

Figure 2. Circuit configuration of multiple output flyback converter

A. Flyback converter

A flyback converter (Fig.2) consists of an input dc voltage, magnetizing inductor of the isolation transformer L_m with primary winding N_p and four secondary windings N_{s1}, N_{s2},

N_{s3}, N_{s4}, high frequency diodes D_1, D_2, D_3, D_4, output filter of capacitors C_{o1}, C_{o2}, C_{o3}, C_{o4} respectively. S_W is the high frequency switch at the primary winding side. The voltage at the output side is having an opposite polarity as compared to the input side making flyback an inverting topology. When the switch is ON the magnetizing inductance L_m stores the energy from the source; during this time the diodes at the output is reverse biased. The stored energy is passed on to the load through the diode at the output side, when the switch is OFF. The energy stored in L_m should be equal to the energy supplied to the load. So, the duty ratio is an important factor. Output capacitors value is so chosen that it eliminates second order harmonic, which is passed on from the ac side. All the secondary outputs are isolated from each other. The various input and output capacitors, inductors values are given in Table II. The switch is chosen such that it can withstand the maximum voltage stress during turn-off and the peak input current. Core losses are the significant limiting factor in the high frequency transformer. Ferrite core is used to minimize core losses at high operating frequencies. Closed loop control is employed to apply control signal to the switch in accordance with the line and load variations.

B. SEPIC (Single Ended Primary Inductor Converter)

Fig. 3 shows the circuit configuration of the isolated multiple output SEPIC which is a buck-boost converter having non-inverted output. This means that the output voltage polarity is same as the input voltage polarity. The circuit diagram for this converter shows a single-phase supply feeding a DBR acting as the front end. The input inductor and capacitor connect the DC output of the DBR through a single switch to the high frequency transformer consisting of a primary winding N_p and four secondary windings N_{s1}, N_{s2}, N_{s3}, N_{s4}. In the output side, four high frequency diodes D_1, D_2, D_3, D_4 and filter capacitors C_{o1}, C_{o2}, C_{o3}, C_{o4} are connected before feeding the required voltage to the loads. The design of SEPIC is explained in [4]. The values of various input and output capacitors and the input inductor for the given specifications are presented in Table II.

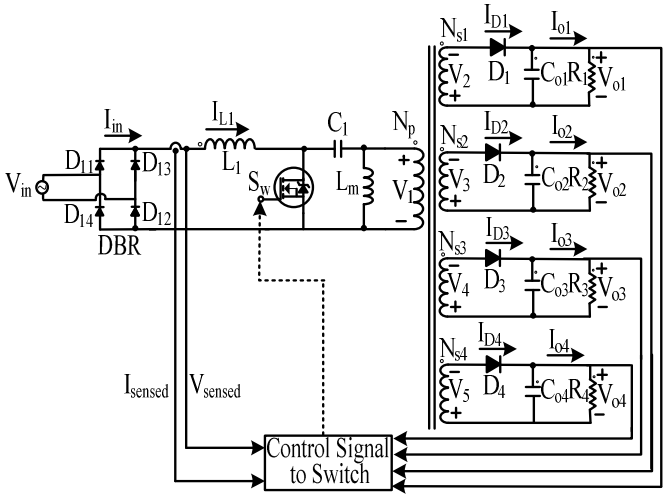

Figure 3. Circuit configuration of single output SEPIC converter

C. Forward Converter

Fig. 4 shows the circuit configuration of the multiple output isolated forward converter, which is a type of buck converter. It offers all the benefits of buck topology with a high level of power quality. It consists of a AC supply V_{in}, single phase DBR, magnetizing inductor of the high frequency transformer L_m with one primary winding N_p, one tertiary winding N_3, four secondary windings N_{s1}, N_{s2}, N_{s3}, N_{s4}, high frequency diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9, output filter of inductor L_1, L_2, L_3, L_4 and capacitor C_{o1}, C_{o2}, C_{o3}, C_{o4} respectively and switching device S_W along with a transformer with its primary winding connected in series with switch S_W to the input supply and a rectification and filtering circuit at each of the secondary windings. A demagnetizing winding N_3 is connected to allow the transformer magnetic energy to be recovered and fed back to input supply. When switch S_W is turned on, input voltage is applied to the primary winding. When switch S_W is turned off, the primary winding as well as all the secondary winding currents are suddenly brought down to zero. The designed values of the multiple output forward converter in Table II.

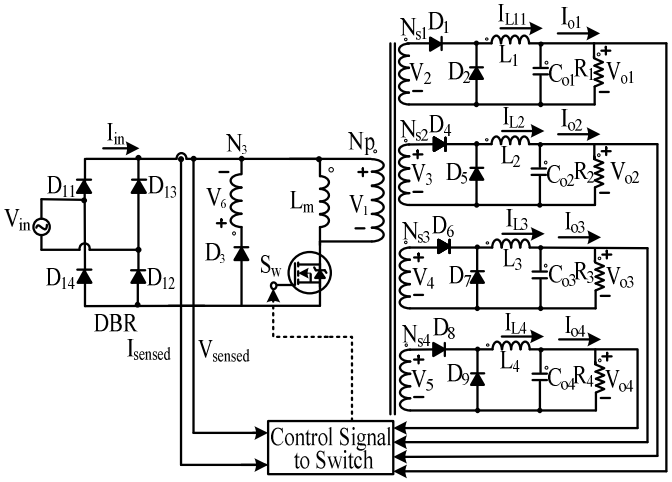

Figure 4. Circuit configuration of single output forward converter

D. Cuk converter

Fig. 5 shows the circuit configuration of the multiple output isolated Cuk converter, which is a type of buck boost converter. The design of a Cuk converter and its various extensions are explained in [14]. In the input section, normally an energy transfer capacitor C_1 exists in the non-isolated Cuk converter which is divided into two portions in the isolated configuration – one on the primary side and the other on the secondary side of the transformer. These are given in Fig. 2d as C_{1o} and C_{11}. In the multiple output case, the energy transfer capacitor is C_{1o} on the primary side and C_{11}, C_{12}, C_{13} and C_{14} are on the four secondary windings of the high frequency transformer. The input inductor is L_1 and the output inductors L_{11}, L_{12}, L_{13}, L_{14} and the output capacitors C_{o1}, C_{o2}, C_{o3}, C_{o4} have been designed for the above mentioned specifications of the multiple output SMPS are given in Table II.

V. SIMULATION RESULTS

As specified earlier, the SMPS has been designed for a multiple output case with +5 V and +12 V having current requirements of 18A and 6 A respectively and -5 V and -12 V outputs of 0.3A and 0.6 A current requirements. As the total rating is well within 250W, the DC-DC converters meant for low power requirements such as flyback and forward converters are also suitable for this particular application.

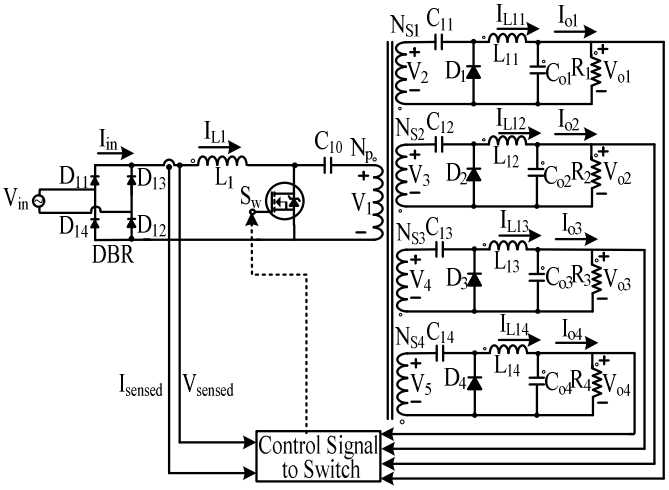

Figure 5. Circuit configuration of single output Cuk converter

A. *Performance of Flyback converter based SMPS*

When the SMPS design is based on a flyback converter, it is found that it takes about 9 cycles (at power frequency) for the output voltages to reach a steady value. The ripples in the various outputs are as specified below: For +5 V it is 1.6%, +12 V it is 1.6%, for -5 V and -12 V the ripples are 1.6% and 1.3% respectively. These are found to be well within acceptable limits.

A load variation of 50% is incorporated on the +5 V outputs at 1 sec and responses are depicted in Fig. 6. It is found that an overshoot is observed at the instant of load reduction by about 4%; but, the control loop acts with a good response time and the output voltages settle back to their nominal values within a duration of 150msec. It is also found that the input power factor remains close to unity and the converter draws a sinusoidal input current from the AC mains during light load as well as full-load conditions.

B. *Performance of SEPIC converter based SMPS*

As the SEPIC converter makes use of inductors and capacitors for energy transfer, it takes longer than the flyback converter to reach steady state. It is found from Fig.7 that it takes about 0.14 sec, to reach steady values of output voltages. Although the ripples in the output voltages are comparable to that of the flyback converter, the current ripples especially for the +5 V output seems to be on the higher side as compared to the flyback converter. The response to the load change is also comparable to that of flyback converter; however, it takes a little longer (i.e., 220msec) to settle back to the nominal voltages for a 50% load reduction. The overshoot in

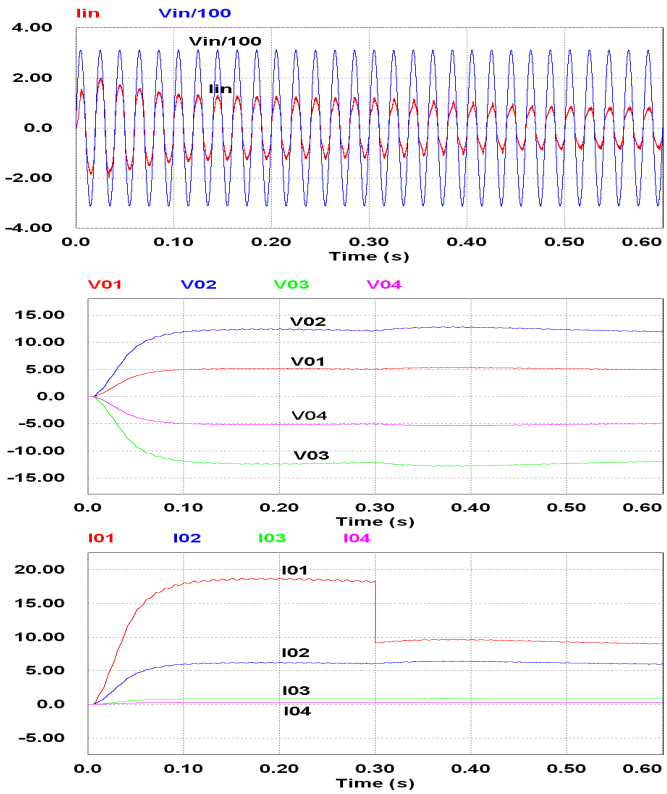

Figure 6. Output voltage, output current, input voltage and input current during load variation of flyback converter

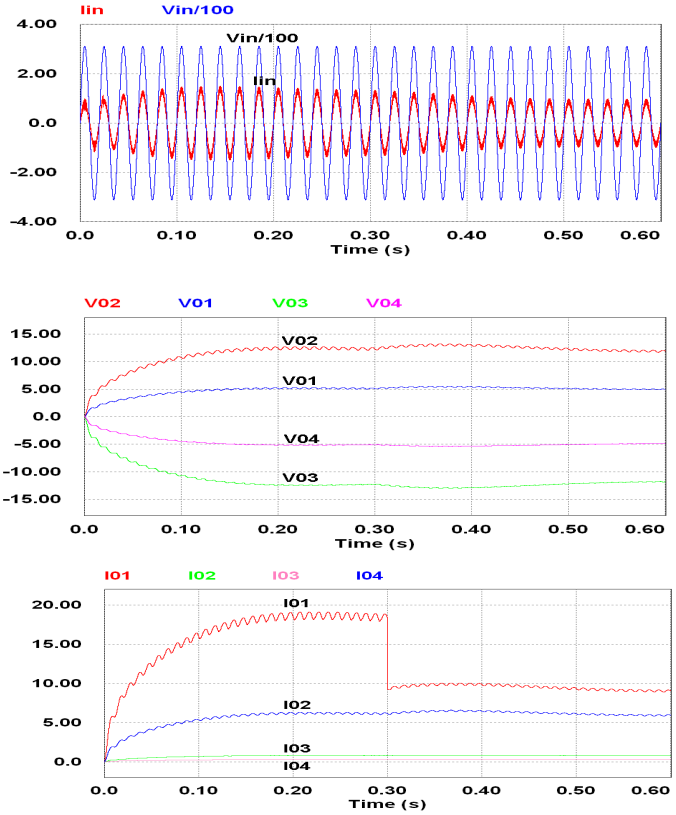

Figure 7. Output voltage, output current, input voltage and input current during load variation of sepic

the +12V and -12 V are 7% and 6% respectively for the SEPIC case.

The input current is observed to be sinusoidal under both full-load and light load conditions with the THD falling within 7.2% under full load condition. The power factor seems to be marginally better than the flyback converter case.

C. *Performance of Forward converter based SMPS*

The starting response of the multiple output SMPS using a forward converter and also the response of this circuit for load change are shown in Fig. 8. It is found that the starting voltage and input current during load variation response of the forward converter and SEPIC converter are comparable in terms of their settling time. However, a kink is observed in the current waveform which may be attributed to the improper tuning of the PI controller gains. The response to the load reduction by 50% is similar to that of SEPIC converter with the overshoots being 7% and 6.2% for +12 and -12 V respectively. The settling time is about 1.9 sec. The power factor is close to unity at the input side with the current fairly being sinusoidal.

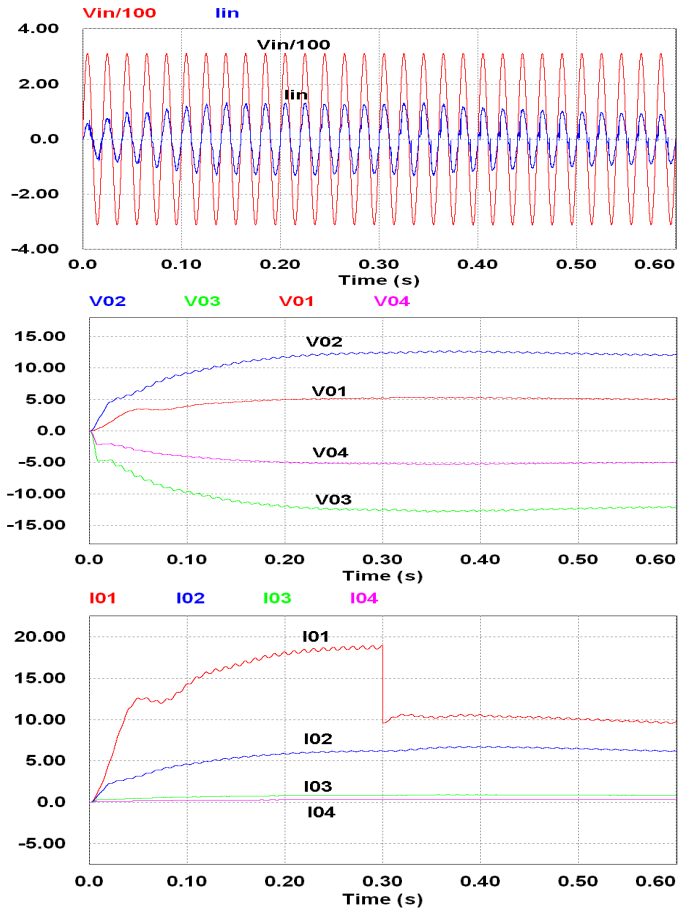

Figure 8. Output voltage, output current, input voltage and input current during load variation of forward converter

D. *Performance of Cuk converter based SMPS*

Fig. 9 shows the response of the multiple output SMPS circuit during starting and load change while employing a Cuk converter. The starting response seems to be very smooth without any overshoots in the output voltages with the settling time being 0.18 sec. The settling time for the voltages when a load change is applied is hardly 0.08 sec. The output voltage ripples are very low and are comparable to flyback and forward converters. The input current is fairly sinusoidal under full-load as well as light load conditions. It can be observed from Table 1 that the Cuk converter yields the lowest value of THD for the input current although SEPIC is the best in terms of power factor.

Table II presents the response of the different converters for a 50% load change in terms of the overshoots in the output voltages and settling time. The THD under light load conditions are also presented. From these two tables, it is found that if an application demands the best possible input power factor and efficiency, then SEPIC is the best choice. If input current THD is the most important performance parameter, then Cuk converter is the best choice. For SMPS of less than 250 W rating with the major objective of minimizing the cost, flyback converter will be the best option. If a moderate performance is to be achieved in terms of the input current THD, power factor, efficiency and the cost of the converter, then forward converter will suit that purpose very well.

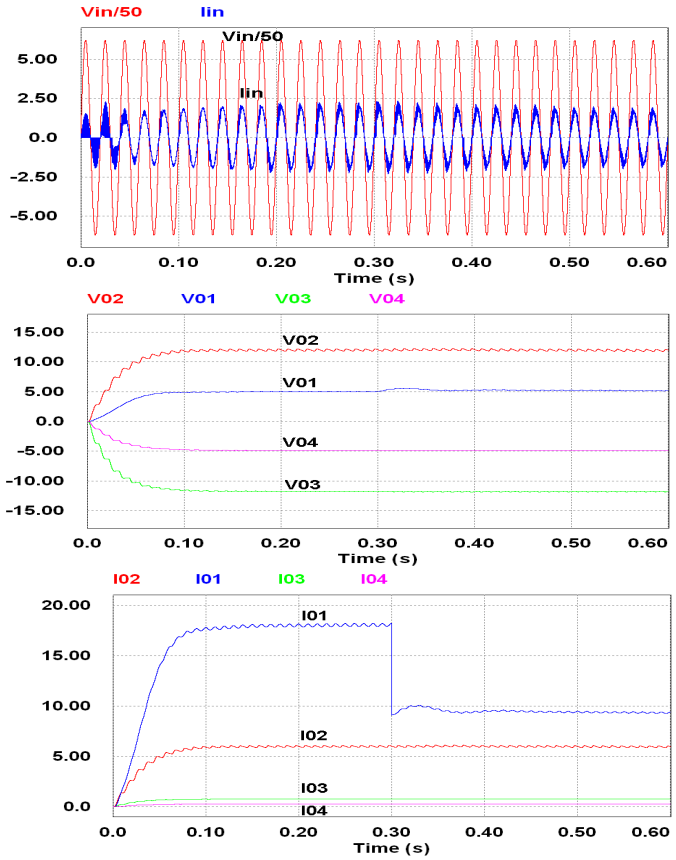

Figure 9. Output voltage, output current, input voltage and input current during load variation of Cuk converter

VI. CONCLUSION

In this paper, the design and simulation of an improved power quality SMPS based on a single flyback, forward, Cuk and SEPIC converters have been presented with multiple

regulated outputs. A comparison of all these configurations is done in terms of various power quality indices in the front end and the output parameters such as voltage ripple and response to load variations, while employing different DC-DC converters in the SMPS circuit. It has been found that when the emphasis is on different performance parameters, different converters turn out to be the best choice for that particular application. The flyback converter is to be best suited for low power applications when the number of components and cost is to be minimized. Forward converter offers moderate performance in every way and also the cost is not high. SEPIC and Cuk converters yield excellent performance in terms of input power quality although these circuits involve more complexity.

TABLE I. COMPARISON OF PERFORMANCES OF CONVERTERS AT FULL LOAD

Converter Topology	Power supply Specification	Output Voltage ripple	I_{Thd} & Power factor		Settling Time (s)
			Full load	*Light Load*	
Flyback Converter	+5 V/18 A	1.6%	4.7% 0.990	8.9% 0.987	0.16
	+12 V/6 A	1.6%			0.15
	-12 V/0.8A	1.3%			0.13
	-5 V/0.3 A	1.6%			0.14
Sepic Converter	+5 V/18 A	3.8%	7.2% 0.998	9.5% 0.994	0.19
	+12 V/6 A	2.2%			0.22
	-12 V/0.8 A	0.8%			0.22
	-5V/0.3 A	1.1%			0.18
Forward Converter	+5 V/18 A	2.4% 2.0%	7.4% 0.994	9.3% 0.985	0.19
	+12 V/6 A				0.19
	-12 V/0.8 A	1.6%			0.19
	-5 V/0.3 A	1.8%			0.18
Cuk Converter	+5 V/18 A	2.1%	4.2% 0.995	5.7% 0.990	0.1
	+12 V/6 A	2.5%			0.1
	-12 V/0.8 A	1.45%			0.05
	-5 V/0.3 A	0.76%			0.05

TABLE II. CONVERTERS SPECIFICATIONS

S.No.	Converter	Component values
1	Flyback Converter	C_{01}=150mF, C_{02}=100 mF, C_{03}=30 mF, C_{04} = 20 mF
2.	SEPIC	C = 40 nF, L=12 mH,C_{01}=150mF, C_{02}=50 mF, C_{03}=40 mF, C_{04} = 40 mF
3.	Forward Converter	Lm=4 mH, L_{11}= 700 uH, L_{12}= 550 uH, L_{13}= 550 uH, L_{14}= 550uH, C_{01}=180 mF, C_{02}=100 mF, C_{03}=20 mF, C_{04}= 15 mF
4.	Cuk Converter	C_{10} = 0.2µF, L_1=5 mH, L_{11}=900µH, L_{12}=50µH, L_{13}=50 µH and L_{14} = 55 µH and C_{11}=150 mF, C_{12}=100 mF, C_{13}=40mF, C_{14}= 40 mF.

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