Logic Gates with NI Multisim

by

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Lecturer

Exercise 4 - 9

Advance Analysis of Logic Gates

Introduction

In order to understand digital electronics, we need to know AND, OR and NOT logic operations, which can be applied using logic gates. Understanding how these gates work and how they combine to create logic statements is important for the design of our own digital circuits used to solve problems, or to understand combinational logic.

Objectives

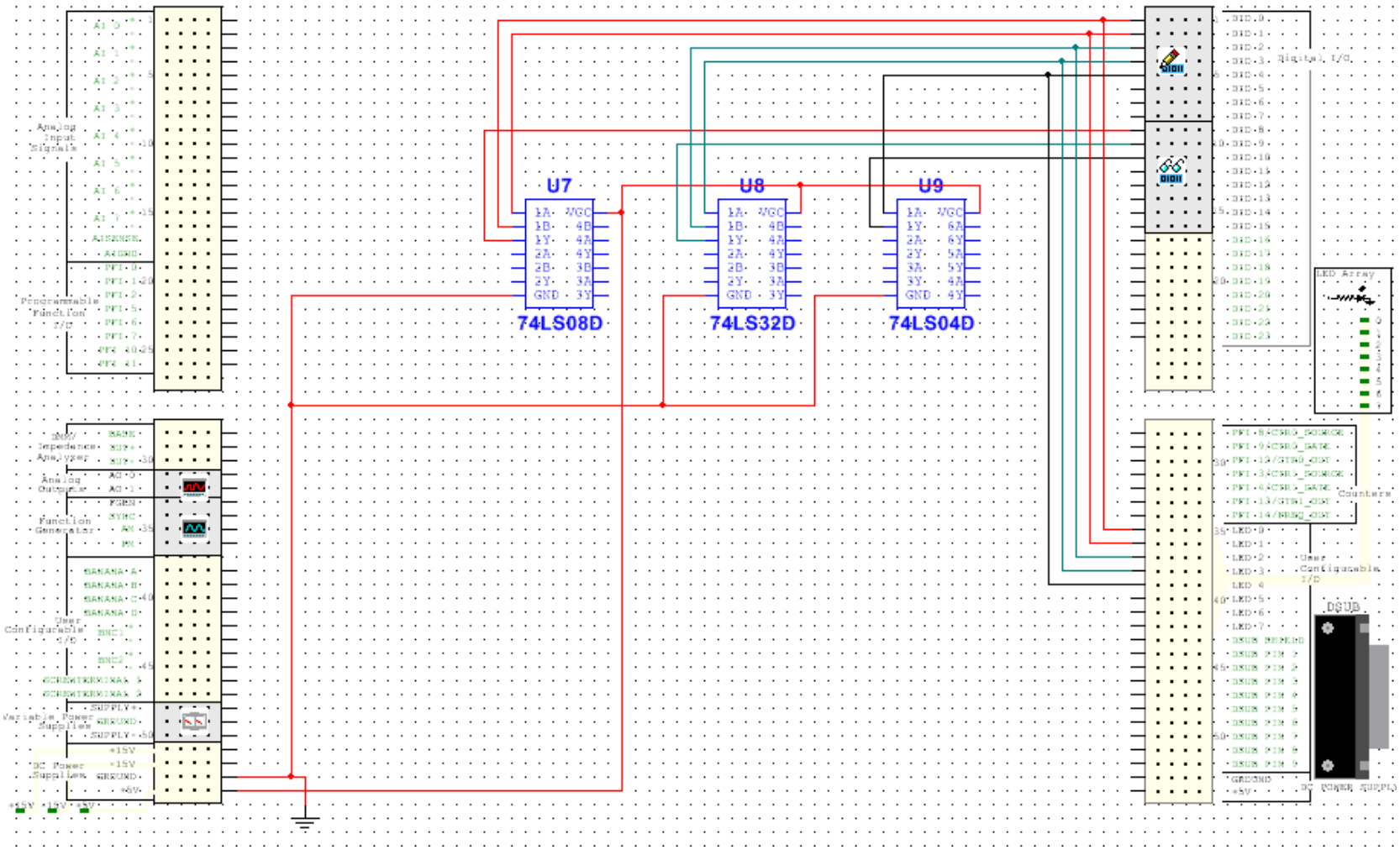
Verify the operation of AND, OR, NOT, NAND, NOR, XOR logic gates.

Parts List

- 1 74LS08D AND gate IC (integrated circuit)
- 1 74LS32D OR gate IC
- 1 74LS04D NOT gate IC
- 1 74LS00D NAND gate IC
- 1 74LS02D NOR gate IC
- 1 74LS86D XOR gate IC

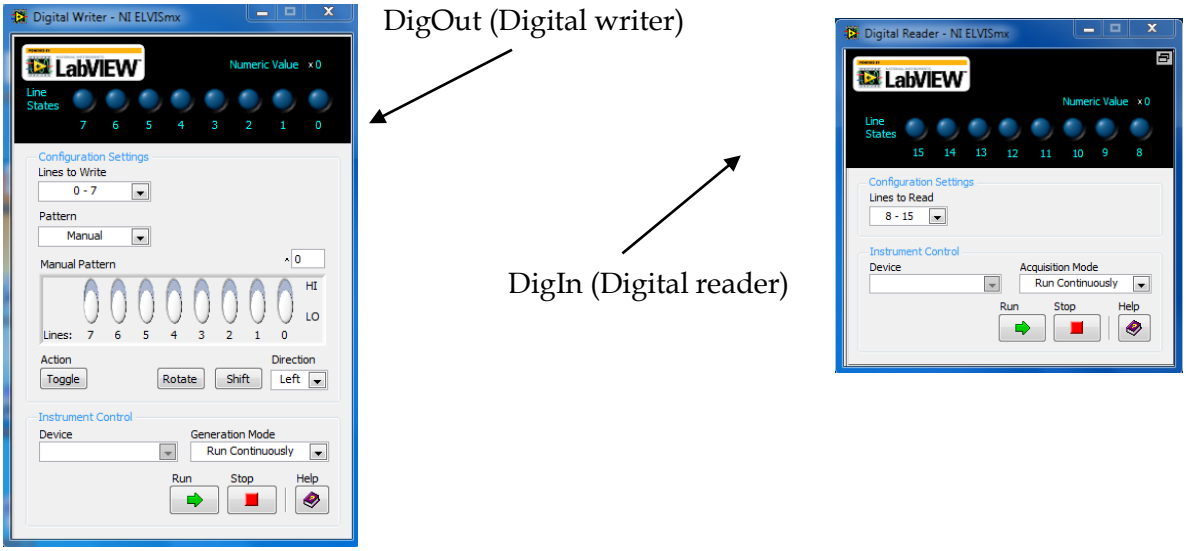
Part 1

1. Use the NI ELVIS II to set up the circuit above, as shown in the illustration.


U7
74LS08D
U8
74LS32D
U9
74LS04D
Analog Input Signals
Programmable Function I/O
Digital I/O
LED Array
Counters
User Configurable I/O
DSUB
Function Generator
Variable Power Supplies
DC Power Supplies

Make sure that the integrated circuits receive their power from the +5 V power supply (pin 54).

2. Turn on the NI ELVIS II, open the NI ELVISmx Instrument Launcher and use the following instruments:
   - DigIn (Digital reader)
   - DigOut (Digital writer)



3. AND Gate (7408)

The AND Gate's two inputs are connected to lines 0 and 1 of the DigOut (Digital writer) and its output is connected to line 8 of the DigIn (Digital reader). On the DigOut (Digital writer), when the switches are moved to HI, this gives a logic 1, and when they are moved to LO, this gives a logic 0. Check the True/False Table for the AND gate and write the results in Table 14-1.

Table 14-1. AND-Gate Behavior

Inputs		Output
A (INT 0)	B (INT 1)	X (LINE 8)
0	0	
0	1	
1	0	
1	1	

4. OR Gate (7432)

The OR Gate's two inputs are connected to lines 2 and 3 of the DigOut (Digital writer) and its output is connected to line 9 of the DigIn (Digital reader). On the DigOut (Digital writer), when the switches are moved to HI, this gives a logic 1, and when they are moved to LO, this gives a logic 0. Check the True/False Table for the OR gate and write the results in Table 14-2.

Table 14-2. OR-Gate Behavior

Inputs		Output
A (INT 2)	B (INT 3)	X (LINE 9)
0	0	
0	1	
1	0	
1	1	

5. NOT Gate (7404)

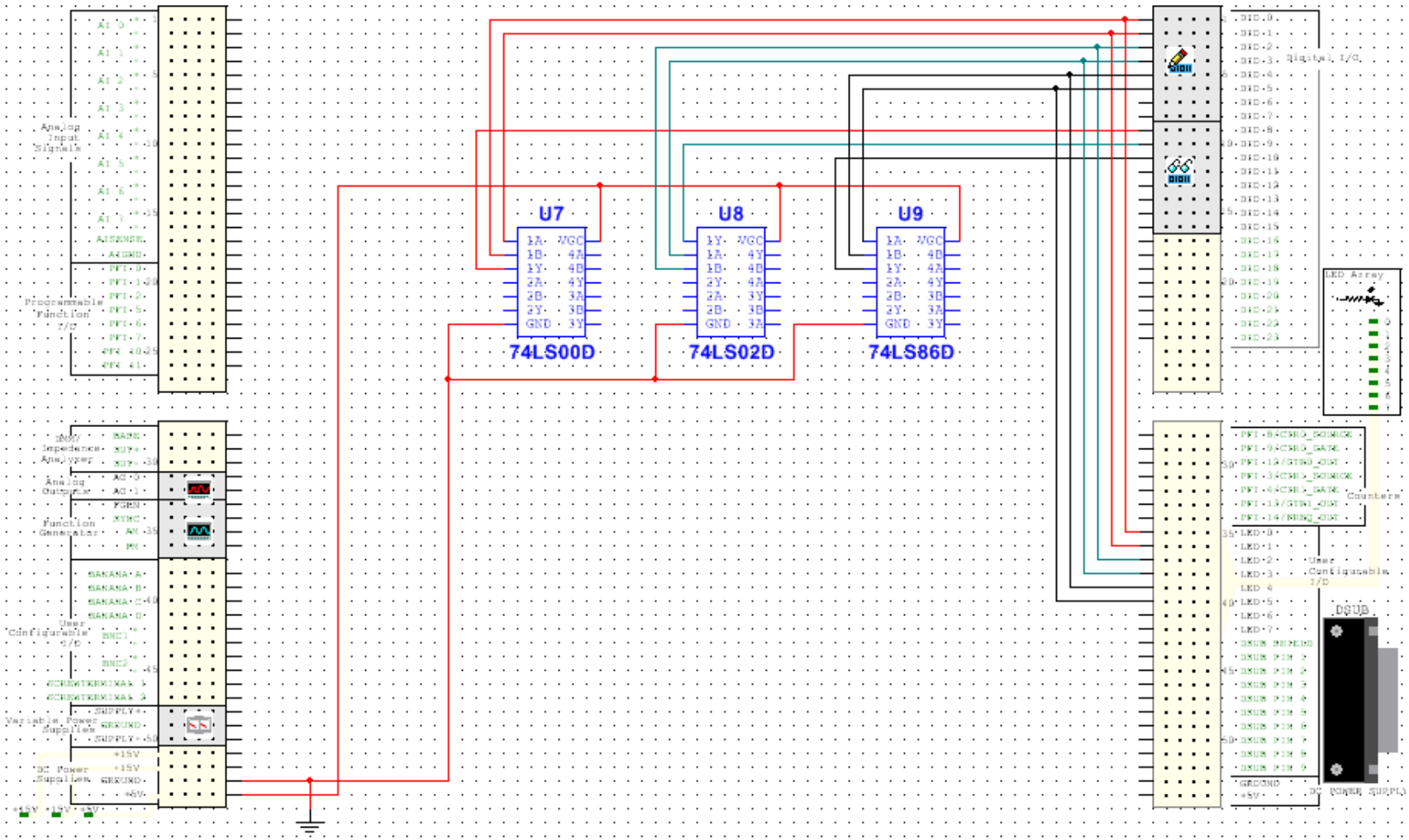
The NOT Gate's input is connected to line 4 of the DigOut (Digital writer) and its output is connected to line 10 of the DigIn (Digital reader). On the DigOut (Digital writer), when the switches are moved to HI, this gives a logic 1, and when they are moved to LO, this gives a logic 0. Check the True/False Table for the OR gate and write the results in Table 14-3.

Table 14-3. NOT-Gate Behavior

Inputs	Output
A (INT 2)	X (LINE 9)
0	
1	

Part 2

6. Use the NI ELVIS II to set up the circuit above, as shown in the illustration.


U7
74LS00D
U8
74LS02D
U9
74LS86D
Analog Input Signals
Programmable Function I/O
Analog Impedance Analyzer
Analog Outputs
Function Generator
User Configurable I/O
Variable Power Supplies
DC Power Supplies
Digital I/O
LED Array
Counters
User Configurable I/O
DSUB
DC POWER SUPPLY

7. NAND Gate (7400)

Make sure that the integrated circuits receive their power from the +5 V power supply (pin 54).

The NAND Gate's two inputs are connected to lines 0 and 1 of the DigOut (Digital writer) and its output is connected to line 8 of the DigIn (Digital reader). On the DigOut (Digital writer), when the switches are moved to HI, this gives a logic 1, and when they are moved to LO, this gives a logic 0. Check the True/False Table for the OR gate and write the results in Table 14-4.

Table 14-4. NAND-Gate Behavior

Inputs		Output
A (INT 0)	B (INT 1)	X (LINE 8)
0	0	
0	1	
1	0	
1	1	

8. NOR Gate

The NOR Gate's two inputs are connected to lines 2 and 3 of the DigOut (Digital writer) and its output is connected to line 9 of the DigIn (Digital reader). On the DigOut (Digital writer), when the switches are moved to HI, this gives a logic 1, and when they are moved to LO, this gives a logic 0. Check the True/False Table for the OR gate and write the results in Table 14-5.

Table 14-5. NOR-Gate Behavior

Inputs		Output
A (INT 2)	B (INT 3)	X (LINE 9)
0	0	
0	1	
1	0	
1	1	

9. XOR Gate

The XOR Gate's two inputs are connected to lines 4 and 5 of the DigOut (Digital writer) and its output is connected to line 10 of the DigIn (Digital reader). On the DigOut (Digital writer), when the switches are moved to HI, this gives a logic 1, and when they are moved to LO, this gives a logic 0. Check the True/False Table for the OR gate and write the results in Table 14-6.

Table 14-6. XOR-Gate Behavior

Inputs		Output
A (INT 4)	B (INT 5)	X (LINE 10)
0	0	
0	1	
1	0	
1	1	