



# Time delay

1

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# Delay

2

MVI C, FFH      7T

LOOP DCR C      4T

JNZ LOOP      10/7T

$T_{\text{delay}} = T_O + T_L$

$T_O$  = delay outside the loop

$T_L$  = delay of the loop

$T_L = ((T_{IL} \times N) - 3)T$

$T_O = 7 \text{ T-States}$

$T_L = (14 \times 255) - 3 = 3567 \text{ T}$

$T_{\text{delay}} = 3574T = 3574 \times 0.5\mu\text{s} = 1787 \mu\text{s}$

Suppose  $F = 2\text{MHz}$  so  $T = 0.5\mu\text{s}$

# Delay Using a Register Pair

3

Note DCX instruction does not affect ZF.

$$TO = 10\ T$$

$$TL = ((24 \times 4096) - 3)T = 98301T$$

$$T_{\text{delay}} = 98311T$$

LXI B, 1000H    10T

LOOP DCX B        6T

MOV A,C            4T

ORA B               4T

JNZ LOOP           10T

# Delay by using nested loop structure

4

**MVI B 10**

**LOOP2 MVI C FF**

**LOOP1 DCR C**

**JNZ LOOP1**

**DCR B**

**JNZ LOOP2**