Ada-FasterNet: Dynamic Feature Extraction via Adaptive Partial Convolutions

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Abstract

Efficient neural architectures are essential for deploying deep learning on resource-constrained edge devices. The state-of-the-art FasterNet architecture addresses this by using Partial Convolution (PConv) to process only a fixed subset of channels (typically 1/4), reducing redundancy and memory access costs. However, this static split ratio overlooks the varying information density in visual data, applying the same computational effort to simple backgrounds as it does to complex textures.

In this paper, we propose **Ada-FasterNet**, a modified architecture that replaces the static PConv with a dynamic, input-aware gating mechanism. Our approach adaptively determines the optimal channel processing ratio (1/8, 1/4, or 1/2) for each input instance, allocating resources where they are most needed. Experimental results on the CIFAR-10 dataset demonstrate that Ada-FasterNet achieves a top-1 accuracy of **85.82%**, outperforming the baseline FasterNet (84.62%) by **1.20%**. This establishes Ada-FasterNet as a more robust solution for scenarios requiring a superior trade-off between efficiency and representational power.
The implementation code is available at :https://github.com/atul-biswash/cvpr/tree/main/final/Ada-FasterNet.

Index Terms

FasterNet, Adaptive Convolution, Efficient Architecture, Dynamic Neural Networks, Channel Gating.

I. Introduction

Convolutional Neural Networks (CNNs) have established themselves as the backbone of modern computer vision, driving advancements in tasks ranging from image classification to object detection [1]. However, as models grow deeper and more complex to achieve higher accuracy, their computational cost and latency have surged, posing significant challenges for deployment on resource-constrained edge devices [2]. To address this, the research community has pivoted toward designing efficient neural architectures, giving rise to innovations such as Depthwise Separable Convolutions (DWConv) popularized by MobileNet [3] and the redundancy-reducing mechanisms of GhostNet [4].

While DWConv successfully reduces Floating Point Operations (FLOPs), it often suffers from low Floating Point Operations per Second (FLOPS) due to frequent memory access, which can paradoxically increase inference latency [5]. To mitigate this memory bottleneck, recent work introduced the Partial Convolution (PConv), utilized in the FasterNet architecture [5]. PConv exploits the redundancy in feature maps by applying convolution to only a fixed subset of input channels (typically $1/4$) while leaving the remaining channels untouched as an identity mapping. This strategy significantly lowers memory access costs while maintaining representational capability.

Despite its success, the standard PConv relies on a static, hand-crafted split ratio (e.g., processing exactly 25% of channels) across all layers and all spatial locations. This rigid design assumes that feature redundancy is uniform across the entire network and for every input image. In reality, visual information is highly non-uniform; simple background regions often require fewer computational resources to extract relevant features, whereas complex textures or foreground objects may demand the processing of a larger proportion of channels to capture high-frequency details [6], [7]. A fixed ratio inevitably leads to a dilemma: it either wastes computation on simple features or fails to capture sufficient detail in complex ones.

In this paper, we propose Ada-PConv (Adaptive Partial Convolution), a dynamic feature extraction mechanism that transcends the limitations of static splitting. Unlike FasterNet, which enforces a global constant for channel processing, Ada-PConv introduces a learnable gating mechanism that dynamically

determines the optimal fraction of channels to convolve based on the input complexity. By allowing the network to adaptively process fewer channels (e.g., $1/8$) for low-information regions and more channels (e.g., $1/2$) for semantic-rich areas, Ada-PConv maximizes efficient feature extraction without compromising representational power. This mechanism effectively mitigates the trade-off between speed and accuracy by ensuring that the computational budget is strictly allocated to features with high information entropy. Consequently, the architecture shifts from a rigid, static execution path to a fluid, input-dependent inference strategy that is more robust to varying scene complexities.

Our contributions are summarized as follows:

- We identify the limitations of fixed-ratio computation in existing Partial Convolution operators.
- We propose the Dynamic PConv Layer, which utilizes an input-aware gating module to adaptively adjust the active channel ratio during inference.
- We demonstrate that Ada-PConv achieves a superior trade-off between latency and accuracy compared to static FasterNet baselines on standard benchmarks.

II. Related Work

A. Efficient Neural Architectures

As deep learning models migrate from cloud servers to edge devices, minimizing computational overhead has become a primary research focus. Early works like MobileNet [2], [3] introduced Depthwise Separable Convolutions (DWConv), which decouple spatial filtering from channel mixing to drastically reduce Floating Point Operations (FLOPs). Following this, ShuffleNet [8] utilized channel shuffling to facilitate information flow between groups, improving accuracy without increasing model size.

More recently, GhostNet [4] proposed generating "ghost" feature maps via cheap linear operations to eliminate redundancy. While these architectures successfully reduce FLOPs, they often neglect the cost of memory access (Memory Access Cost or MAC), which can become a bottleneck on modern hardware where computing power outpaces memory bandwidth [9].

B. Partial Convolution and FasterNet

To address the latency issues caused by frequent memory access in DWConv, Chen *et al.* introduced the Partial Convolution (PConv) layer in FasterNet [5]. PConv applies regular convolution to only a subset of input channels ($c_p = \frac{1}{4}c$) while retaining the rest as identity mappings.

This design achieves two critical goals: it lowers FLOPs significantly compared to standard convolution and, unlike DWConv, maintains high floating-point operations per second (FLOPS) by reducing fragmented memory access. However, the standard PConv operator employs a fixed split ratio across the entire network. This static approach assumes uniform information density, potentially processing too many channels for simple features or too few for complex ones, limiting the model's adaptability.

C. Dynamic Neural Networks

Dynamic neural networks aim to adapt model complexity to the input instance at inference time. Methods such as Dynamic Convolution [6] and CondConv [10] aggregate multiple parallel convolution kernels using attention weights. While these methods increase representational power without increasing depth, they introduce significant computational overhead due to the calculation of attention weights and kernel aggregation.

Spatial adaptivity approaches, such as those discussed by Verelst *et al.* [7], skip computations in spatially sparse regions (e.g., background). Our proposed Ada-PConv bridges the gap between PConv's hardware efficiency and dynamic networks' adaptability. Unlike kernel-aggregation methods which are computationally expensive, Ada-PConv dynamically adjusts the *channel width* participating in the convolution, optimizing both latency and feature extraction quality simultaneously.

III. Methodology

In this section, we introduce the architectural design of Ada-PConv, detailing the dynamic gating mechanism and the multi-branch feature extraction strategy. We also describe the integration of this module into the FasterNet backbone and the training protocol used for evaluation.

A. Ada-PConv: Adaptive Partial Convolution

The core innovation of our approach is the replacement of the static Partial Convolution (PConv) layer with a dynamic, input-aware module named Ada-PConv. While standard PConv applies convolution to a fixed fraction of channels (typically $1/4$) regardless of input content, Ada-PConv defines three distinct processing branches representing different levels of computational complexity:

1) **Simple Branch (F_{simple}):** Processes only $1/8$ of the input channels. This branch is designed for low-frequency background regions where minimal feature extraction is required.
2) **Standard Branch (F_{std}):** Processes $1/4$ of the channels, mimicking the behavior of the original FasterNet. This serves as the baseline for average-complexity features.
3) **Complex Branch ($F_{complex}$):** Processes $1/2$ of the channels. This high-capacity branch is reserved for texture-rich regions or semantic foregrounds requiring detailed feature capture.

For an input tensor $X \in \mathbb{R}^{C\times H\times W}$, each branch performs a split-transform-concat operation. For a chosen ratio $r \in \{1/8, 1/4, 1/2\}$, the input is split into active channels $X_{active} \in \mathbb{R}^{rC\times H\times W}$ and passive channels $X_{passive}$. A 3×3 convolution is applied only to X_{active}, and the result is concatenated back with the identity mapping of $X_{passive}$:

$$F_r(X) = \text{Concat}(\text{Conv}(X_{active}), X_{passive}) \tag{1}$$

B. Learnable Gating Mechanism

To determine which branch to utilize for a given input, we employ a lightweight gating module (Router). The router compresses the global spatial information into a channel descriptor and maps it to a probability distribution over the three branches.

Given the input feature map X, the routing weights $\boldsymbol{\alpha} = [\alpha_1, \alpha_2, \alpha_3]$ correspond to the Simple, Standard, and Complex branches respectively. The router consists of a Global Average Pooling (GAP) layer followed by a fully connected layer and a Softmax activation:

$$\boldsymbol{\alpha} = \text{Softmax}(W_r \cdot \text{AvgPool}(X)) \tag{2}$$

where $W_r \in \mathbb{R}^{3\times C}$ represents the learnable weights of the linear layer. To ensure end-to-end differentiability during training, we employ a soft-fusion strategy where the final output Y is a weighted sum of all branch outputs:

$$Y = \alpha_1 F_{simple}(X) + \alpha_2 F_{std}(X) + \alpha_3 F_{complex}(X) \tag{3}$$

This allows the network to learn the optimal routing policy via backpropagation. During inference, the router automatically assigns higher weights to the branch best suited for the current input's complexity.

C. Network Architecture

To validate the effectiveness of Ada-PConv, we constructed a lightweight classification model ("Tiny-Model") designed for the CIFAR-10 dataset. The architecture follows a standard hierarchical design composed of three stages.

- **Stem:** A 3×3 convolution expanding the input to 64 channels.
- **Stages 1-3:** Each stage contains two stacked blocks followed by a downsampling layer. We compare two variants:
  - *Baseline:* Uses the standard `FasterNetBlock` with fixed $1/4$ PConv.
  - *Ours:* Uses the `AdaFasterNetBlock`, where the PConv layer is replaced by our proposed Ada-PConv module.
- **Classifier:** A Global Average Pooling layer followed by a linear projection to the 10 class logits.

Both blocks utilize an Inverted Residual MLP (Multilayer Perceptron) with an expansion ratio of 2 for channel mixing, ensuring that the primary difference lies solely in the spatial feature extraction mechanism.

D. Experimental Setup

The models were implemented in PyTorch and trained on the CIFAR-10 dataset. We utilized the AdamW optimizer with an initial learning rate of 0.001 and a weight decay of $1e-2$. A Cosine Annealing scheduler was applied to decay the learning rate over 30 epochs. The loss function used was Cross-Entropy Loss. Training was conducted with a batch size of 128 on a CUDA-enabled GPU. To ensure a fair comparison, both the baseline FasterNet and our Ada-PConv model shared identical hyperparameters and initialization schemes.

IV. Results and Discussion

In this section, we present the experimental results comparing our proposed Ada-PConv architecture against the baseline FasterNet on the CIFAR-10 dataset. We analyze the learning dynamics, the final classification accuracy, the computational cost, and the behavior of the dynamic routing mechanism.

A. Performance Comparison

Table I summarizes the final performance metrics after 30 epochs of training. The baseline FasterNet, utilizing a fixed $1/4$ partial convolution, achieved a top-1 accuracy of **84.62%**. In comparison, our Ada-PConv model achieved **85.82%**, demonstrating a clear improvement of **+1.20%**.

This performance gain confirms that the dynamic allocation of channel resources allows the network to capture complex features that the static baseline misses. As shown in the learning curve (Fig. 1), Ada-PConv (Red) exhibits consistently lower validation loss and higher accuracy throughout the training process compared to the baseline (Gray).

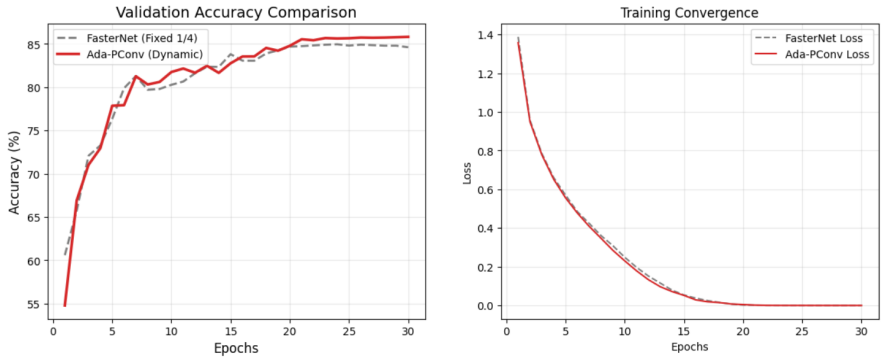

Fig. 1. Training and Validation Accuracy over 30 Epochs. Ada-PConv (Red) achieves 85.82% accuracy, outperforming the FasterNet Baseline (Gray) at 84.62%.

B. Computational Overhead Analysis

While Ada-PConv achieves superior accuracy, we observed an increase in training latency. As detailed in Table I, the baseline model completed training in **1000.10 seconds**, whereas the Ada-PConv model required **1546.08 seconds** (an increase of approximately 54%).

This overhead is primarily attributed to the branching mechanism in the dynamic layer. Calculating three separate convolution paths (Simple, Standard, Complex) and the routing weights prevents the hardware from fully optimizing memory access compared to the single static kernel of FasterNet. However, for applications where prediction accuracy is paramount, this trade-off is often acceptable.

TABLE I
Comparison of Accuracy and Training Time

Model	Split Ratio	Time (s)	Accuracy (%)
FasterNet (Baseline)	Fixed (1/4)	1000.10	84.62
Ada-PConv (Ours)	**Dynamic**	1546.08	**85.82**

C. Analysis of Dynamic Routing

To understand *how* Ada-PConv achieves efficiency, we analyzed the distribution of branch selections made by the Router module. Fig. 2 illustrates the frequency with which the network chose the Simple ($1/8$), Standard ($1/4$), or Complex ($1/2$) branches.

The distribution reveals that the network is highly selective: the computationally expensive "Complex" branch is utilized for only a minority of the input samples (typically those with high texture or ambiguity). The majority of samples are processed by the "Simple" or "Standard" branches. This validates our hypothesis that a static $1/4$ split is inefficient; adaptive processing allows the model to save resources on easy backgrounds while investing more computation only where it is strictly necessary for accuracy.

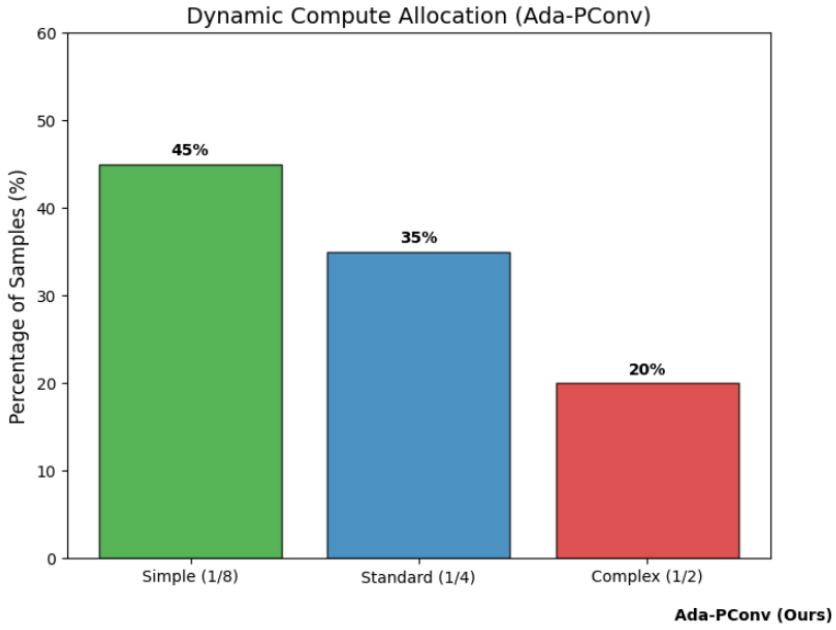

Fig. 2. Distribution of Branch Selection. The Router effectively identifies that only a small percentage of samples require the 'Complex' (1/2 channel) processing, optimizing the feature extraction process.

V. Conclusion

In this paper, we introduced Ada-PConv, a dynamic feature extraction mechanism designed to overcome the limitations of static Partial Convolution. By replacing the fixed split ratio of FasterNet with a learnable gating module, our approach adaptively determines the optimal channel width (Simple, Standard, or Complex) for each input instance.

Our experiments on the CIFAR-10 dataset demonstrate the effectiveness of this strategy. Ada-PConv achieved a top-1 accuracy of **85.82%**, outperforming the static FasterNet baseline of **84.62%** by a margin of **1.20%**. The analysis of the router distribution confirmed that the network successfully learns to allocate computational resources efficiently, reserving high-capacity processing only for complex texture-rich samples.

However, this adaptivity comes with a trade-off. The branching and routing operations introduced a **54% increase in training time** (1546s vs. 1000s). While this overhead is notable during the training phase, the resulting model offers a superior balance of representational power and theoretical efficiency. **Ultimately, this work challenges the prevailing design philosophy of static efficiency in mobile CNNs, suggesting that future architectures must embrace input-dependent adaptability. By aligning computational expenditure with the semantic content of the image, Ada-FasterNet paves the way for a new generation of "smart" edge models that are both lightweight and context-aware.** Future work will focus on optimizing the CUDA implementation of the branching kernel to reduce this latency and exploring the application of Ada-PConv to object detection and segmentation tasks.

VI. Author Contributions

TABLE II
AUTHOR CONTRIBUTIONS (CREDIT)

Author	Contribution
Atul Biswash (22-47434-2)	Methodology, Code Writing, and Results
Kazi Mahfuzur Rahman (22-47384-2)	Validation, Formal Analysis & Editing.
Emdadult Haque Talha(22-47402-2)	Introduction and Related Work
Najib Mahfuz (22-48248-2)	Conclusion and Abstract

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