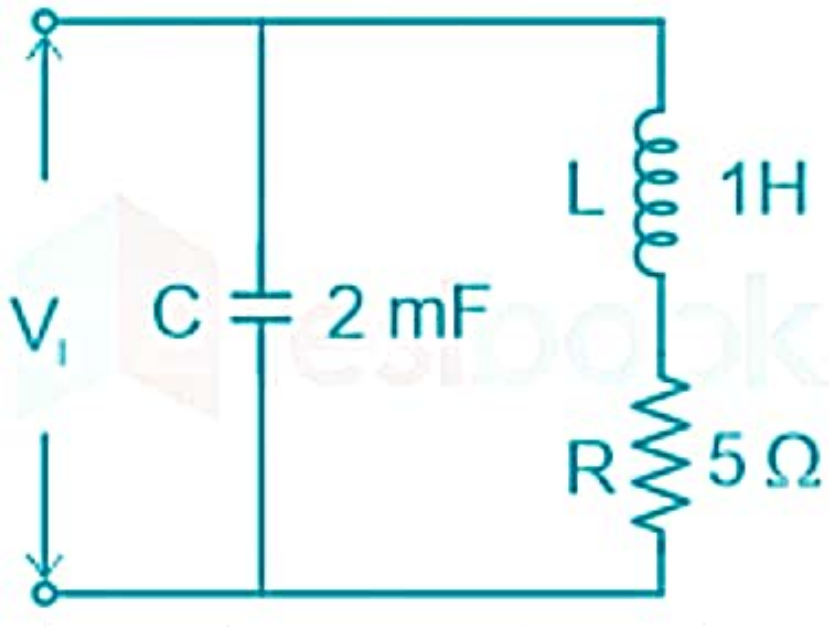
2 55sec | +1.0 -0.33

Consider the circuit as shown in the figure below:



The Q-factor of the inductor is

1. $\sqrt{20}$
2. $\sqrt{18}$
3. $\sqrt{50}$
4. $\sqrt{49}$

Correct Answers Is: 1 35% got this right

SOLUTION

Concept:

The quality factor is given by:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

where Q = Quality factor

R = Resistance

L = Inductor

C = Capacitance

Calculation:

Given R= 5Ω, L= 1H, C= 2mF

$$Q = \frac{1}{5}\sqrt{\frac{1}{2\times10^{-3}}}$$

$$Q = \sqrt{\frac{1000}{2\times25}}$$

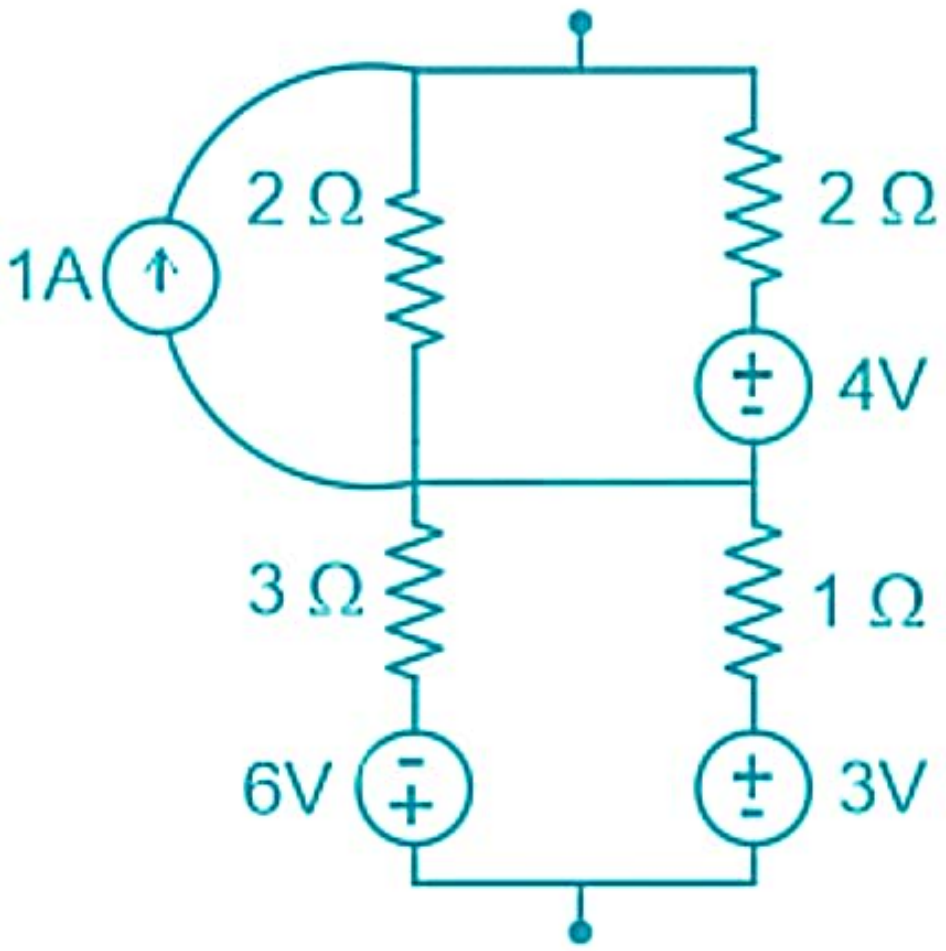
$$Q = \sqrt{20}$$

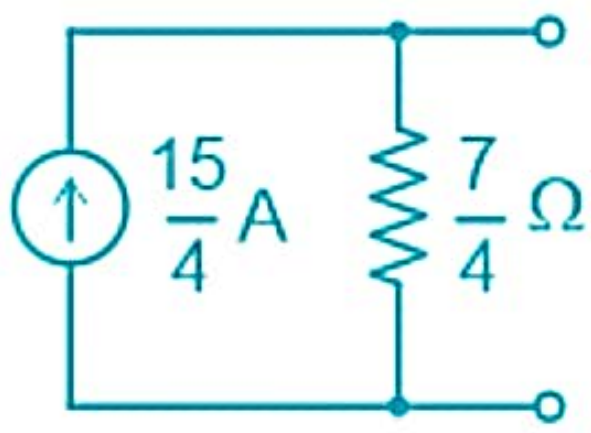
Was this solution helpful?

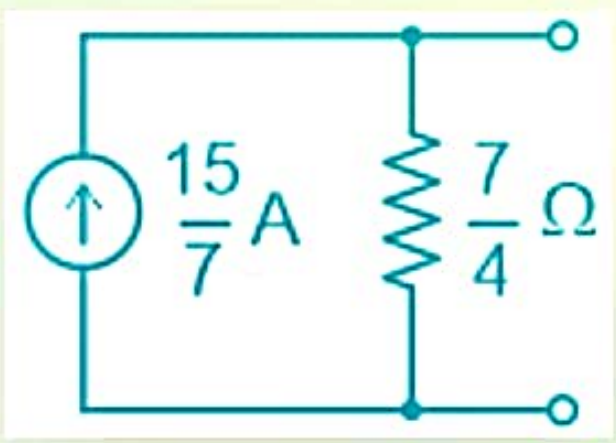
Hide Solution

Reattempt Mode

Simplify circuit given below into current source -

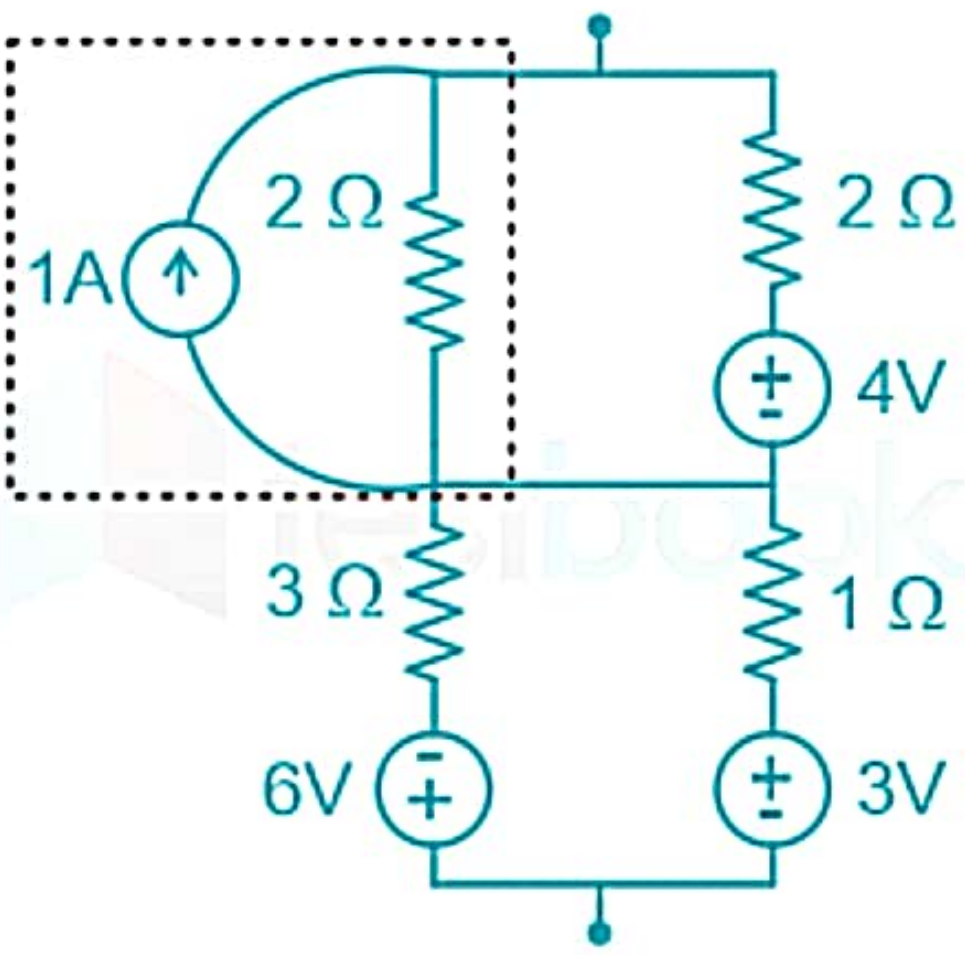


1. 

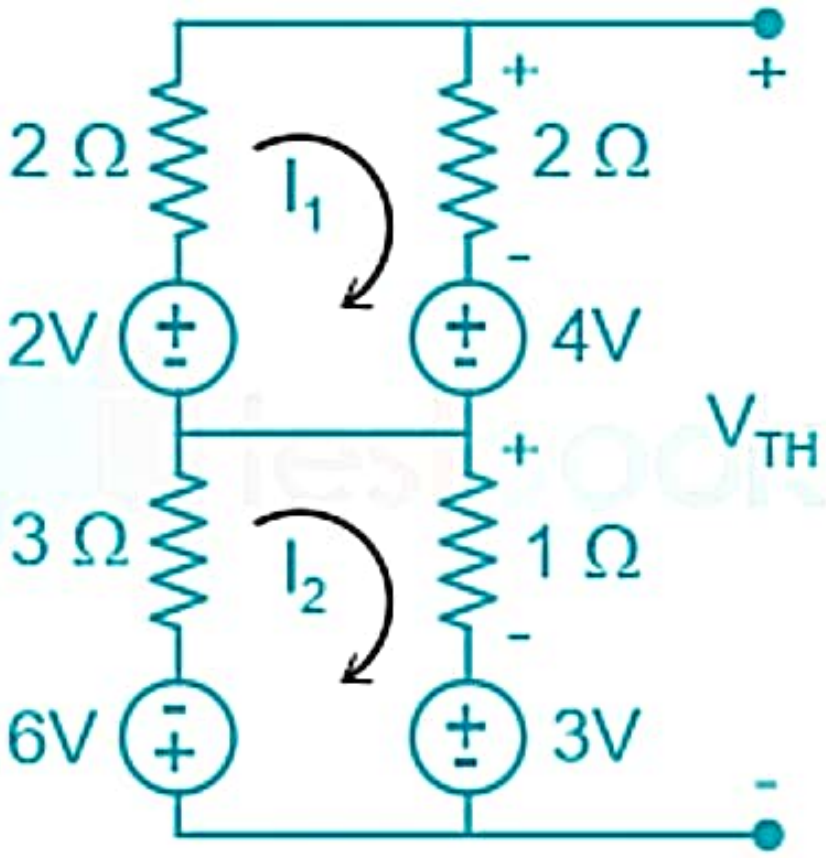
2. 

Reattempt Mode

Use source transformation in dotted region



The circuit can be redrawn as



Calculation of V_{TH}:

$I_1 = (2-4)/(2+2) = -(1/2)$ A

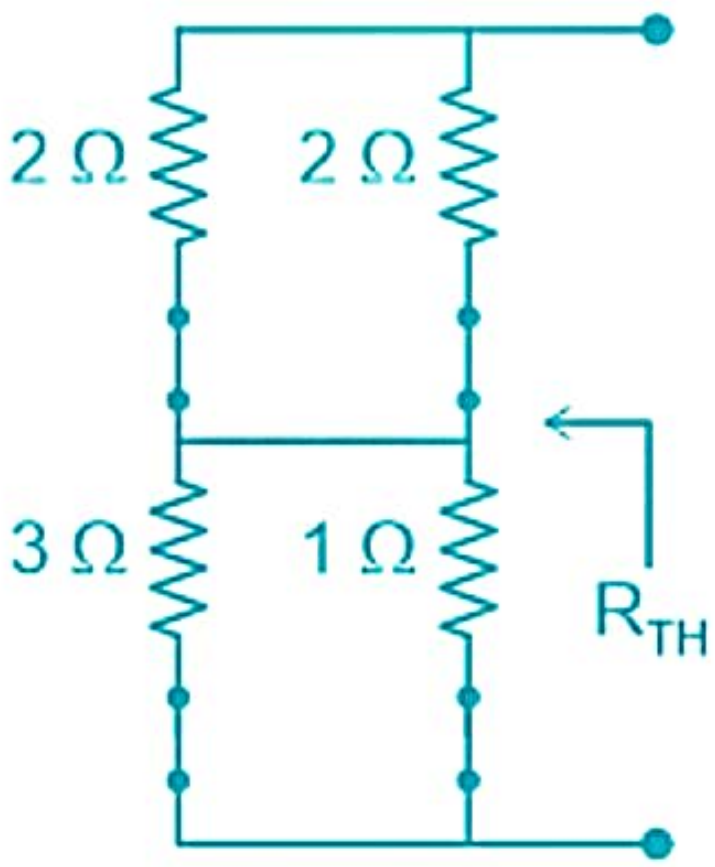
$I_2 = (-6 - 3)/(3 + 1) = -(9/4)$ A

$V_{TH} = 2I_1 + 4 + I_2 + 3 = (2 \times -1/2) + 4 + (-9/4) + 3 = 15/4$ V or 3.75 V

$I_2 = (-6 - 3)/(3 + 1) = -(9/4)$ A

$V_{TH} = 2I_1 + 4 + I_2 + 3 = (2 \times -1/2) + 4 + (-9/4) + 3 = 15/4$ V or 3.75 V

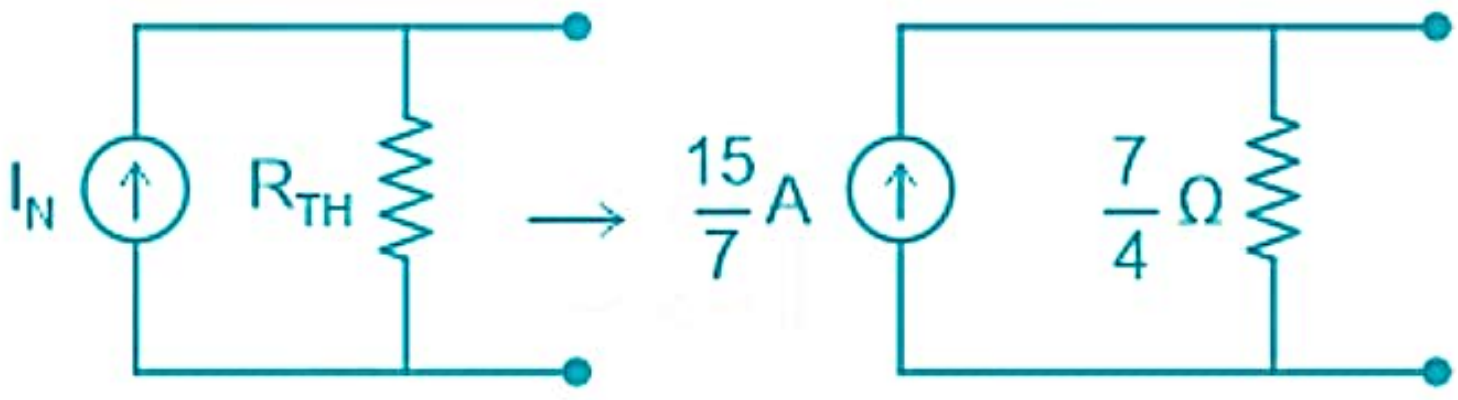
Calculation of R_{TH}:



$R_{TH} = (2||2) + (3||1) =$ **7/4 Ω**

$I_N = V_{TH} / R_{TH} = (15/4)/(7/4) =$ **15/7 A**

Norton equivalent circuit:



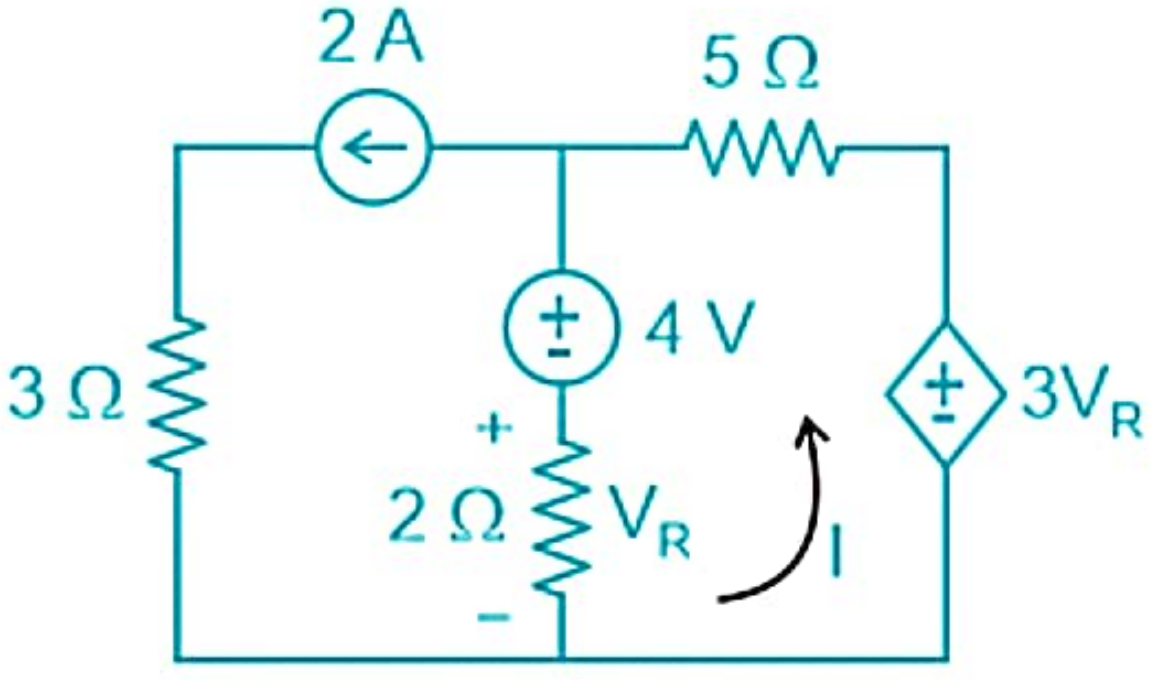
Was this solution helpful?

Hide Solution

Reattempt Mode

4 3sec | +1.0 -0.33

Obtain the current 'I' in the network shown below -



1. I = −12 A ✓

2. I = −9 A

3. I = 12 A ✗

4. I = 9 A

Correct Answers Is: 1

47% got this right

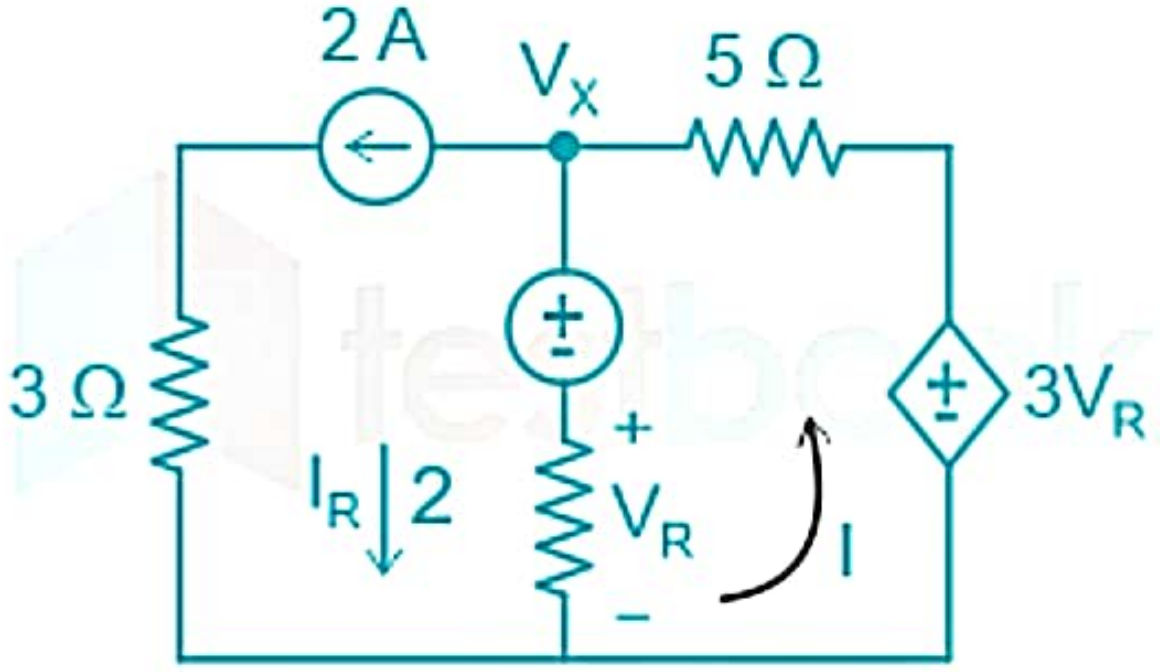
Reattempt Mode

Concept:

Nodal analysis is a method that provides a general procedure for analyzing circuits using node voltages as the circuit variables. Nodal Analysis is also called the **Node-Voltage Method.**

Nodal Analysis is based on the application of Kirchhoff's Current Law (KCL).

Calculation:



Use Nodal analysis at the node $\mathbf{V_X}$

$$2 + (V_R/2) + (V_X - 3V_R)/5 = 0$$

$$\Rightarrow 2 + (V_R/2) + (4 + V_R - 3V_R)/5 = 0 \ [\because V_X = 4 + V_R]$$

$$\Rightarrow 2 + (V_R/2) + (4 - 2V_R)/5 = 0$$

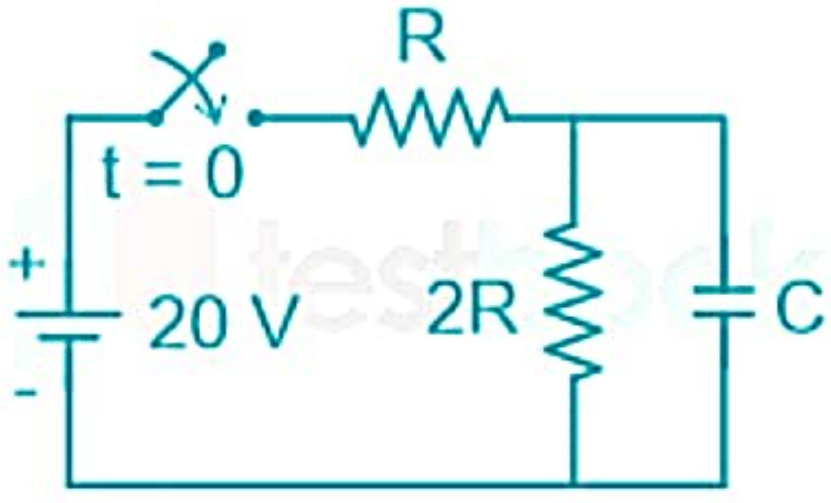
$$\Rightarrow V_R = -28 \text{ V}$$

$$I_R = V_R/2 = -28/2 = -14 \text{ A}$$

$$I = 2 + I_R = 2 + (-14) = \mathbf{-12\ A}$$

5 42sec | +1.0 -0.33

The time constant of the network shown in the figure below is



1. 2RC

2. 3RC

3. $\frac{RC}{2}$

4. $\frac{2RC}{3}$ ✓

Correct Answers Is: 4 76% got this right

7 25sec | +1.0 -0.33

Which of the following conditions holds good for a 2-port network to be reciprocal?

1. $Z_{11} = Z_{22}$

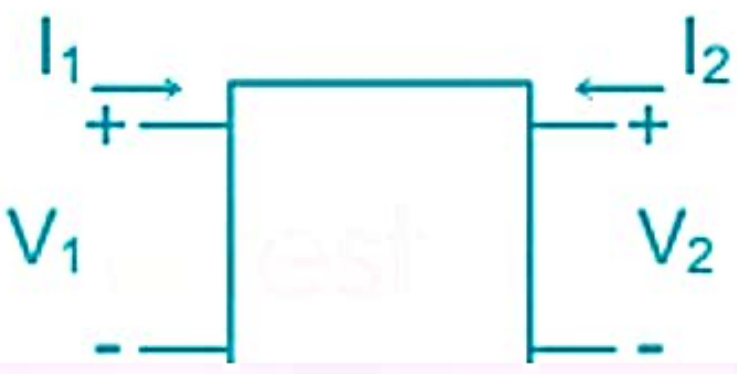
2. $H_{12} = H_{21}$

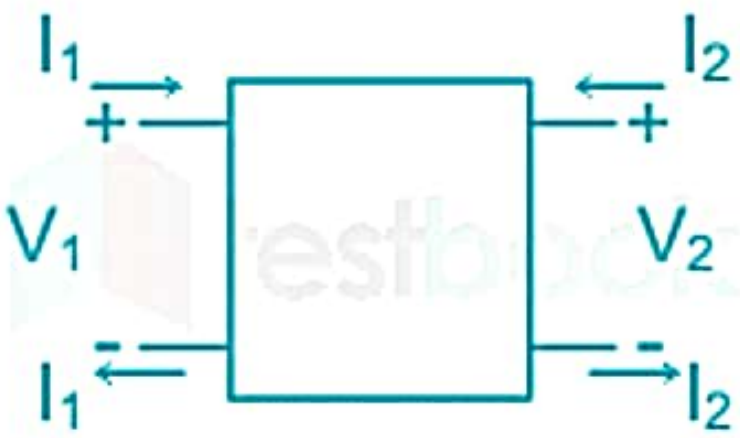
3. $Y_{12} = -Y_{21}$ ✗

4. $BC - AD = -1$ ✓

Correct Answers Is: 4 57% got this right

SOLUTION



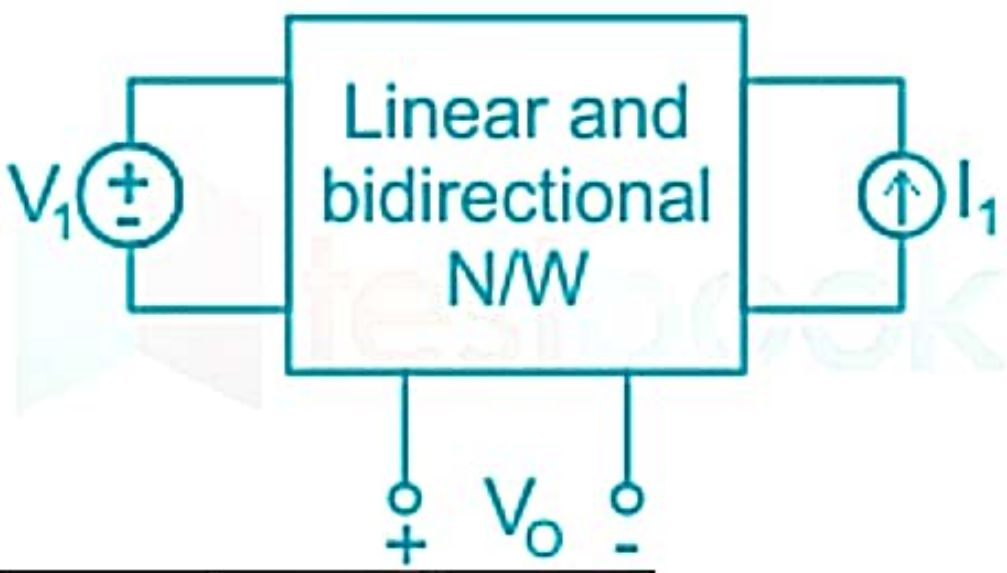


A network is said to be reciprocal if the voltage appearing at port 2 due to a current applied at port 1 is the same as the voltage appearing at port 1 when the same current is applied to port 2.

Two Port Parameters	Condition for Symmetry	Condition for Reciprocal
Z Parameters	$Z_{11} = Z_{22}$	$Z_{12} = Z_{21}$
Y parameters	$Y_{11} = Y_{22}$	$Y_{12} = Y_{21}$
ABCD parameters	A = D	$\Delta T = AD - BC = 1$
H parameters	$\Delta h = h_{11}h_{22} - h_{12}h_{21} = 1$	$h_{12} = -h_{21}$

8 4min 19sec | +2.0 -0.66

In the network given below, the output voltage V_o, when V_1 and I_1 are 10 V and 8 A respectively is:



V_1	I_1	V_0
5V	0A	3V
0V	2A	6V

1. 10 V

2. 30 V ✓

3. 24 V

Reattempt Mode

Correct Answers Is: 2 45% got this right

SOLUTION

The voltage V_0 is contributed by the two sources present in the network.

$\therefore$ Let $V_0 = \alpha V_1 + \beta I_1$

Case 1: $V_1 = 5$ V, $I_1 = 0$ A, $V_0 = 3$ V

$V_0 = \alpha V_1 + \beta I_1$

$\Rightarrow 3 = 5\alpha$

$\Rightarrow \alpha = 0.6$

Case 2: $V_1 = 0$ V, $I_1 = 2$ A, $V_0 = 6$ V

$V_0 = \alpha V_1 + \beta I_1$

$\Rightarrow 6 = 0 + 2\beta$

$\Rightarrow \beta = 3$

$V_0 = 0.6\, V_1 + 3\, I_1$

Now, $V_1 = 10$ V, $I_1 = 8$ A

$V_0 = 0.6\,(10) + 3\,(8) = 30$ V

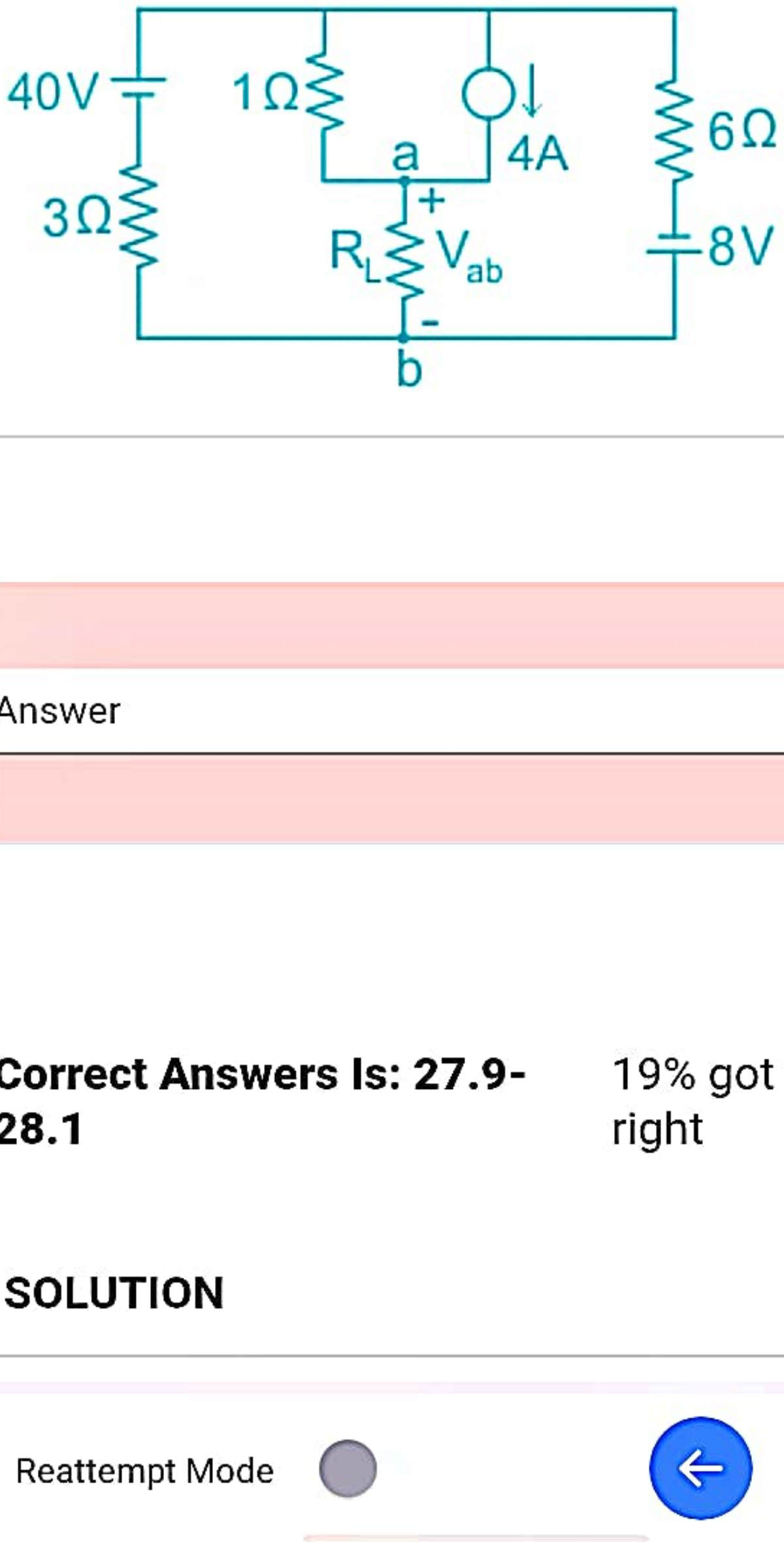
Was this solution helpful?

Hide Solution

Reattempt Mode

10 2sec | +2.0 -0.0

The Thevenin equivalent voltage, V_{th}, in V across the load resistance (R_L) of the network shown below, is _____



Answer

Correct Answers Is: 27.9-28.1

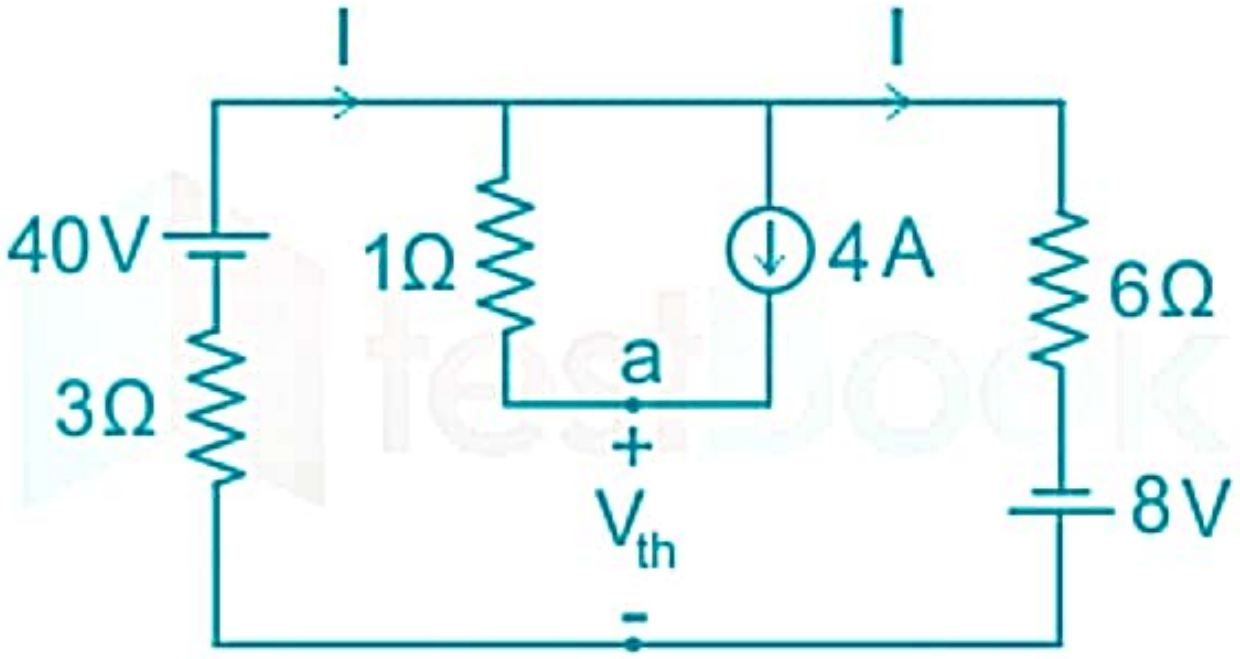
19% got this right

SOLUTION

Reattempt Mode

SOLUTION

By open circuiting the load terminals to evaluate the open circuit Thevenin voltage, the circuit becomes:



By applying KVL in the outer loop, we can write:

$40 - 6I + 8 - 3I = 0$

$$I = \frac{48}{9} = \frac{16}{3}\ A$$

Since 4 A of current will flow across the 1 Ω resistance, by applying KVL to the left side of the circuit, we can write:

$$40 + 4 \times 1 - V_{th} - 3 \times \frac{16}{3} = 0$$

$40 + 4 - V_{th} - 16 = 0$

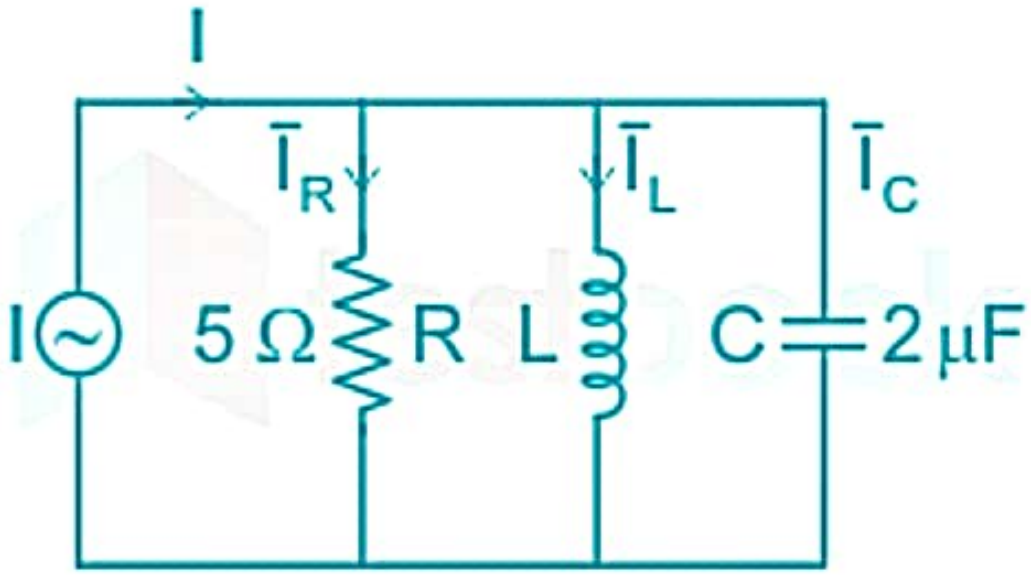
$V_{th} = 28$ V

Was this solution helpful?

Reattempt Mode

15 1sec | +2.0 -0.0

For the parallel RLC circuit given below, the magnitudes of currents I_L and I_C are four times that of I_R.



The value of the inductance L is _____ (in μH)

Answer

Correct Answers Is: 3.1-3.2 22% got this right

SOLUTION

Reattempt Mode

Correct Answers Is: 3.1-3.2 22% got this right

SOLUTION

$|I_L| = |I_C| = 4\, I_R$

$\bar{I}_L$ and $\bar{I}_C$ are equal in magnitude and opposite in phase, $\bar{I}_L + \bar{I}_C = 0$

$\Rightarrow \bar{I} = \bar{I}_R$

Therefore, the circuit is working under the resonance condition.

Quality factor, $Q_o = \frac{|I_L|}{|I_R|} = \frac{4|I_R|}{|I_R|} = 4$

For a parallel RLC circuit, the quality factor is

$$Q = R\sqrt{\frac{C}{L}}$$

From the given circuit diagram,

R = 5 Ω, C = 2 μF

$$\Rightarrow 4 = 5\sqrt{\frac{2\times10^{-6}}{L}}$$

$\Rightarrow$ L = 3.125 μH

Was this solution helpful?

1 20sec | +1.0 -0.33

In a 4-stage ripple counter, the propagation delay of a flip-flop is 100 ns. For a pulse width of the strobe as 100 ns, the maximum frequency at which the counter operates reliably is?

1. 1 MHz

2. 2 MHz ✓

3. 500 MHz

4. 0.5 MHz

Correct Answers Is: 2 46% got this right

SOLUTION

For a n stage ripple counter the time period of clock is given by

4. 0.5 MHz

Correct Answers Is: 2 46% got this right

SOLUTION

For a n stage ripple counter the time period of clock is given by

$T_{CLK} \geq n\, t_{pd}$

$T_{CLK} \geq 4(100)$

$T_{CLK} \geq 400$ nsec

$$f_{CLK} \leq \frac{1}{400} \times 10^9$$

$$f_{CLK} \leq 2.5\ \mathbf{MHz}$$

Hence from given options, the maximum frequency at which the counter operates reliably is 2 MHz

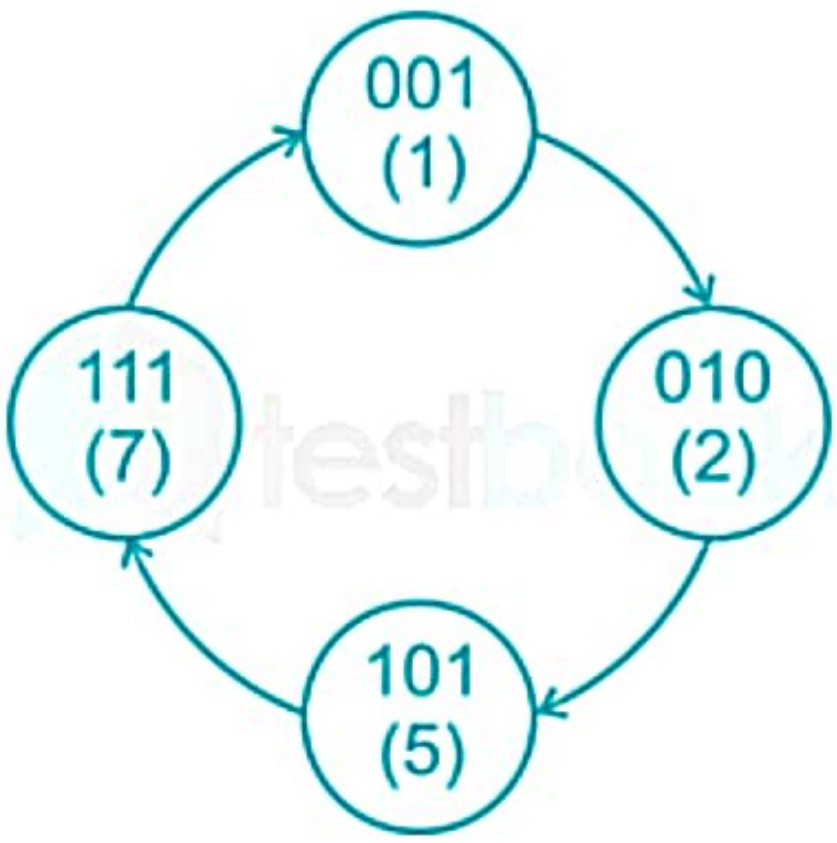
Was this solution helpful?

Hide Solution

Reattempt Mode

2 27sec | +1.0 -0.0

The minimum number of flip flops required to implement the following state diagram which has 4 valid states.



Answer

Correct Answers Is: 3-3 58% got this right

SOLUTION

Reattempt Mode

Answer

Correct Answers Is: 3-3 58% got this right

SOLUTION

The state diagram shown in the figure has only four states. But a 3-bit counter is required to implement this sequence because the maximum binary count is seven.
So, number of flip flops required = 3

Was this solution helpful?

Hide Solution

Reattempt Mode

4 9sec | +1.0 -0.33

Three T flip flops are connected to form a counter. The maximum states possible for the counter will be:

1. 5

2. 3

3. 8 ✓

4. 7

Correct Answers Is: 3 72% got this right

SOLUTION

Concept:

For a counter with 'n' flip flops:

- The total number of states = 2^n (0 to 2^n –

Concept:

For a counter with 'n' flip flops:

- The total number of states = 2^n (0 to $2^n - 1$)
- The largest number that can be stored in the counter = $2^n - 1$

To construct a counter with any MOD number, the minimum number flip flops required must satisfy:

Modulus ≤ 2^n

Where n is the number of flip-flops and is the minimum value satisfying the above condition.

Calculation:

The total number of states required when n = 3:

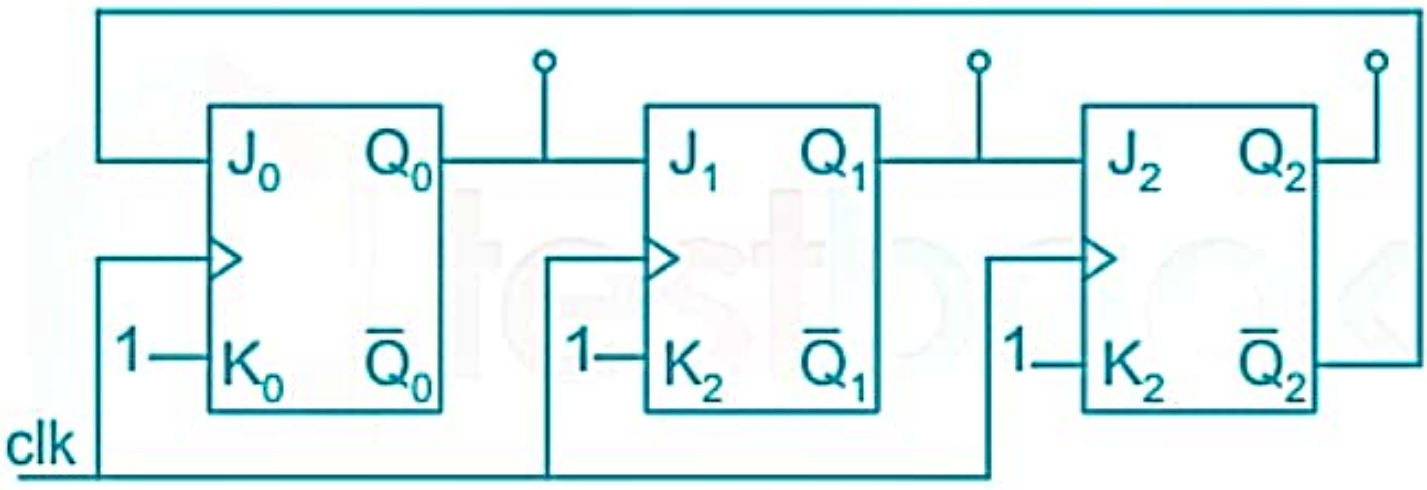
$2^3 \geq 8$

The states will vary from **(0 to 7)**

So the maximum states possible for the counter will be 8.

5 0sec | +0.0 -0.0

Consider the sequential circuit given below.



If the initial state of the flip-flops $Q_0\ Q_1\ Q_2$ is 101, which of the following is/are true?

*This question may have multiple correct answers

1. The modulus of the counter is 3

2. The value of $Q_0\ Q_1\ Q_2$ after 6 clock pulses is 101 — You missed this answer

3. The value of $Q_0\ Q_1\ Q_2$ after 5 clock pulses is 010 — You missed this answer

4. Number of unused states are 5

Reattempt Mode

4. Number of unused states are 5

Correct Answers Is: 2, 3 43% got this right

SOLUTION

From the given, sequential circuit,
$J_o = \bar{Q}_2$bar, $J_1 = Q_0$, $J_2 = Q_1$

Clock pulse	Q_0 Q_1 Q_2	J_0 K_0	J_1 K_1	J_2 K_2
Initial	1 0 1	0 1	1 1	0 1
1	0 1 0	1 1	0 1	1 1
2	1 0 1			

After two clock pulses, it reaches its initial value. ∴ The Modulus of the counter will be 2.
Number of unused states = 8 − 2 = 6
After 5^{th} clock pulse, Q_0 Q_1 Q_2 = 0 1 0
After 6^{th} clock pulse, Q_0 Q_1 Q_2 = 1 0 1

6 3sec +2.0 -0.0

For the multistage counter arrangement of the given figure, determine the frequency of the output signal in Hz.

Answer

Correct Answers Is: 125-125 23% got this right

SOLUTION

Input frequency = 1 MHz.

4-bit binary ripple counter has 2^4 = 16 states

Now, the frequency =

$$\frac{1\times10^6}{16} = 62.5 \times 10^3\, Hz$$

Answer

Correct Answers Is: 125-125 23% got this right

SOLUTION

Input frequency = 1 MHz.

4-bit binary ripple counter has $2^4 = 16$ states

Now, the frequency =

$\frac{1\times10^6}{16} = 62.5 \times 10^3\, Hz$

5-bit ring counter has 5 states.

Now, the frequency = . $\frac{62.5\times10^3}{5} = 12.5\ kHz$

BCD counter has 10 states

Now, the frequency = $\frac{12.5\times10^3}{10} = 1250\ Hz$

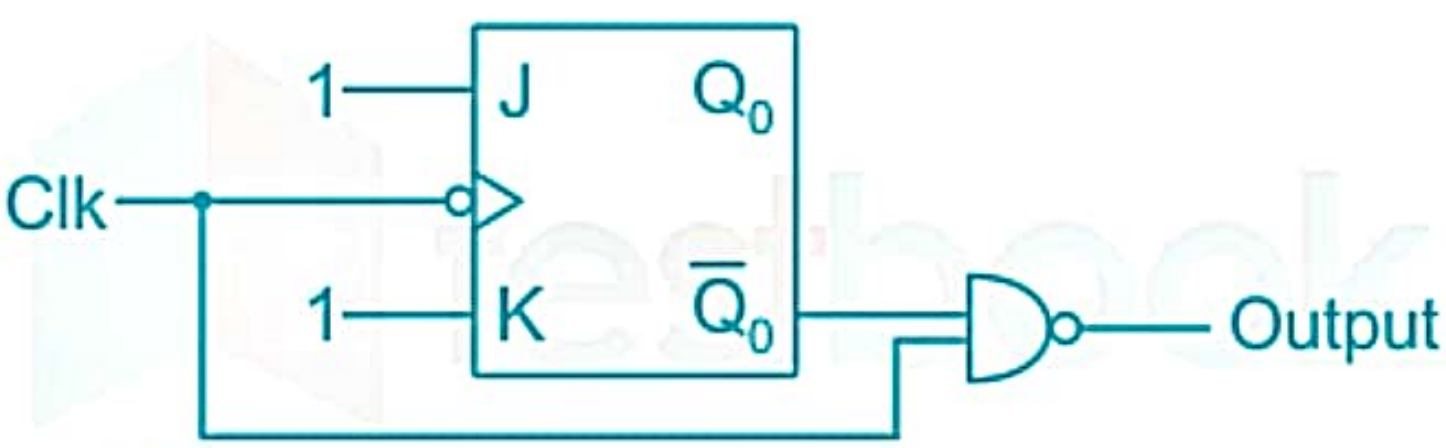
5-bit Johnson counter has 2 × 5 = 10 states.

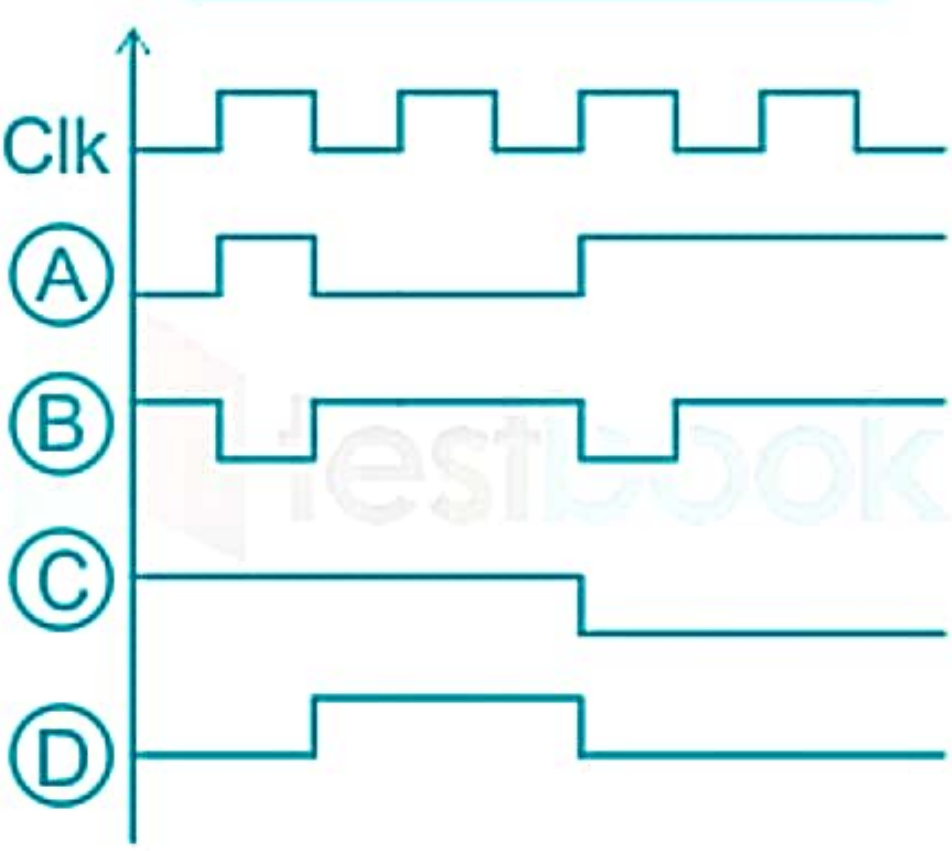
The output frequency = $\frac{1250}{10} = 125\ Hz$

Was this solution helpful?

7 2min 25sec | +2.0 -0.33

The propagation delay of flip-flop and logic is zero, which of the following will be the waveform of output If Q_0 is reset to '0'





1. A

2. B ✓

Reattempt Mode

Concept:

Characteristic table of JK flip flop:

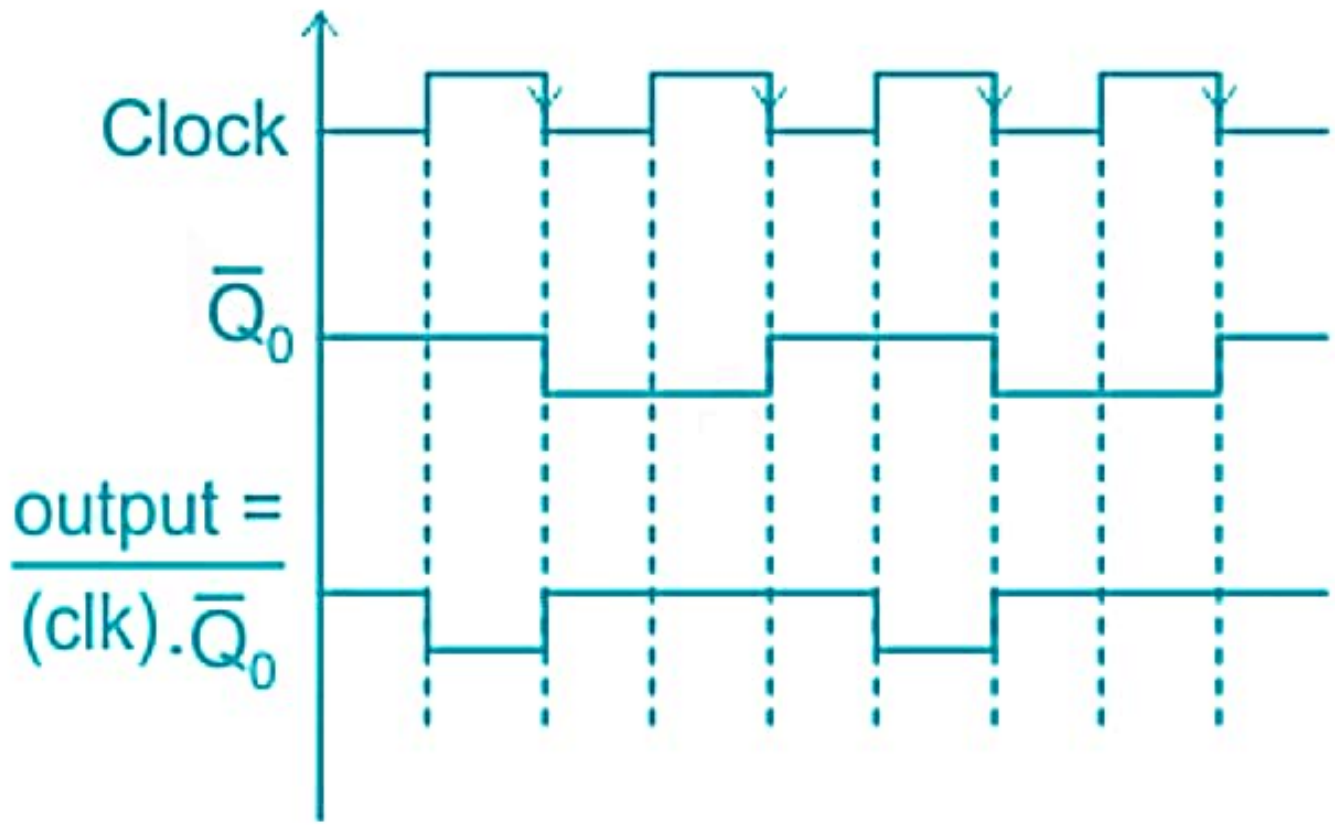
J	K	Q_{n+1}
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

Truth Table of NAND gate:-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

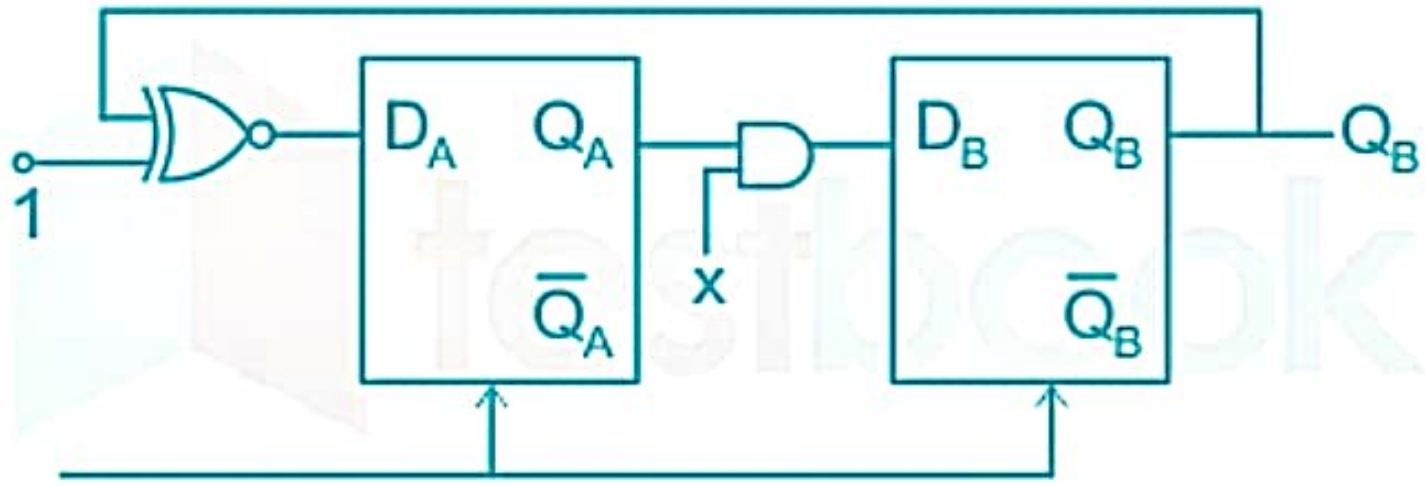
Analysis:-

From the circuit diagram, it is clear that the applied clock is a negative edged Trigger. Since, J = K = 1, the Next state will always be the complement to its previous state.



8 0sec | +0.0 -0.0

A finite state machine with 4 possible states as 00, 01, 10, and 11 are implemented using two D Flip flops (Q_A is the MSB and Q_B is the LSB). The FSM is initialized to states 00, and the input x is constant throughout the operation.



Which of the following statements is/are true?

This question may have multiple correct answers

1. The FSM produces all possible states when x is 0.

2. The FSM produces all possible states when x is 1. !

You missed this answer

3. The FSM produces 3 possible states when x is 0.

Reattempt Mode

$D_A = Q_B \odot 1$

$D_B = Q_A x$

We will take two conditions for x, that is when x = 0 and when x = 1

x = 0

Q_A	Q_B	D_A	D_B	Q_A^+	Q_B^+
0	0	0	0	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	1	1	0	1	0

∴ When x = 0, we can have only two out of the four possible states.

x = 1

Q_A	Q_B	D_A	D_B	Q_A^+	Q_B^+
0	0	0	0	0	0
0	1	1	0	1	0
1	0	0	1	0	1
1	1	1	1	1	1

∴ When x = 1, we can have all four possible states.