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## **Department of Electronics & Telecommunication Engineering**

# Mini Project To Realize 4-Bit binary Sequence Using 8086 Trainer Kit

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### **CERTIFICATE**

This is to certify that M/S	<b></b>
SAP ID	_ of TE EXTC 1: has submitted their
Mini Project for MPP for th	e Academic Year 2018-2019.
Guide	Examiner
	Head of Department
	EXTC Department

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### Aim:

To realize the generation of 4 bit binary sequence using 8086 microprocessor and also using 8255 PPI and write a program to display the sequence with the use of LED's.

## Theory:

The 8255 is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.

It consists of three 8-bit bidirectional I/O ports (24I/O lines) which can be configured as per the requirement.

#### Ports of 8255A

8255A has three ports, i.e., PORT A, PORT B, and PORT C.

**Port A** contains one 8-bit output latch/buffer and one 8-bit input buffer.

**Port B** is similar to PORT A.

**Port** C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

#### **Operating Modes**

8255A has three different operating modes –

**Mode 0** – In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.

**Mode 1** – In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as handshake signals. Inputs and outputs are latched.

**Mode 2** – In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals

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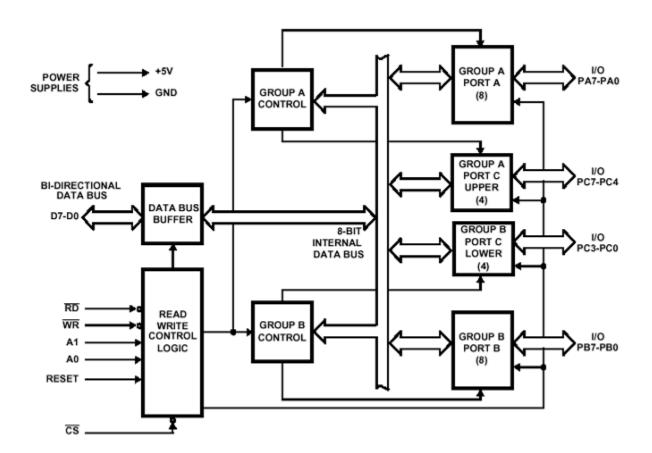
from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

#### Features of 8255A

The prominent features of 8255A are as follows – It consists of 3 8-bit IO ports i.e. PA, PB, and PC. Address/data bus must be externally demux'd. It is TTL compatible. It has improved DC driving capability.

#### 8255 Architecture

The following figure shows the architecture of 8255A –



Software Used: Tasm / debug

**Hardware Used:** 8086 trainer kit, FRC cables, 4 LED's,  $10k\Omega$  resistor, connecting wires.

SUBJECT TITLE: MPP SUBJECT CODE:ECL501 SEMESTER V

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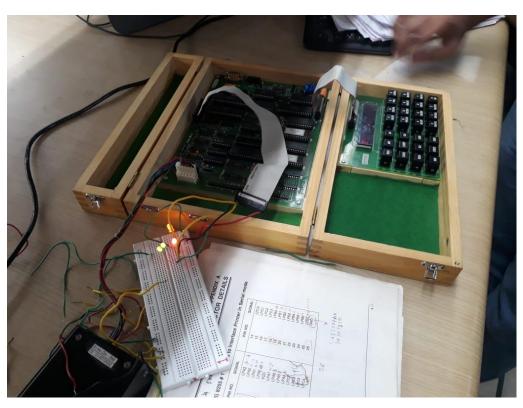
## **Overview:**

PA0,PA1,PA2,PA3 are connected to the 4LED's and PC0 is either connected to Vcc(+5V) or Ground.

## **Procedure:**

- 1) Initialize the 8255 PPI; configure port A as a output port in mode 0.
- 2) Insert the code for 4-bit binary sequence generation.
- 3) Connect 4 LEDs for displaying output sequence.
- 4) Introduce necessary delay
- 5) Execute the code.

## **Circuit Diagram:**



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## Code:

Address	OP code	Mnemonics	Data
2000:0100	B089	MOV	AL,89
2000:0102	E666	OUT	66,AL
2000:0104	B10F	MOV	CL,0F
2000:0106	E464	IN	AL,64
2000:0108	3C01	CMP	AL,01
2000:010A	7410	JZ	011C
2000:010C	B00F	MOV	AL,0F
2000:010E	E660	OUT	60,AL
2000:0110	BAFFFF	MOV	DX,FFFF
2000:0113	4A	DEC	DX
2000:0114	75FD	JNZ	0113
2000:0116	FEC8	DEC	AL
2000:0118	FEC9	DEC	CL
2000:011A	75F2	JNZ	010E
2000:011C	B0000	MOV	AL,00
2000:011E	E660	OUT	60,AL
2000:0120	BAFFFF	MOV	DX,FFFF
2000:0123	4A	DEC	DX
2000:0124	75FD	JNZ	0123
2000:0126	FEC0	INC	AL
2000:0128	FEC9	DEC	CL
2000:012A	75F2	JNZ	011E
2000:012C	EB02	JMP	0100
2000:012E	F4	HLT	

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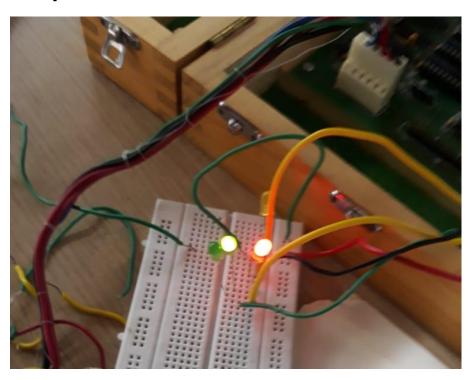
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## **Output:**



## **Conclusion:**

We have successfully realized sequence generation using 8086 trainer kit using LED's.

When PC0 is connected to Vcc the sequence is in increasing order and when connected to ground the sequence is in decreasing order.

Here 1 represents LED to be ON and 0 is when LED is OFF.

PC0 is connected to Vcc	PC0 is connected to ground	
0000	1111	
0001	1110	
0010	1101	
0011	1100	
1111	0000	

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## **References:**

- https://nptel.ac.in/courses/Webcourse-contents/IISc-BANG/Microprocessors%20and%20Microcontrollers/pdf/Teacher Slides /mod1/M1L3.pdf
- 2. Microprocessors and Interfacing 3<sup>rd</sup> edition by Douglas V Hall and SSSP Rao.
- 3. <a href="http://faculty.kfupm.edu.sa/COE/shazli/coe305/part2-expr03.pdf">http://faculty.kfupm.edu.sa/COE/shazli/coe305/part2-expr03.pdf</a>

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