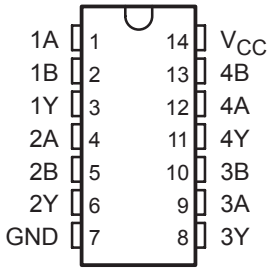
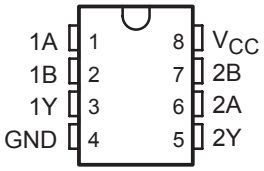
- **Package Options Include Plastic Small-Outline (D, NS, PS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**
- **Also Available as Dual 2-Input Positive-NAND Gate in Small-Outline (PS) Package**

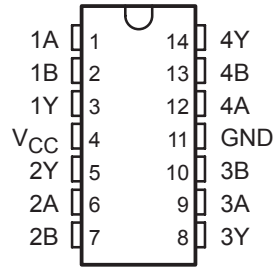
**SN5400 . . . J PACKAGE**
**SN54LS00, SN54S00 . . . J OR W PACKAGE**
**SN7400, SN74S00 . . . D, N, OR NS PACKAGE**
**SN74LS00 . . . D, DB, N, OR NS PACKAGE**
**(TOP VIEW)**



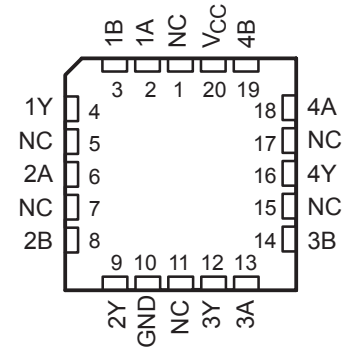

**SN74LS00, SN74S00 . . . PS PACKAGE**
**(TOP VIEW)**




**SN5400 . . . W PACKAGE**
**(TOP VIEW)**




**SN54LS00, SN54S00 . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

These devices contain four independent 2-input NAND gates. The devices perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.