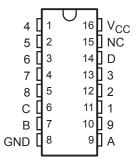
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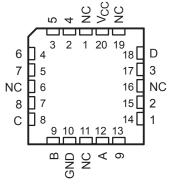
'147, 'LS147

- Encode 10-Line Decimal to 4-Line BCD
- Applications Include:
 - Keyboard Encoding
 - Range Selection

SN54147, SN54LS147 . . . J OR W PACKAGE SN74147, SN74LS147 . . . D OR N PACKAGE (TOP VIEW)



SN54LS147 . . . FK PACKAGE (TOP VIEW)

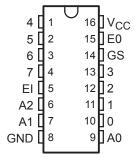


NC - No internal connection

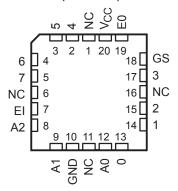
'148, 'LS148

- Encode 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
 - n-Bit Encoding
 - Code Converters and Generators

SN54148, SN54LS148 . . . J OR W PACKAGE SN74148, SN74LS148 . . . D, N, OR NS PACKAGE (TOP VIEW)



SN54LS148 . . . FK PACKAGE (TOP VIEW)



TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION				
'147	10 ns	225 mW				
'148	10 ns	190 mW				
'LS147	15 ns	60 mW				
'LS148	15 ns	60 mW				

NOTE: The SN54147, SN54LS147, SN54148, SN74147, SN74LS147, and SN74148 are obsolete and are no longer supplied.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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description/ordering information

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 devices encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 devices encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input El and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54/74LS load, respectively.

ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP - N	Tube	SN74LS148N	SN74LS148N	
0°C to 70°C	0010 0	Tube	SN74LS148D	LS148	
	SOIC - D	Tape and reel	SN74LS148DR		
	SOP - NS	Tape and reel	SN74LS148NSR	74LS148	
−55°C to 125°C	CDIP - J	Tube	SNJ54LS148J	SNJ54LS148J	
	CFP - W	Tube	SNJ54LS148W	SNJ54LS148W	
	LCCC - FK	Tube	SNJ54LS148FK	SNJ54LS148FK	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE - '147, 'LS147

INPUTS								OUTPUTS				
1	2	3	4	5	6	7	8	9	D	С	В	Α
Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н
X	Χ	Χ	Χ	Χ	Χ	Χ	Χ	L	L	Н	Н	L
X	Χ	Χ	Χ	Χ	Χ	Χ	L	Н	L	Н	Н	Н
Х	Χ	Χ	Χ	Χ	Χ	L	Н	Н	Н	L	L	L
Х	Χ	Χ	Χ	Χ	L	Н	Н	Н	Н	L	L	Н
Х	Χ	Χ	Χ	L	Н	Н	Н	Н	Н	L	Н	L
Х	Χ	Χ	L	Н	Н	Н	Н	Н	Н	L	Н	Н
Х	Χ	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L
Х	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

H = high logic level, L = low logic level, X = irrelevant

SN54147, SN54148, SN54LS147, SN54LS148 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS SDLS053B - OCTOBER 1976 - REVISED MAY 2004

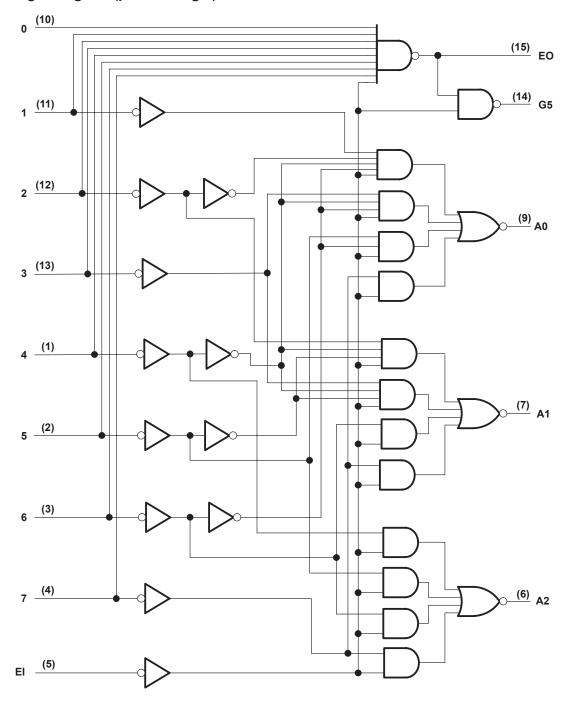
FUNCTION TABLE - '148, 'LS148

INPUTS						OUTPUTS							
EI	0	1	2	3	4	5	6	7	A2	A 1	A0	GS	EO
Н	Х	Х	Χ	Χ	Х	Χ	Χ	Х	Н	Н	Н	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
L	Х	Χ	Χ	Χ	X	Χ	Χ	L	L	L	L	L	Н
L	Х	Χ	Χ	Χ	Χ	Χ	L	Н	L	L	Н	L	Н
L	Х	Χ	Χ	Χ	Χ	L	Н	Н	L	Н	L	L	Н
L	Х	Χ	Χ	Χ	L	Н	Н	Н	L	Н	Н	L	Н
L	Х	Χ	Χ	L	Н	Н	Н	Н	Н	L	L	L	Н
L	Х	Χ	L	Н	Н	Н	Н	Н	Н	L	Н	L	Н
L	Х	L	Н	Н	Н	Н	Н	Н	Н	Н	L	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н

H = high logic level, L = low logic level, X = irrelevant

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'148, 'LS148 logic diagram (positive logic)



Pin numbers shown are for D, J, N, NS, and W packages.

