Nwatu Victor Praise

40206992

1. First four iterations: 3 misses
   Second four iterations: 8 misses
   First four iterations: 8 misses
   First four iterations: 1 miss

2. A. T_AVE = ht + mr * mp * mem_avg
   = 1.5 + (0.06 * 12) * 1/3
   = 1.5 + 0.24
   = 1.74 clock cycles per instructions

   B. = base_cpi + (L1_mr * L1_mp + L1_mr(L2_mr * L2_mp)) * 1/3

   = 1.5 + (0.15 * 10 + 0.15(0.05 * 80)) * 1/3

   = 2.2 clock cycles per instructions

3. A. cache size = 6 + 19 = 25
   = 2^25
   B. cache mapping scheme is direct mapping
   C. 2^15

4. 8k = 2^13 frames

   Index = 13bits

   16words = 2^4 words

   Offset = 4bits

   Tag = 32 – 13 + 4 = 15bits

   Word address 45d7e5ba to binary =

   [0100 0101 1101 0111 1110 0101 1011 1010]

   Tag value = [010001011101011]

   Converting to hexadecimal with binary extensions

   Tag value = [45d]011

   Cache frame = [1111001011011]

   Converting to hexadecimal with binary extensions

   Cache frame = [f2d]1

5. Concurrency = latency * bandwidth

5A. Average concurrency in pipeline = 1.75 * 100 = 175 arrows

5B. Latency = 85/100 = 0.85 arrows per cycle

Since maximum input bandwidth is 2arrows per cycle, the concurrency becomes a bottle neck when the latency(input bandwidth) exceeds 2 arrows per cycle

5C. Regular supplier concurrency = 0.95 * 100 = 95 arrows

Demand-driven concurrency = 1.79 * 100 = 179 arrows

Regular supplier provides 95 arrows, however if we require more arrows, the demand driven supplier will be accessed. Since the maximum concurrency is 200 arrows, bottleneck is achieved when Demand driven supplier supplies more than 105 arrow.