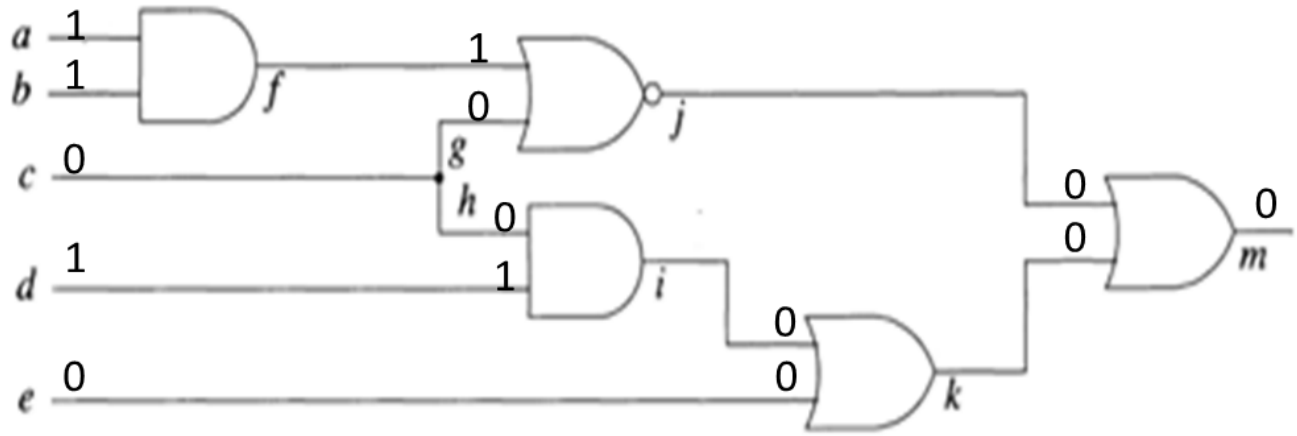
5.3 For the circuit and the fault set used in Example 5.1, determine the faults detected by the test 11010 by deductive simulation.



Given the circuit above, and the collapsed fault list (see Example 4.8) $\{a_0,a_1,b_1,c_0,c_1,d_1,e_0,g_0,h_0,h_1\}$ determine the faults detected by 11010 by deductive simulation.

☆ Remember:

$$if\ C = \emptyset\ then\ L_z = \left\{\bigcup_{j\in I} L_j\right\} \bigcup \{Z_{s-a-(c\oplus i)}\}$$

$$else\ L_z = \left(\left\{\bigcap_{j\in C} L_j\right\} - \left\{\bigcup_{j\in I-C} L_j\right\}\right) \bigcup \{Z_{s-a-(\bar{c}\oplus i)}\}$$

Comparing the collapsed fault list with the input vector we have:

$L_a = \{a_0\}$

$L_b = \{\emptyset\}$

$L_c = \{c_1\}$

$L_d = \{\emptyset\}$

$L_e = \{\emptyset\}$

Apply ☆ to the AND gate, f:

$$L_f = L_a \bigcup L_b \bigcup \{f_{s-a-0}\} = L_a \bigcup L_b = \{a_0\} \bigcup \emptyset = \{a_0\}$$

Not in fault list

$L_g = \{c_1\}$

$L_h = \{c_1, h_1\}$

Apply ☆ to the NOR gate, j:

$$L_j = (L_f - L_g) \bigcup \{j_{s-a-(0 \oplus 1)}\} = \{a_0\} - \{c_1\} = \{a_0\}$$

Not in fault list

Apply ☆ to the AND gate, i:

$$L_i = L_h - L_d \bigcup \cancel{\{i_{s-a-(1\oplus 0)}\}} = L_h - L_d = \{c_1, h_1\} - \emptyset = \{c_1, h_1\}$$

Not in fault list

Apply ☆ to the OR gate, k:

$$L_k = L_i \bigcup L_e \bigcup \cancel{\{k_{s-a-(1\oplus 0)}\}} = L_i \bigcup L_e = \{c_1, h_1\} \bigcup \emptyset = \{c_1, h_1\}$$

Not in fault list

Finally, apply ☆ to the OR gate, m:

$$L_m = L_j \bigcup L_k \bigcup \cancel{\{m_{s-a-(1\oplus 0)}\}} = L_j \bigcup L_k = \{a_0\} \bigcup \{c_1, h_1\} = \{a_0, c_1, h_1\}$$

Not in fault list

∴ a_0 ,c_1, h_1 are detected!

5.5 For the latch shown in Figure 5.36, assume $\bar{y} = 0$, $y = 1$, and $S = R = 1$. Assume the initial fault lists associated with lines y, $\bar{y}$, R and S are L_y, $L_{\bar{y}}$, L_R, and L_S. Let S change to a 0. Determine the new output fault lists in terms of the given fault lists produced by this input event. Also, include all s-a-faults associated with this circuit.

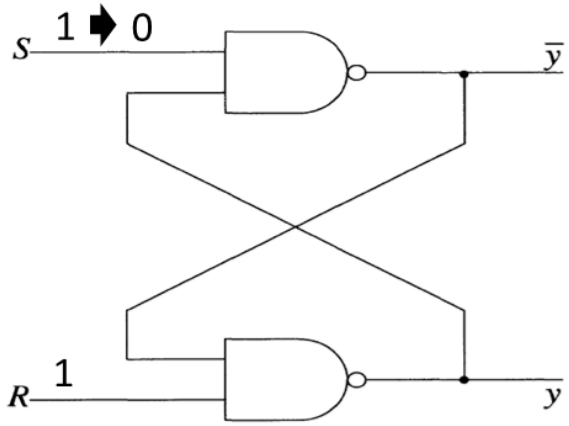


Figure 5.36

Assume the initial values:

$\bar{y} = 0 \quad y = 1 \quad S = 1 \quad R = 1$

Assume the initial fault lists:

$L_y, \quad L_{\bar{y}}, \quad L_R, \quad L_S$

Let S➡0, then find the new output fault list.

First determine the correct (fault-free) behavior:

	Initial State	T=0	T=1	T=2	T=3	T=4
S	1	0	0	0	0	0
R	1	1	1	1	1	1
$\bar{y}$	0	0	1	1	1	1
y	1	1	1	0	0	0

Next, apply ☆ for 2-input NAND gate

(Note: for NAND, c=0, i=1➡$c \oplus i = 1, \bar{c} \oplus i = 0$)

-So, we can make a table of the fault lists as a function of time.

-We want to continue until the circuit is stable

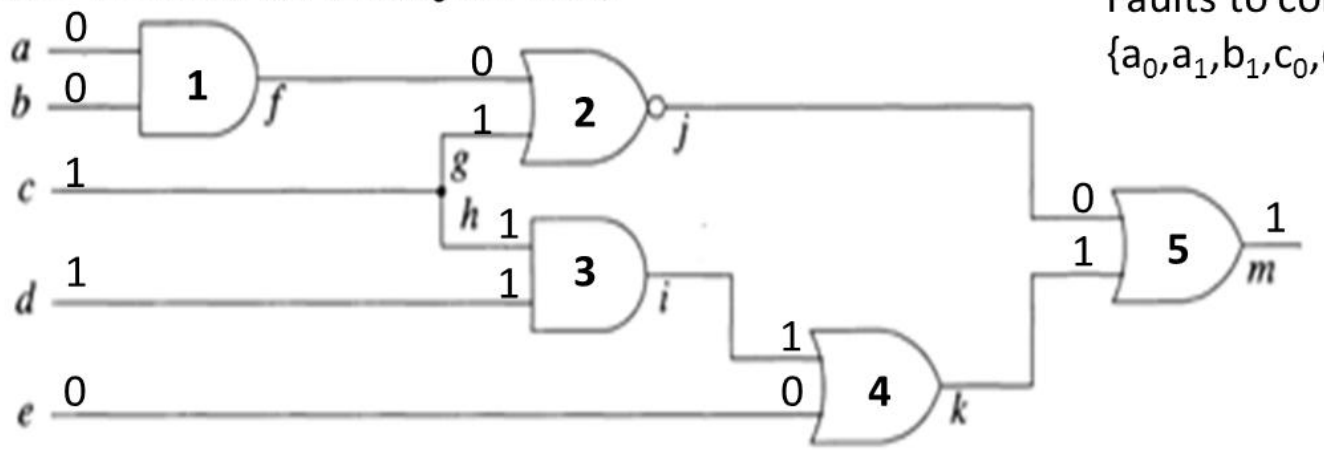
	T=0	T=1	T=2	T=3
L_S	L_S	L_S	L_S	L_S
L_R	L_R	L_R	L_R	L_R
$L_{\bar{y}}$	$L_{\bar{y}}$	$\left[(L_S - \mathrm{L_y}) \bigcup \bar{y}_0\right] \equiv A$	A	$A \bigcap B = (L_S - L_y) \bigcup \bar{y}_0$
L_y	L_y	L_y	$\underbrace{A \bigcup L_R \bigcup y_1}_{\equiv B}$	$\left[(L_S - L_y) \bigcup \bar{y}_0\right] \bigcup L_R \bigcup y_1$

☆ Remember:

$$if\ C = \emptyset\ then\ L_z = \left\{\bigcup_{j \in I} L_j\right\} \bigcup \{Z_{s-a-\overbrace{(c \oplus i)}^{\text{1 for NAND}}}\}$$

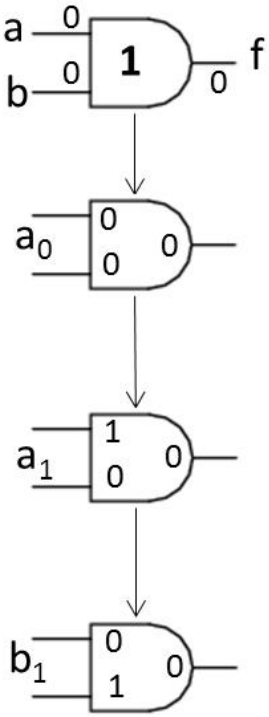
$$else\ L_z = \left(\left\{\bigcap_{j \in C} L_j\right\} - \left\{\bigcup_{j \in I-C} L_j\right\}\right) \bigcup \{Z_{s-a-\underbrace{(\bar{c} \oplus i)}_{\text{0 for NAND}}}\}$$

5.7 Repeat the simulation carried out in Example 5.1 using the concurrent method. (Show the fault lists after simulating each vector.)



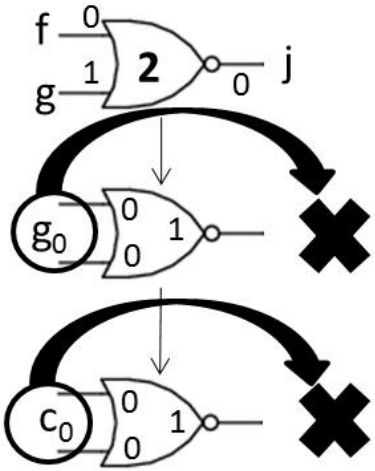
Faults to consider (after collapsing):
$\{a_0,a_1,b_1,c_0,c_1,d_1,e_0,g_0,h_0,h_1\}$

Start with the AND-gate with output, f:



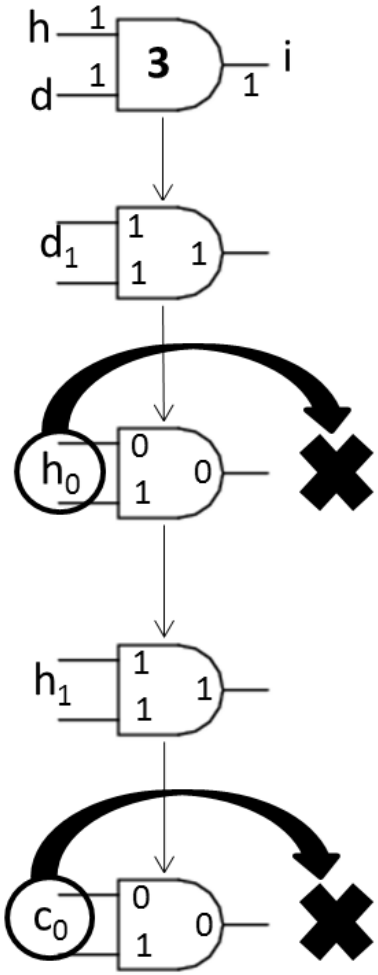
Note that a_0, a_1, b_1 are **local faults** so they are included even though f is not different from the correct operation

Next, consider the NOR-gate with output, j:



Note that none of the faults considered on the AND-gate f effect this NOR-gate… so we consider only local faults and faults effecting g. The only local fault in our list is g_0. But, c_0 has the same effect.

Next, consider the AND-gate with output, i:

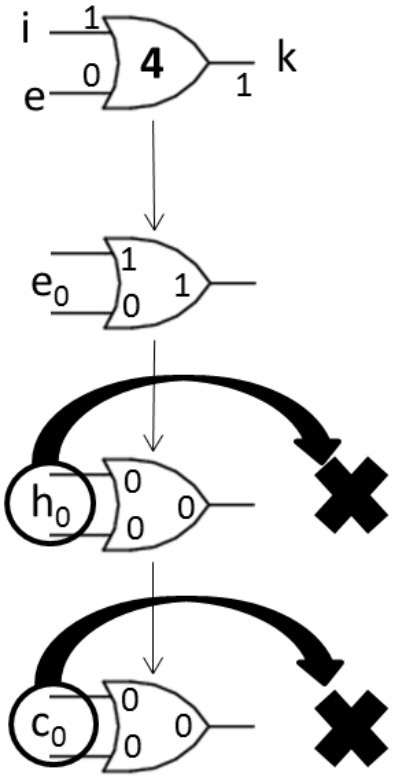


Note the only local faults are d_1, h_0, h_1. We also consider c_0.

Next, consider the OR-gate with output, k:

Local faults = e_0

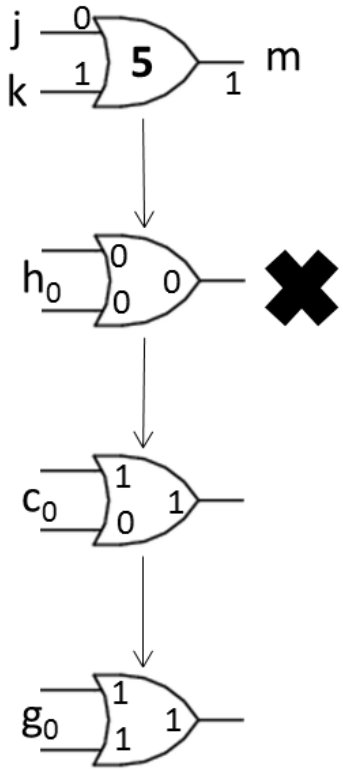
But, we must also consider the effects of the AND-gate with output, i.



Finally, consider the OR-gate with output, m:

Local faults = none

However, we must consider faults from the NOR (output j) and OR (output k) gates.



Note: Looking at the NOR-gate we see that its faults do not effect the output m.

Therefore, (h_0) is detected.

5.9 For the circuit in Figure 5.38, determine the faults detected by the test 111 by

a. concurrent fault simulation (start with a collapsed set of faults)

b. critical path tracing.

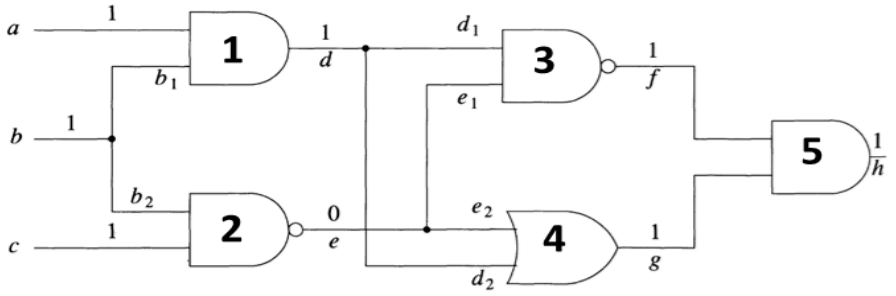


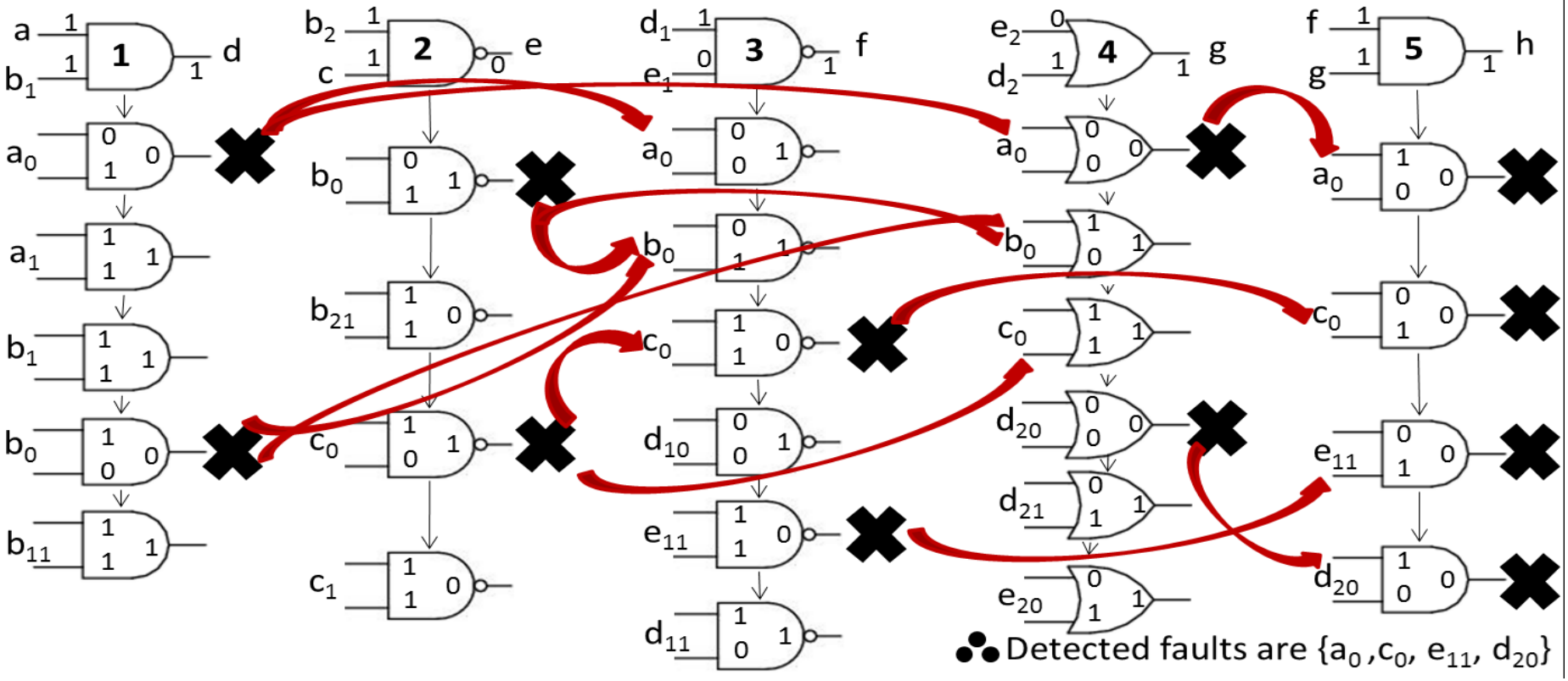
Figure 5.38

Part A:

checkpoint faults =

$\{a_0,a_1,b_0,b_1,c_0,c_1,d_{10},d_{11},b_{10},b_{11},b_{20},b_{21},d_{20},d_{21},e_{10},e_{11},e_{20},e_{21}\}$

Remove equivalent faults (collapse): $\{a_0,a_1,b_0,b_1,c_0,c_1,d_{10},d_{11}, b_{11}, b_{21},d_{20},d_{21}, e_{11},e_{20}\}$



Part B:

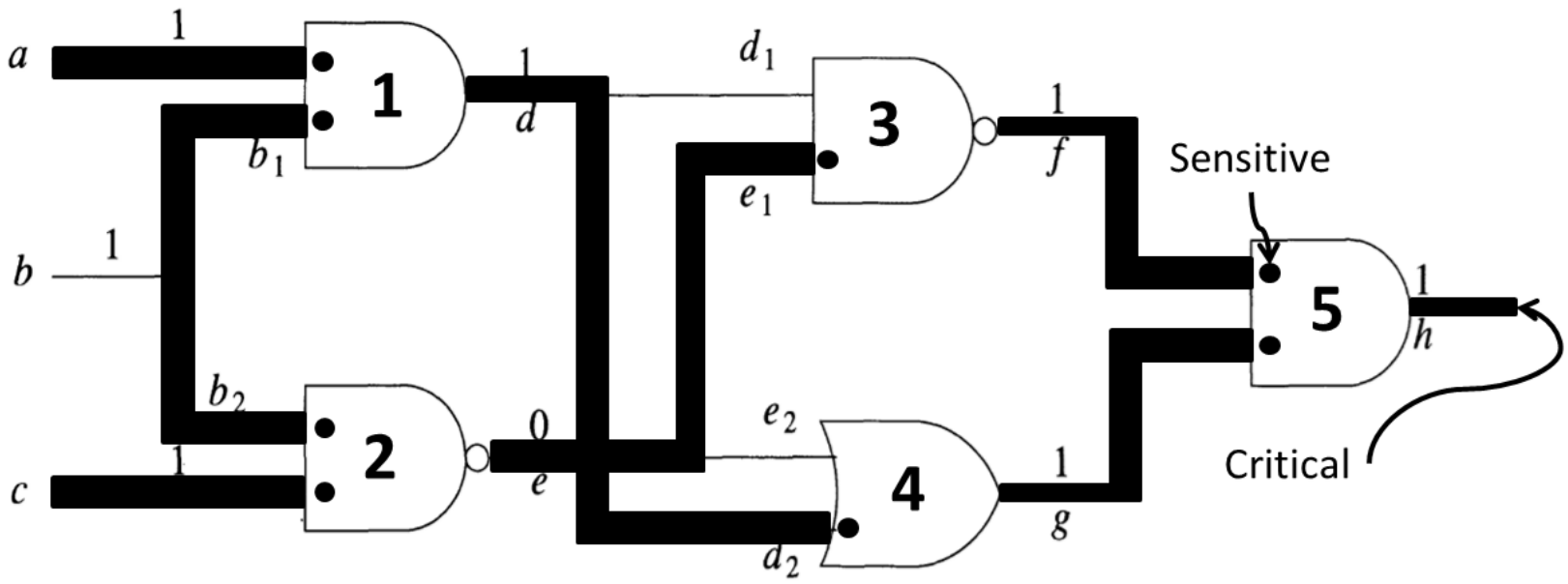


Figure 5.38

These are **all** the detected faults: {a_0, b_{10}, b_{20}, c_0, d_0, d_{20}, e_1,e_{11},f_0,$g_{0,}$ h_0}

Comparing this to the collapsed list from part (A), we have: {a_0, c_0, d_{20}, e_{11}}
(Same as Part A)