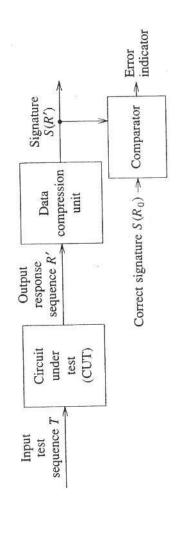
Compression Techniques & BIST (CH.10)

- Overview:
- Signature / Response Compacting
- Ones-Count Compression (10.2)
- Transition-Count Compression (10.3)
- Parity-Check Compression (10.4)
- Syndrome Testing (10.5)
- Special case of Ones-counting (Normalized)
- Signature Analysis (LFSRs) (10.6)

Compression Techniques & BIST (CH.10)

- requirements for the CUT output response Objective: Reduce the memory storage
- Response Compression ==> signature

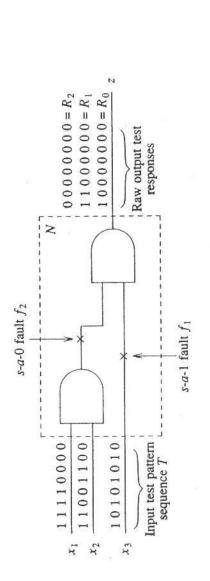


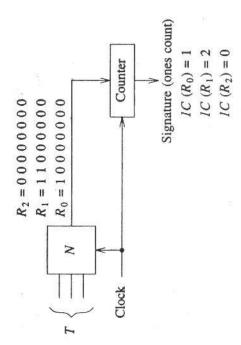
General Aspects of Compression Techniques (CH.10.1)

- Compression circuitry must be:
- reliable
- simple (low cost, small size)
- must not introduce significant delays
- capable of significantly reducing the output response
- Difficulties:
- Error Masking => alias
- How to determine the correct signature
- simulation can be too expensive for long patterns
- possibly use "Golden Device"
- or find circuits which produce common signatures

Ones-Count Compression (CH.10.2)

- In this method, the number of 1's in the output signature is counted.
- The signature is denoted:
- $IC(R) = \sum_{i} r_{i}$
- and the summation is from 1 to m
- where m is the length of the output pattern





Ones-Count Compression (CH.10.2)

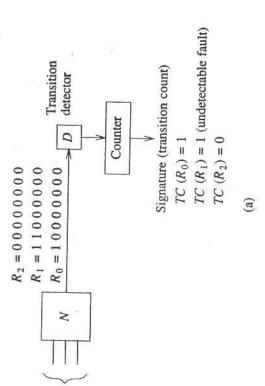
- The probability of masking depends on the number of 1's in a given response
- If the number of 1's is close to 0 or to m, then the chances of masking are reduced
- (assuming that all output patterns are equally likely)
- will be detected (an even number might not) A fault that causes an odd number of errors
- Inverting the output will not effect the test
- For combinational circuits, the order of the tests is not important.

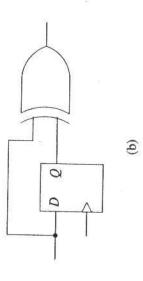
Ones-Count Compression (CH.10.2)

- Theorem 10.1 For lengthy patterns, the masking probability approaches $(^{\prime\prime}m)^{4/2}$
- Theorem 10.2 We can devise a set of tests which will not exhibit error masking:
- let $T = \{T^0, T^1\}$ be m test vectors that detect faults F.
- T⁰ are those tests with output 0
- T¹ are those tests with output 1
- Then let $T'(1C) = \text{one copy of } T^0 \text{ and } |T^0| + 1 \text{ copies}$
- then, T'(1C) detects all faults F with no masking.
- the worst-case length of T'(1C) is m^2

- In this method, we count the number of 0-1 and 1-0 transitions in the output response.
- Clearly the order of the tests is important.
- patterns that have long sequences of The compression factor is greater for repeated 1's and/or 0's.
- The T-C response signature is:

 $TC(R) = \sum_{i=1}^{m-1} (r_i \oplus r_{i+1})$





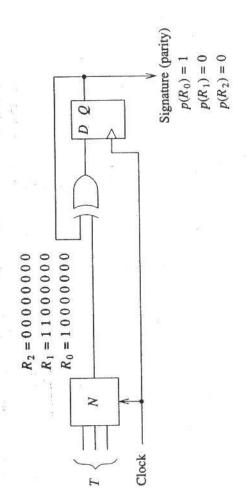
(a) Transition-count testing (b) A transition detector

- sequence, the probability of a single-bit error Theorem 10.3 - With an arbitrary m-bit being masked is (m-2)/2m
 - Note that for large m, this approaches 1/2
- Theorem 10.4 For combinational circuits, the masking probability appraches $(\pi m)^{1/2}$

- Theorem 10.5 Let T be a SSF test set for an irredundant single-output combinational circuit. Then we construct a TC test, $X^* = t(1)t(2)t(3)...t(p)$ as follows:
- X* contains every test in T
- X* alternates between tests from T⁰ and T¹

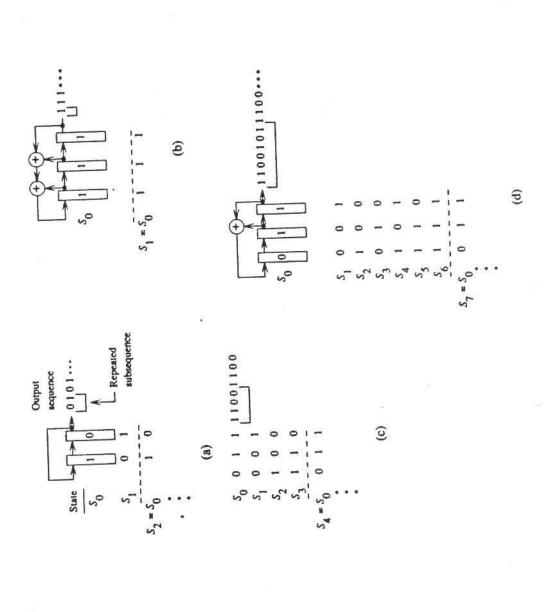
Parity-Check Compression (CH.10.4)

- section 10.6) where the primitive polynomia Actually this is a special case of LFSR (see is just G(x) = x+1
- The signature is the parity of the response
- S = 0 for even parity
- S=1 for odd parity (assuming initial state is 0)



- Linear Feedback Shift Registers (10.6.1)
 - LFSRs can be used as pseudo-random pattern generators for input stimuli
 - and/or for output compression
- Note that modulo-2 addition/subtraction can be implemented using XOR gates
- Note: x+x = -x-x = x-x = 0 for Mod-2 addition

Examples of Feedback Shift Registers



Two types of LFSRs:

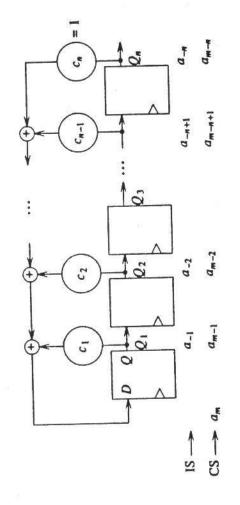


Figure 10.10 Type 1 LFSR

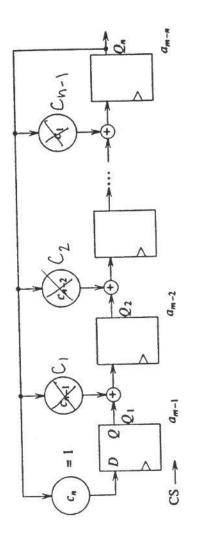


Figure 10.11 Type 2 LFSR

Polynomial Division - Examples

Example 10.1:

since
$$x^2 + x^2 = 0$$
.

$$x^{2} + \frac{x^{2} + x + 1}{x^{4} + x^{3} + x^{2} + x + 1}$$

$$(-) \frac{x^{3} + x^{2} + x + 1}{x^{3} + x^{2} + x + 1}$$
 (note $x^{2} = -x^{2}$)
$$(-) \frac{x^{2} + x + 1}{x^{3} + x^{2} + x + 1}$$

LFSR Polynomials - Definitions / relations

Characteristic Polynomial:

•
$$P(x) = 1 + c_1x + c_2x^2 + c_2x^3 + \dots + c_nx^n$$

Reciprocal Polynomial:

•
$$P^*(x) = c_n + c_{n-1}x^1 + c_{n-2}x^2 + ... + c_1x^{n-1} + x^n$$

- Note:
$$P^*(x) = x^n P(1/x)$$

LFSR implementations:

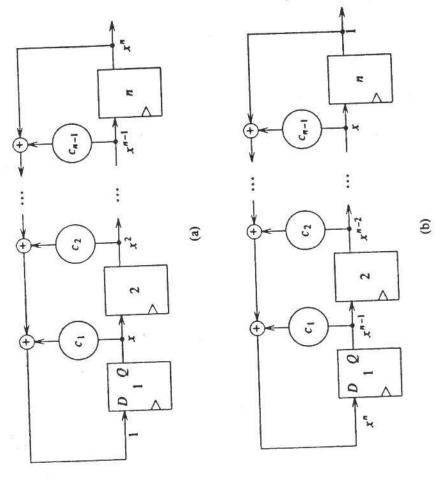


Figure 10.12 Reciprocal characteristic polynomials

(a) $P(x) = 1 + c_1 x + c_2 x_2 + ... + c_{n-1}x^{n-1} + x^n$ (b) $P^*(x) = 1 + c_{n-1} x + c_{n-2} x^2 + ... + c_1 x^{n-1} + x^n$

Periodicity of LFSRs

- periodic with a period that is the smallest integer k for - Theorem 10.6 - If the initial state (IS) of the LFSR is all zeros except a_{-n}=1, then the LFSR sequence is which p(x) divides $(1-x^k)$.
 - An n-stage LFSR with period 2ⁿ-1 produces a maximum-length sequence.
- Theorem 10.8 A primitive polynomial is irreducible polynomial to divide evenly into 1+xk occurs for $k=2^{n}-1$, where n is the degree of the polynomial. if the smallest positive integer k that allows the

Number of primitive polynomials:

λ ₂ (π)	-	-	2	91	2048	67108864
E	-	2	4	000	91	32

Examples of exponents for primitive polynomials:

11			13:	4	3	-	0	25:	3	0		
			14:	12	Ξ	-	0	26:	00	1	-	0
			15:	-	0			27:	∞	7	-	0
			16:	2	3	2	0	28:	3	0		
			17:	3	0			29:	7	0		
			18:	1	0			30:	16	15	_	0
			19:	9	2	-	0	31:	3	0		
	_	0	20:	Э	0			32:	28	27	-	0
			21:	7	0			33:	13	0		
			22:	-	0			34:	15	14	-	0
			23:	2	0			35:	7	0		
	1	0	24:	4	3	-	0	36:	=	0		

Characteristics of maximum-length sequences

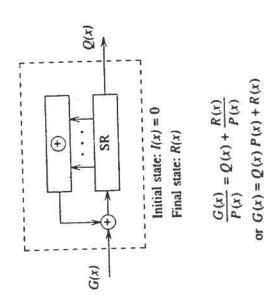
Patterns are pseudorandom

The number of 1s differs from the number of 0s by 1

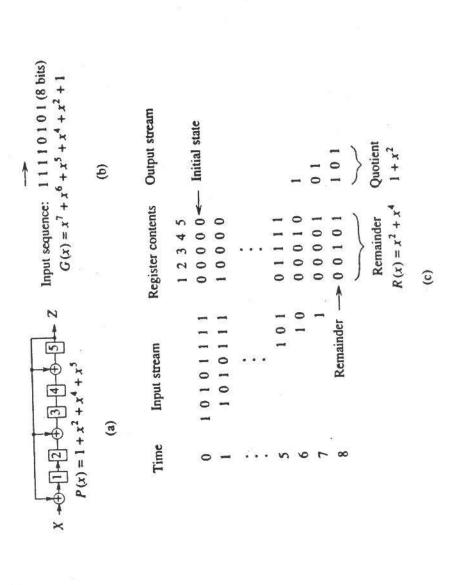
- The number runs of 1s and 0s is equal

Half the runs have length 1, 1/4 have length 2, 1/8 have length 4, etc.

LFSRs as Signature Analyzers (10.6.2) - Based on Cyclic Reduncancy Checking (CRC)



Example 10.2



Error Masking

- The chance of NOT detecting an error approaches 2-n

- see Theorem 10.10.

Multiple-input signature register (MISR) 10.6.3

