9-V algorithm: 199-202

- A -

active signal: 42, 50, 79
activity: 42, 50, 65, 70, 79, 83
addressing fault: 325-328, 330-332
advanced scan: 343
algorithm partitioning: 79, 80, 82, 83
alias: 422, 423, 426
ambiguous delay: 53, 76, 77
appearance fault: 595, 598
arbitrary delay model: 61-64, 77
ATG system: 240, 242, 243

- B -

B-structure: 390, 392, 393
backtrace-stop line: 212, 213, 218
backtracing: 204-206, 208, 209, 211, 215, 240
backtracking: 187, 189, 191, 192, 196, 198, 201, 206-209, 211, 212, 221, 223, 224, 243, 251, 258, 264
back line: 294, 301
BALLAST: 389, 390, 393
behavioral model: 9, 23
Berger code: 571, 579, 587, 588
BEST: 483, 512, 513, 535
BIDCO: 505
BILBO: 459, 500-506, 510-516, 518, 519, 521, 522, 536, 537
binary decision diagram: 17, 18
BIST architecture: 457, 477, 481-484, 487, 488, 491-496, 500, 503, 505, 510, 512, 513, 518, 533, 534, 535
BIST circuitry: 458, 477, 481, 498
BIST element: 477
bit-sliced system: 321-323
boundary-scan cell: 396, 399, 407, 418
boundary scan: 343, 363, 382, 383, 395, 396, 416, 492
bridging fault: 93, 94, 96, 99, 107, 119, 289, 290
burst error: 422, 445
bus: 40, 42, 71-74, 82, 83
bus driver: 71, 72
bypass storage cell: 476-480, 526, 533

- C -

C-testable: 317
CAMELOT: 346
CATS: 495, 513, 534
cause-effect analysis: 7
CBIST: 489, 490, 513, 535
CEBS: 491, 492, 513
characteristic polynomial: 436, 437, 439, 442, 446, 448-450
checker: 571, 574, 580-588, 591
checking sequence: 315, 317
checking the checker problem: 580
checkpoint: 116, 117
check bit: 572-579, 587
circular masking relation: 120
circular self-test path: 498, 499
cloud: 390-394, 415
common ambiguity: 77
compaction: 245, 246
compact testing: 6
comparison testing: 6
compiled-code model: 24
compiled simulator: 42, 46, 47, 49, 80
complete detection test set: 99, 103
complete LFSR: 460, 470, 532
complete location test set: 107
composite logic value: 182, 248
composite operation: 268
concurrent decision processing: 272
concurrent fault list: 147, 148, 150
concurrent fault processing: 272
concurrent guidance processing: 272
condensed LFSR: 474-476
conditional operation: 21
conflict: 40, 71
connectivity language: 10
constant-weight code: 473
constant-weight counter: 473, 505
constant-weight pattern: 467, 473
constraint network: 564
constraint suppression: 564-566
controllability: 343-347, 352, 353, 355, 358, 359, 362, 363, 368, 401
controllability measure: 214, 215, 217
controlling value: 59

control event: 51
control fault: 122
control point: 347, 349, 358, 362, 363, 416
cover: 11, 12
critical fault: 244
crosspoint: 593-601, 603-609, 614, 616-618, 621, 624, 625
crosspoint faults: 594-599, 603, 605, 608, 609, 614, 617, 618, 621, 625
CSBL: 512, 513, 535
CSTP: 495, 505, 513
cube: 11, 12
cubical notation: 11
cutting algorithm: 232
cyclic LFSR: 476
cyclic redundancy checking: 431, 441

- D -

D-algorithm: 225
D-frontier: 192, 193, 195, 198, 203-206, 208, 215, 253, 263
data fault: 122
decision tree: 189-191, 196, 198, 201, 206, 208, 209, 221, 253, 272
deductive fault simulation: 139, 146
defect level: 131
delay element: 56
delay fault: 93, 111, 122
delay model: 39, 52-56, 61-64, 74-77
design error: 2, 3, 7
design for testability: 343
design verification testing: 3, 7
detection function: 639, 641
detection probability: 227-230, 232, 233, 235, 275, 276
detection quality: 227, 229, 232, 234, 276
diagnostic graph: 633-638, 640
diagnostic program: 2, 4, 5, 7
diagnostic resolution: 541, 544, 547, 548, 551-553, 556
diagnostic tree: 544, 545
distinguishing sequence: 317, 320
dominance fault collapsing: 109, 116, 117
double-latch design: 376, 380
driven value: 32, 289, 294, 295
dynamic compaction: 245, 246
dynamic hazard: 62, 63

- E -

effect-cause analysis: 7, 541, 543, 559, 560, 563, 564
empty fault: 107
equality checker: 586-588
equivalence fault collapsing: 107, 114, 116
equivalent under a test set: 108
error masking: 422, 425, 442, 445, 453
error polynomial: 444, 446
error propagation: 182, 184, 186, 189, 195, 198, 202, 204, 205, 225, 247, 248, 253, 255, 261, 269
escape probability: 227, 228
evaluation: 39-42, 46, 47, 49, 50, 56-60, 66-68, 71, 74-77, 80, 81
event: 39, 40, 42, 43, 49-51, 53, 64-70, 74-79, 81-83
event-driven simulation: 39, 42, 50, 64, 77, 81, 82
event list: 50, 64-68, 70, 75, 82, 83
exhaustive testing: 305, 313-315, 317, 337, 457, 460-462, 474, 476, 491
expansion: 26, 31, 32
expert system: 541, 557-560, 564
explicit fault model: 93, 111
external model: 10, 25, 26, 31
external testing: 8

- F -

fabrication defect: 2, 3
fabrication error: 2
FAN: 208, 209, 211
fanout node: 27, 28
fault-independent algorithm: 220, 226
fault-list propagation: 139, 146
fault coverage: 3, 41
fault detection: 93, 98, 104, 107, 109, 116
fault dictionary: 7, 541, 543, 544, 548, 549, 553, 554, 557
fault dropping: 135, 139

fault effect: 98
fault insertion: 134-136, 138
fault location: 104, 107
fault model: 3, 7
fault pattern: 634-644
fault preventing initialization: 106
fault sampling: 131
fault secure: 580, 581, 584, 588-590
fault simulation: 3, 7
fault specification: 134
fault variable: 122, 123
feedback bridging fault: 290
fixed variable: 310-312
flexible signal: 225
flow table: 13-15
forced value: 32, 561, 562
frequent testing strategy: 94, 99
front line: 294, 298, 299, 301
full serial integrated scan: 366, 374
functionally equivalent: 106-109, 113, 114
functional block: 33
functional equivalence class: 106
functional fault: 93, 111, 122
functional model: 9, 10, 18, 33
functional testing: 305, 307-309, 312, 325, 337, 338
fundamental mode: 64

- G -

gate-level model: 32, 33
generalized diagnostic graph: 638, 640
generating function: 433
generic algorithm: 265
global feedback: 344, 347, 351, 358
global implication: 194
growth fault: 595, 598
guided-probe testing: 7, 541, 549-554, 564

- H -

Hamming code: 573
Hamming distance: 572
hardcore: 4, 5, 458, 581, 582, 590
hazard detection: 39, 61, 62
head line: 208, 209, 211, 212
heuristic testing: 306
HITEST: 272, 273
horizontal implication: 560, 561

- I -

I-mode: 386, 387, 389
I-path: 386-389
identity mode: 386
IEEE 1149.1: 395, 522, 523
implication: 187, 191-195, 200, 206, 211, 265, 266
implicit enumeration: 190, 191
implicit fault model: 93
implicit simulation: 298, 301
in-circuit testing: 6
inconsistency: 12
independent checking: 575
independent fault: 138
inertial delay: 54, 55, 75, 76
information bit: 573-575, 577, 579, 587, 588
information redundancy: 6
initialization: 347, 351, 366
initialization sequence: 104
injection circuit: 347, 348, 352, 358
input counting: 60
input scanning: 60
internal model: 9, 10, 12, 31
intersection operator: 12
invalidation function: 639, 641
inverse operation: 266
inversion parity: 27
irreducible polynomial: 439
irredundant: 101, 103, 117, 120
isolated scan architectures: 374
iterative array: 15, 16
iterative logic array: 317

- J -

J-frontier: 192, 193, 198, 204, 206
JTAG: 343, 396

- K -

knowledge base: 557-560

- L -

level: 9, 10, 18, 20, 22-24, 28, 31-35
level-sensitive latch: 369, 376
level-sensitive scan design: 370, 381
level of abstraction: 1, 2
level of modeling: 32-34
LFSR: 431-437, 439-442, 444-446, 447, 453
linear code: 473, 476
linear feedback shift register: 428, 432, 433, 459
line justification: 186, 247, 261, 267, 273
list event: 139, 141, 144, 146, 148
local fault: 140, 147, 148
LOCST: 487, 513, 535
logical fault: 3, 7, 93, 94
logical strength: 73
logical transfer path: 329
logic simulation: 3, 39, 40, 42, 57
LSSD: 446, 484, 487
LSSD design rule: 416

- M -

m-sequence: 440
macro approach: 26, 31
maintenance testing: 5
masking: 422-427, 429, 441, 442, 445, 446, 453
masking relation: 119, 120
mask word: 136, 138
maximal fault resolution: 541
maximum-length sequence: 439
maximum implications principle: 192
microprogramming model: 328
minimum pulse width: 55
mixed-level modeling: 34, 35
model partitioning: 79-83
modular redundancy: 6
module: 33, 633, 635, 636, 638, 640
morphic function: 581, 582, 590
MOS logic: 72
multiple-backtrace: 208
multiple-input signature register: 458
multiple-line redundancy: 120
multiple-path sensitization: 198, 202, 206, 223
multiple fault: 93, 94, 102, 119-121

- N -

nonclassical fault: 110, 111
nonfeedback bridging fault: 290
nonprocedural language: 23
nonseparable code: 579
nonserial scan: 374
nonuniform distribution: 234

- O -

objective: 204-206, 208, 209, 211, 220, 235, 240, 262, 264, 273
observability: 343-347, 352, 353, 355, 358, 359, 361-363, 368, 399
observability measure: 214-216, 219
observation point: 347, 348, 351, 358, 361-363
on-line testing: 5
one-pass strategy: 68, 69
ones counting: 421, 423, 425, 427, 429
open: 93-95
operation: 12, 21-23
oscillation: 39, 40, 46, 64, 77-79, 82
oscillation control: 39, 78, 79, 82
overhead: 349, 358, 367, 368, 376-378, 388, 416
overlapped mode: 383, 385

- P -

pairwise distinguishing sequence: 320
parallel-pattern evaluation: 47
parallel fault simulation: 135, 138, 139
parity-check code: 572-574, 578, 579
parity-check compression: 429, 453
parity-check function: 581, 582
partial-dependence circuit: 313, 314
partial-intrusion BIST: 457, 519-521
partially specified composite value: 199, 200

partial scan: 383, 386, 388, 390, 392, 394, 418
partitioning technique: 315
path-sensitization algorithm: 196
pattern coverage: 499-501
permanent fault: 94
personality: 593, 598, 600, 603, 618
physical failure: 2-4
physical fault: 3
physical model: 33
physical segmentation: 476
pin-fault model: 95
pipelined test plan: 520
plausible fault: 556, 557
PLA folding: 620
PMC model: 640, 642, 643
PODEM: 203-209, 211, 215, 235, 264, 272
polarity-hold latch: 372, 381
post-test diagnosis: 133
potential operation: 265, 267
predictability: 343, 347
primitive cube: 11, 12
primitive element: 9, 18, 31
primitive operator: 21, 22, 33
procedural language: 23
programmable logic arrays: 593
pseudoexhaustive testing: 305, 313, 314, 337
pseudorandom pattern generator: 458, 460
pseudorandom sequence: 440
pseudorandom testing: 457

- R -

random-access scan: 372, 411
random path sensitization: 236
RAPS: 235-238, 240, 242, 243, 277
reciprocal polynomial: 437
reconvergent fanout: 26
reduced neighborhood: 298
redundancy: 93, 101-103, 120, 347, 358
register adjacency graph: 514, 515, 528
replaceable unit: 541, 542
residue code: 571, 575-577, 579, 587
restart gate: 238-240, 246
rise and fall delay: 53, 55, 74
RTD: 491, 493, 504, 513
RTS: 484-486, 513

- S -

S-mode: 388
S-path: 389
scan-in: 358, 359, 363, 381, 396
scan-out: 358, 359, 363, 372, 381, 396
scan/set: 366
scan design: 343, 351, 364, 366-368, 371, 372, 374, 376-380, 383, 384, 388, 390, 392, 394, 416
scan path: 363, 370, 376, 383, 384, 386, 388-394, 397, 399-401, 404, 406-408, 418
scan register: 358-366, 368, 388-390, 392, 394, 396, 397, 404, 407-409, 411, 416, 417
SCIRTSS: 269-271
SCOAP: 346
selection criteria: 213
self-checking design: 571, 590
self-initializing test sequence: 253, 278
self-testing: 4, 7, 580-582, 589, 590
self-test storage cell: 493, 494
sensitive variable: 310, 311
sensitized mode: 388
sensitized path: 98
separate mode: 383, 385
sequential diagnosability: 634, 636
sequential diagnosis: 542
shadow register: 364, 367, 413, 415
shift register pattern generator: 458
short: 93, 94
shrinkage fault: 595
signal probability: 229, 230, 232, 234, 276
signature: 6, 7, 421-425, 428, 429, 432, 441, 442, 444-447, 455
signature analysis: 421, 432, 442, 445
signature analyzer: 441, 442, 444-448
simulation-based TG: 262, 264
simulation engine: 79, 80, 82
simultaneous self-test: 493
single-fault assumption: 94, 99, 103
single-input signature register: 458
single-latch design: 376, 380

single-loop system: 636, 638, 641, 643
single-path sensitization: 203
SMART: 238, 240, 242, 243
spike: 54, 68, 69, 76
SPLASH: 386
SST: 493, 494, 496, 513
start-small: 307, 331, 333
state coverage: 499
state event: 50
state table: 13, 18
static compaction: 245, 246
static hazard: 60-62, 77
statistical fault analysis: 131
stop line: 212, 213, 218, 238-240
storage cell: 358-363, 365, 366, 368-370, 372, 376, 377, 379, 382, 384, 390, 391, 393, 394, 399, 407, 418
stored-pattern testing: 7
strong value: 73
structural equivalence: 113, 114, 116, 117
structural fault: 93, 94, 113
structural model: 9, 10, 18, 24, 26, 29, 31, 33
structured DFT: 345, 364, 382
stuck-fault model: 93, 95, 109, 122
STUMPS: 488, 489, 512, 534
subsystem approach: 31
switch-level model: 32
synchronizing sequence: 317
syndrome: 634-638, 640
syndrome driver counter: 473
syndrome testing: 429, 431, 448
system-level DFT: 343, 382

- T -

T-mode: 388
TAP controller: 401-404, 406, 407, 419
target fault: 133, 182, 190, 204-206, 209, 220, 243-246, 248, 251, 259, 271
testability: 343, 346, 347, 354, 363
testing quality: 227-229, 276
test access port: 396, 401
test bus: 382, 396, 397, 400-403, 419
test latency: 490
test plan: 520, 521, 535
test point: 346-349, 351, 358, 362
test session: 383, 385, 387, 457, 503, 510, 511, 513, 515-518, 528
test signal: 462, 466, 467, 472
time-flow mechanism: 50
time frame: 249-255, 257, 258, 261, 262, 269, 272
timing wheel: 70
together mode: 383
total-dependence circuit: 314
total-reconvergence line: 211-213
transfer-mode: 388
transition-count testing: 427
transition-independent delay: 53, 74, 76
transmission gate: 72, 74
transport delay: 52-55, 64, 76
tristate logic: 39
truth table: 10-12, 15, 17, 18
two-pass strategy: 64, 69
type 1 LFSR: 435-437, 447

- U -

undetectable fault: 99, 102, 103, 107
unidirectional error: 579
union algorithm: 265, 278
unit-delay model: 52, 61
universal fault model: 313, 315
universal minimal pseudoexhaustive test set: 470
unknown logic value: 43, 71

- V -

verification testing: 462
vertical implication: 560-563

- W -

weak value: 73
weighted test generator: 461
wired logic: 31, 32

- Z -

zoom table: 58, 81