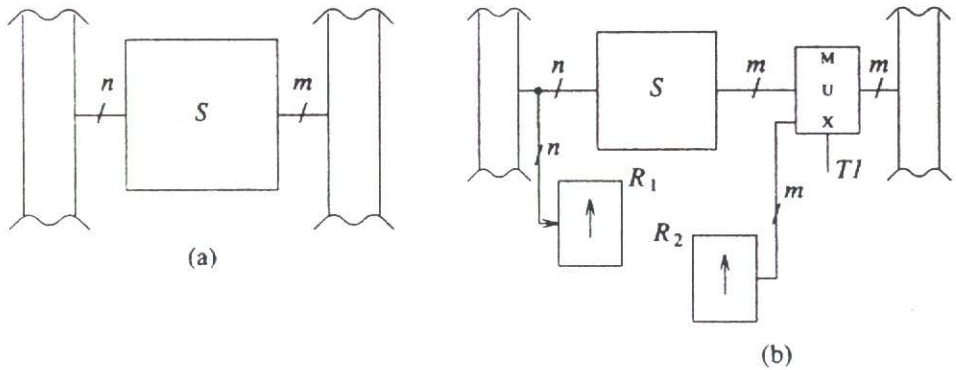
Design for Testability (CH.9)

- Generic Scan-Based Design (9.4)
  - There are two objectives which are achieved with scan-based design:
    - Improved controllability and observability
    - Partitioning of sequential circuits into combinational logic blocks and scannable storage registers
  - The approach is to configure storage registers so that they form scannable registers during testing
    - Full Serial Integrated Scan (9.4.1)
    - Isolated Serial Scan (9.4.2)
    - Non-Serial Scan or Random-Access Scan (9.4.3)

Design for Testability (CH.9)

- Generic Scan-Based Design (9.4)



Design for Testability (CH.9)

- Full Serial Integrated Scan (9.4.1)

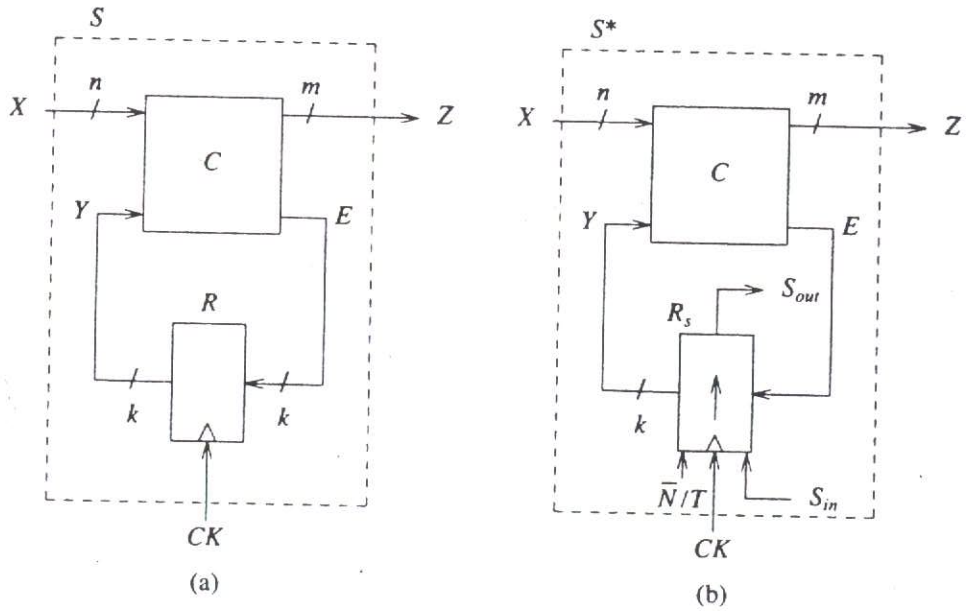
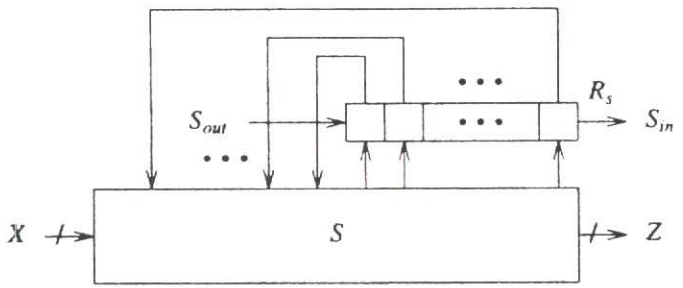
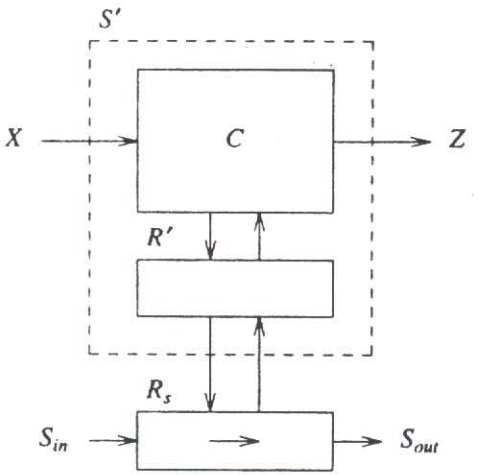


Figure 9.19 (a) Normal sequential circuit S (b) Full serial integrated scan version for circuit

Design for Testability (CH.9)

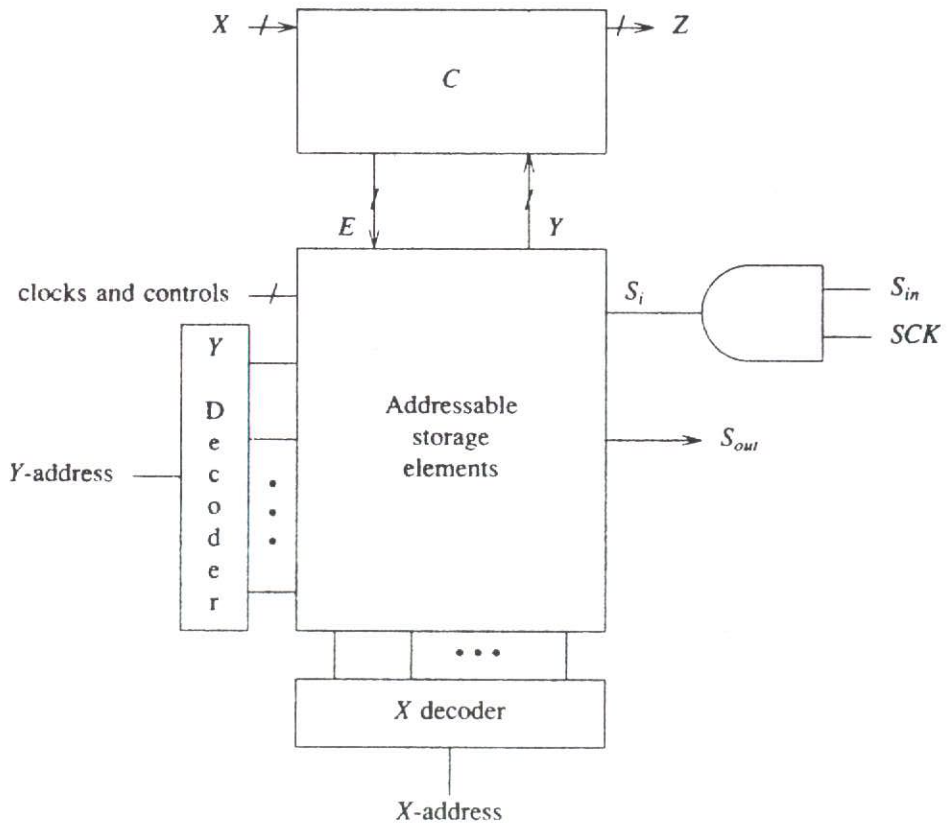
- Isolated Serial Scan (9.4.2)





Design for Testability (CH.9)

- Non-Serial Scan, Random Access (9.4.3)

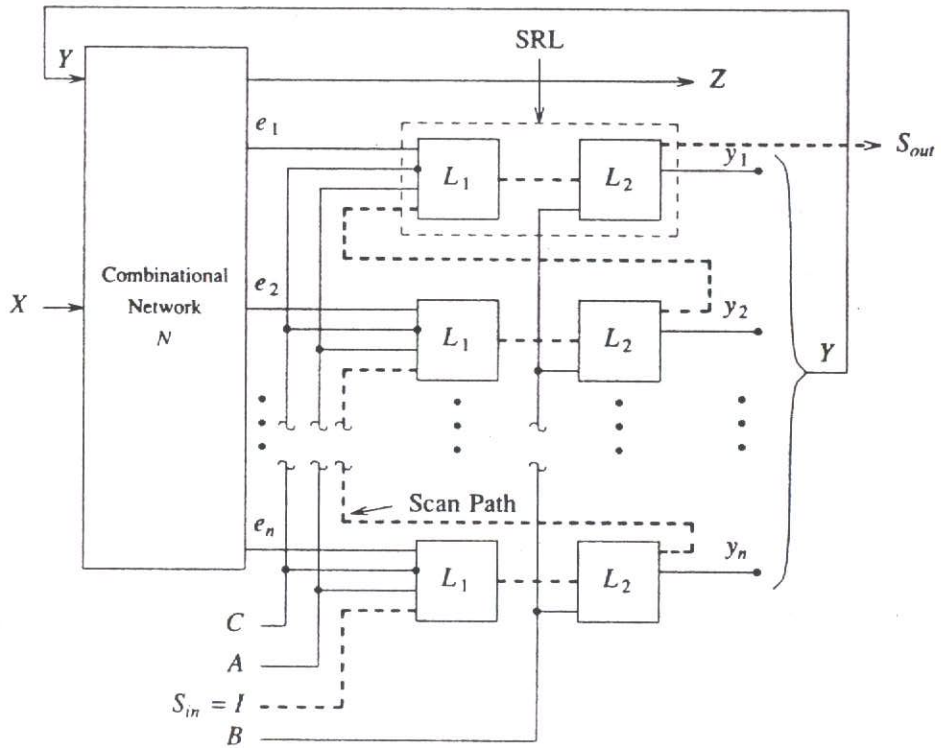


Design for Testability (CH.9)

- Classical Scan Designs (9.6)
  - Scan Path [refs. 1968-75]
    - Full serial integrated scan
    - Uses a raceless Master-Slave D flip-flop (Fig.9.26)
  - Scan/Set [refs. 1977-78]
    - Isolated scan architectures
  - Random Access Scan [ref. 1980]
    - nonserial scan architecture
    - Uses an addressable storage cell
  - Level-Sensitive Scan Design (LSSD)
    - Promoted and used by IBM [ref. 1977-78]
    - Uses two non-overlapping clocks and two-latches

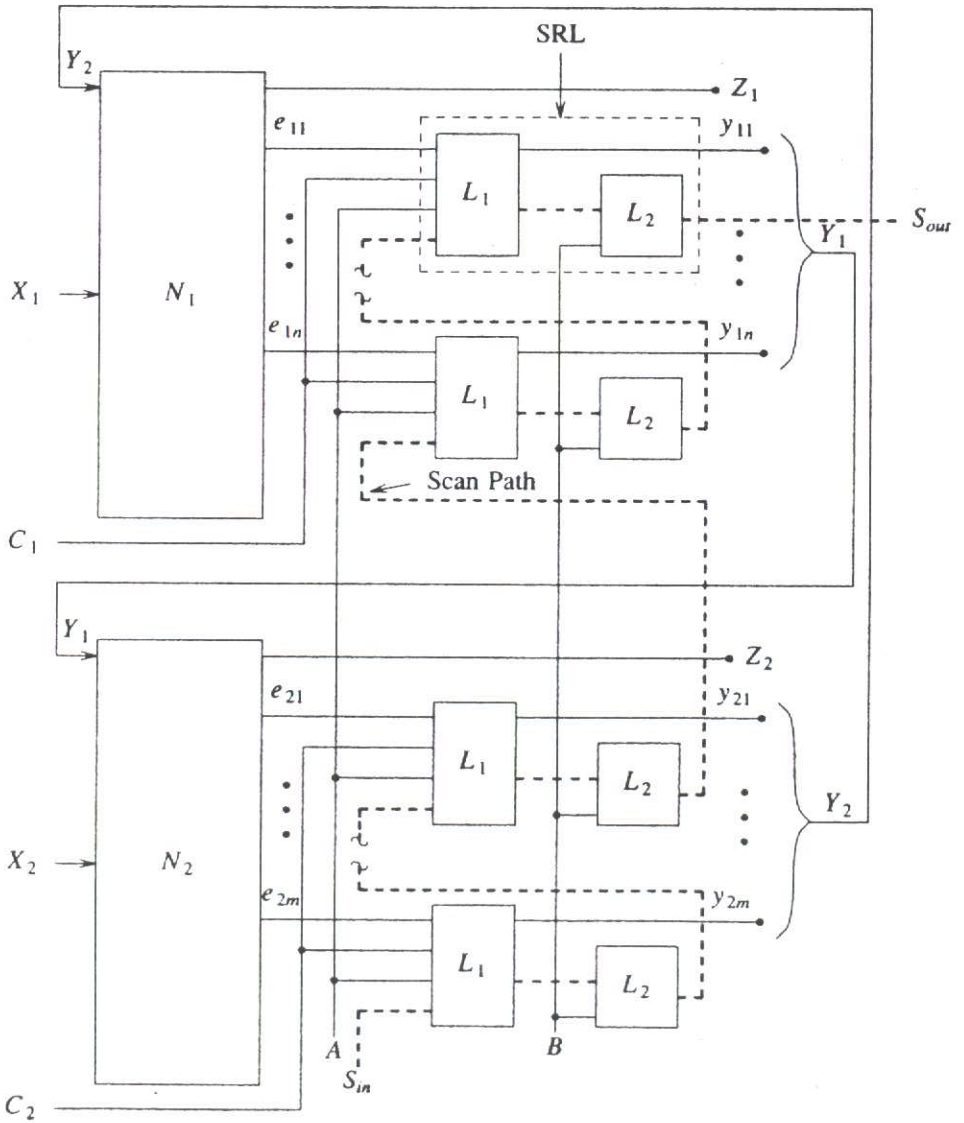
Design for Testability (CH.9)

- LSSD



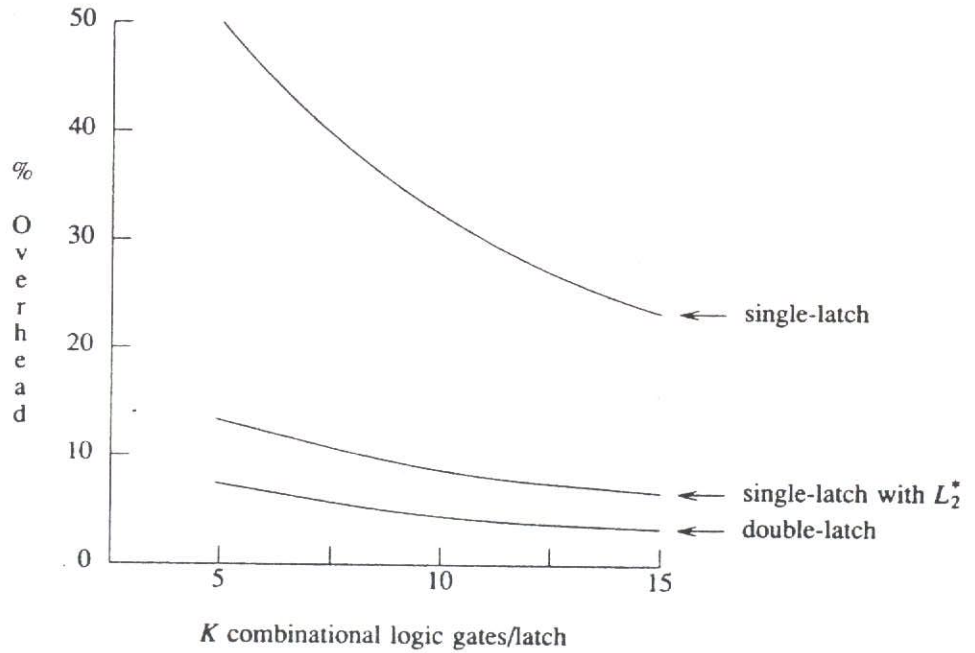
Design for Testability (CH.9)

- LSSD - modified to use conventional SRLs



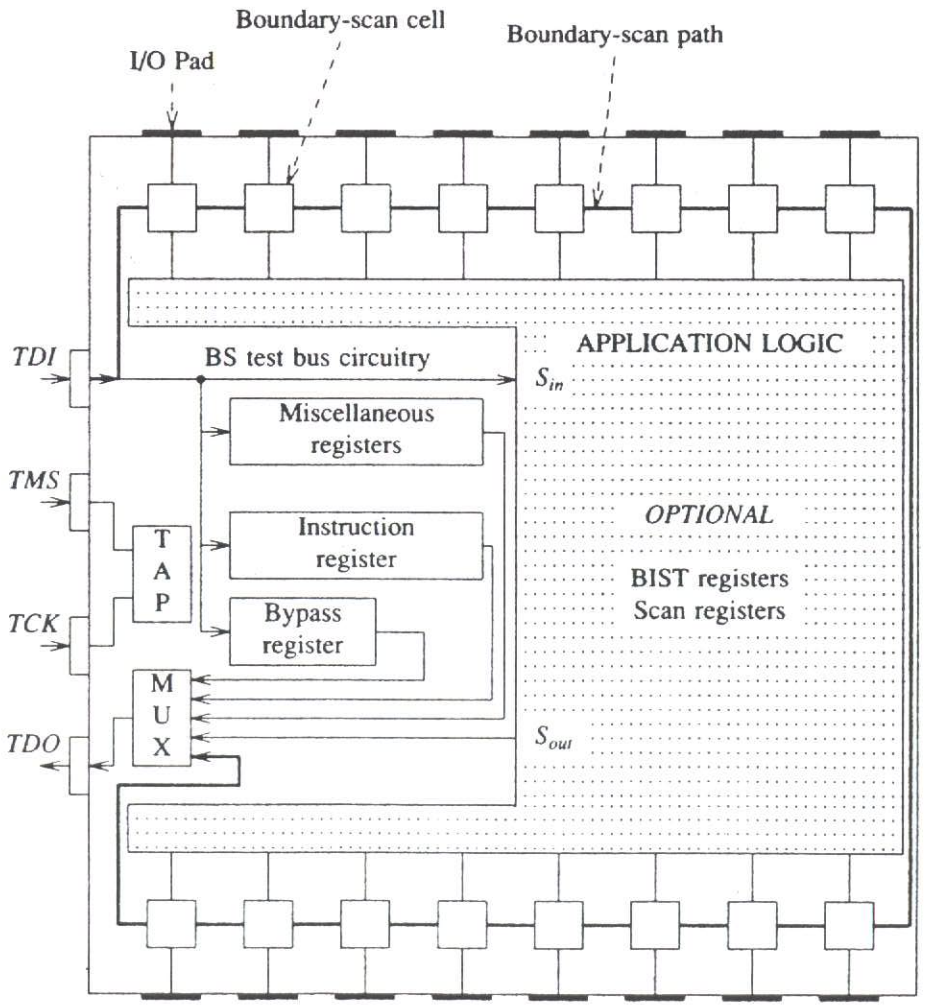
Design for Testability (CH.9)

- LSSD - Overhead



Design for Testability (CH.9)

- Boundary-Scan Standards (9.10)
  - IEEE 1149.1 chip architecture



Design for Testability (CH.9)

- Boundary-Scan Standards (9.10)
  - IEEE 1149.1 applied to a printed circuit board