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TITLE

Voting Circuit

1/12/2024

Design Brief: We will design, simulate, build, and test a voting circuit that will input a "yes" or "no" vote from each of a company's president, vice president, secretary, and treasurer. If the majority vote is "yes," the circuit will output a passing green light, and if the majority votes "no," the circuit will output a fail, or a red light. If the vote is tied, the vote will pass if the president voted "yes," and not pass if the president voted "no." This project will be completed by Monday, January 29. The circuit will be built using a MYDAQ board, 2-input A.O.I. chips, wire, Multisim, and constrained to a 5" x 4" space.

1/16/2024

Define Variables:

P = president (0 = no, 1 = yes)
V = vice president (0 = no, 1 = yes)
S = secretary (0 = no, 1 = yes)
T = treasurer (0 = no, 1 = yes)

L_G = green light (0 = off, 1 = on)
L_R = red light (0 = off, 1 = on)

Truth Table:

PVST	L_G	L_R
0000	0	1
0001	0	1
0010	0	1
0011	0	1
0100	0	1
0101	0	1
0110	0	1
0111	1	0
1000	0	1
1001	1	0
1010	1	0
1011	1	0
1100	1	0
1101	1	0
1110	1	0
1111	1	0

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WITNESSED BY: Cade Mahone
DATE: 1/30/24

TITLE

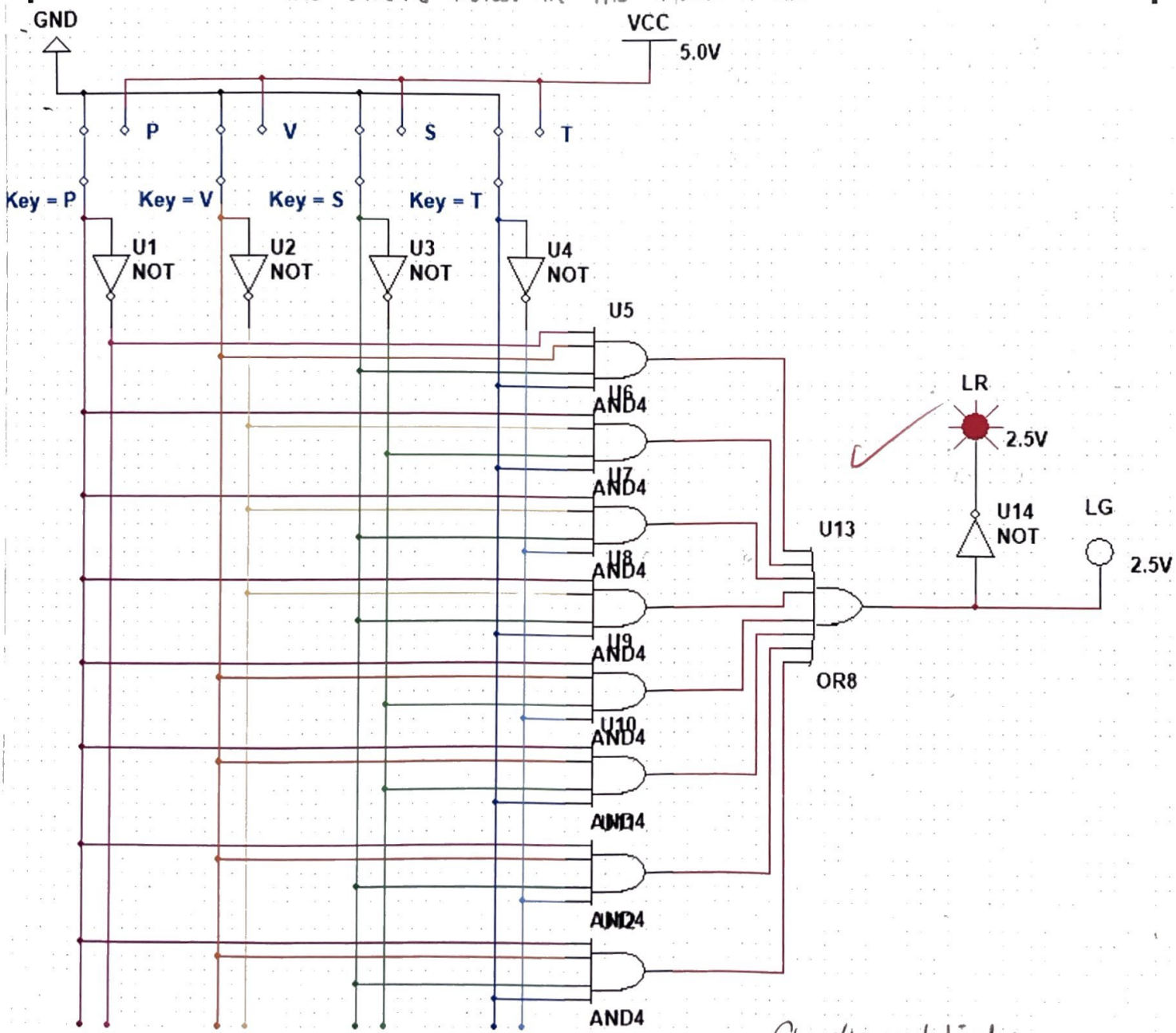
Voting Circuit (2)

Expression: (unsimplified)

$$L_G = \bar{P}VST + P\bar{V}ST + PV\bar{S}T + PVS\bar{T} + P\bar{V}\bar{S}T + PV\bar{S}\bar{T} + \bar{P}VS\bar{T} + \bar{P}\bar{V}\bar{S}\bar{T}$$

1/17/2024

Simulation: I checked every input and each of the 2 outputs matched the binary listed in the truth table.



Built on Multisim

Audrey Wiebe

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TITLE

Voting Circuit (3)

Boolean Simplification:

$L_G = \bar{P}VST + P\bar{V}\bar{S}T + P\bar{V}S\bar{T} + P\bar{V}ST + PV\bar{S}\bar{T} + PV\bar{S}T + PVS\bar{T} + PVST$

factor:

$L_G = \bar{P}VST + P\bar{V}(\bar{S}T + S\bar{T} + ST) + PV(\bar{S}\bar{T} + \bar{S}T + S\bar{T} + ST)$

factor:

$L_G = \bar{P}VST + P\bar{V}(\bar{S}T + S(\bar{T}+T)) + PV(\bar{S}(\bar{T}+T)) + S(\bar{T}+T))$

OR rule:

$L_G = \bar{P}VST + P\bar{V}(\bar{S}T + S(1)) + PV(\bar{S}(1) + S(1))$

AND rule:

$L_G = \bar{P}VST + P\bar{V}(\bar{S}T + S) + PV(\bar{S} + S)$

consensus rule:

$L_G = \bar{P}VST + P\bar{V}(S+T) + PV(\bar{S}+S)$

OR rule:

$L_G = \bar{P}VST + P\bar{V}(S+T) + PV(1)$

AND rule:

$L_G = \bar{P}VST + P\bar{V}(S+T) + PV$

distributive law:

$L_G = \bar{P}VST + P\bar{V}S + P\bar{V}T + PV$

commutative law:

$L_G = \bar{P}VST + PV + P\bar{V}S + P\bar{V}T$

factor:

$L_G = V(\bar{P}ST + P) + P\bar{V}S + P\bar{V}T$

consensus law:

$L_G = V(P + ST) + P\bar{V}S + P\bar{V}T$

distributive law:

$L_G = PV + VST + P\bar{V}S + P\bar{V}T$

commutative law:

$L_G = PV + P\bar{V}S + P\bar{V}T + VST$

factor:

$L_G = P(V + \bar{V}S) + P\bar{V}T + VST$

consensus law:

$L_G = P(V + S) + P\bar{V}T + VST$

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DESIGNED BY: Audrey Wiele — DATE: 1/17/2024

WITNESSED BY: Cade Nahman — DATE: 2/1/24

Voting Circuit (4)

1/22/2024

distributive law:

$L_G = PV + PS + P\bar{V}T + VST$

commutative law:

$L_G = PV + P\bar{V}T + PS + VST$

factor:

$L_G = P(V + \bar{V}T) + PS + VST$

consensus law:

$L_G = P(V + T) + PS + VST$

distributive law:

$L_G = PV + PT + PS + VST$

commutative law:

$L_G = VST + PV + PS + PT$

Simplified Expression:

$L_G = VST + PV + PS + PT$

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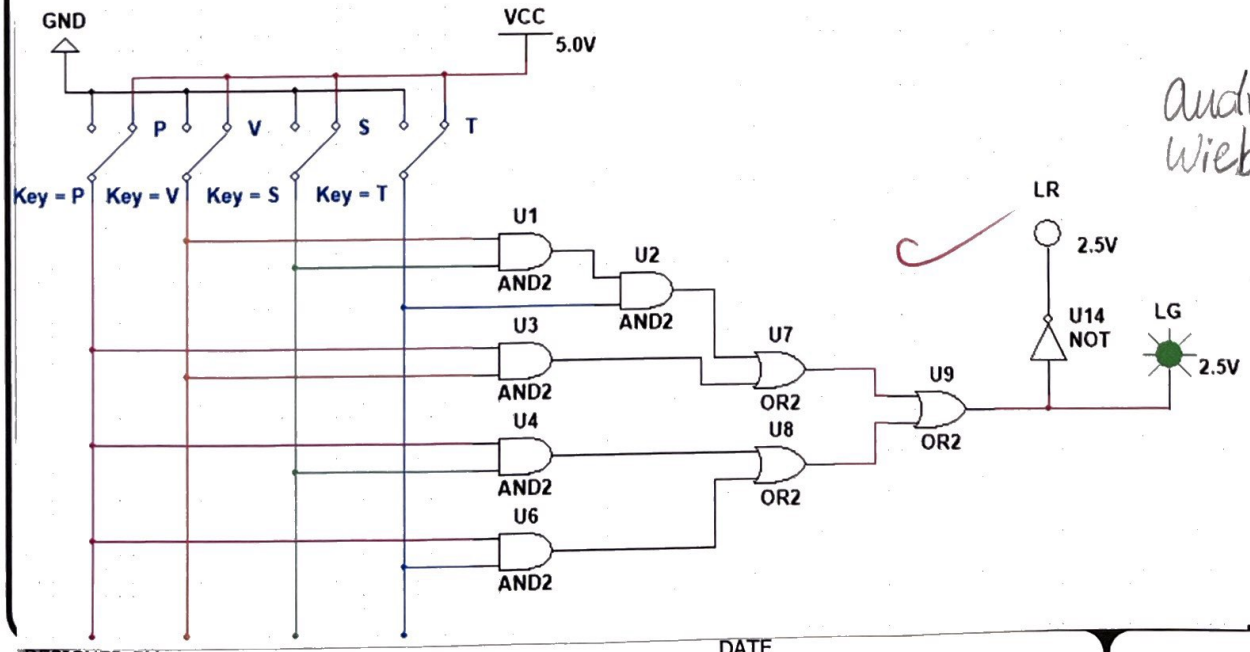
1/23/2024

Simulation: Built on Multisim

I tested every input and each of the 2 outputs matched the binary in the truth table.



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DESIGNED BY: Audrey Wiele DATE 1/23/2024

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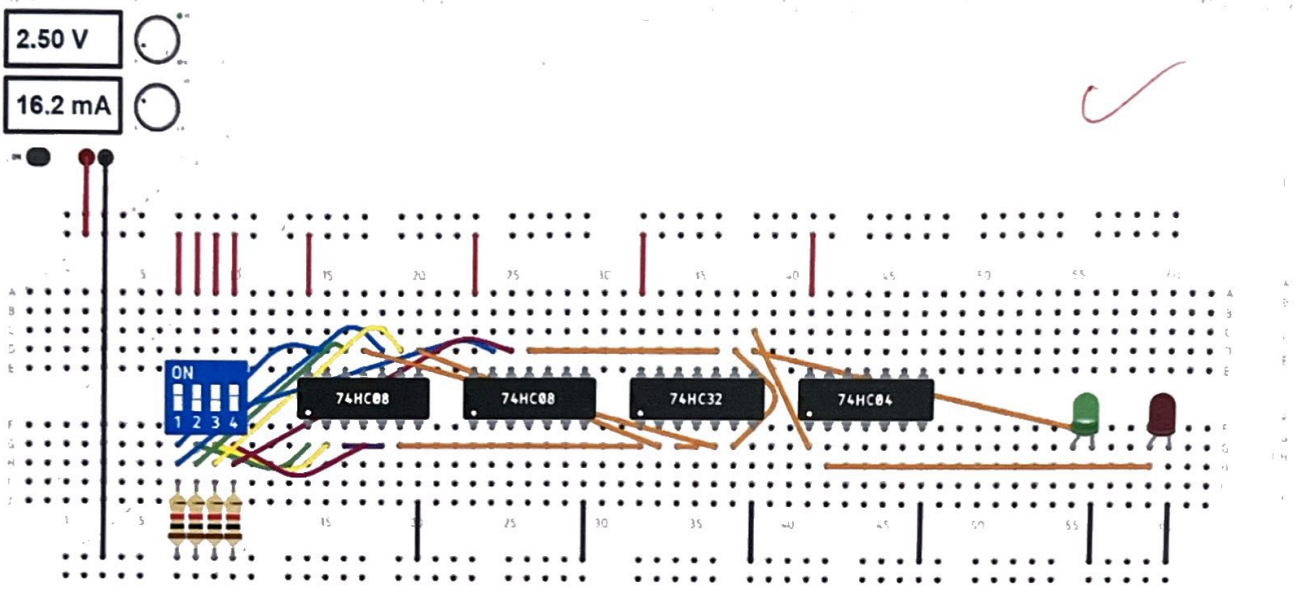
Voting Circuit (5)

1/25/2024

Tinkercad Build: I tested all of the inputs using the switches and each output matched the outputs on the truth table.



Audrey Wiebe

1/29/2024

Build Notes:

- The switches and LEDs were already built into the MyDAQ board, so we didn't need to include or power and ground them.
- One of the holes on the MyDAQ board (D19) was defective, so we began the first chip in column 22.
- We powered and grounded the buss lines in columns 6 and 7.
- We connected the S3 switch to column 15 to allow for more input holes.
- We left 4 holes between each chip.
- We used the same 4 chips as in Tinkercad (08, 08, 32, 04).
- We connected the OR output to LED G1 (LG) and the inverter output to LED R1 (LR).
- We used the following switches for each input: S3 = P, S2 = V, S1 = S, S0 = T
- We used blue wiring for all P inputs, green for all V inputs, yellow for S inputs and red for T inputs.
- We used white wire instead of orange for OR and inverter inputs and outputs.

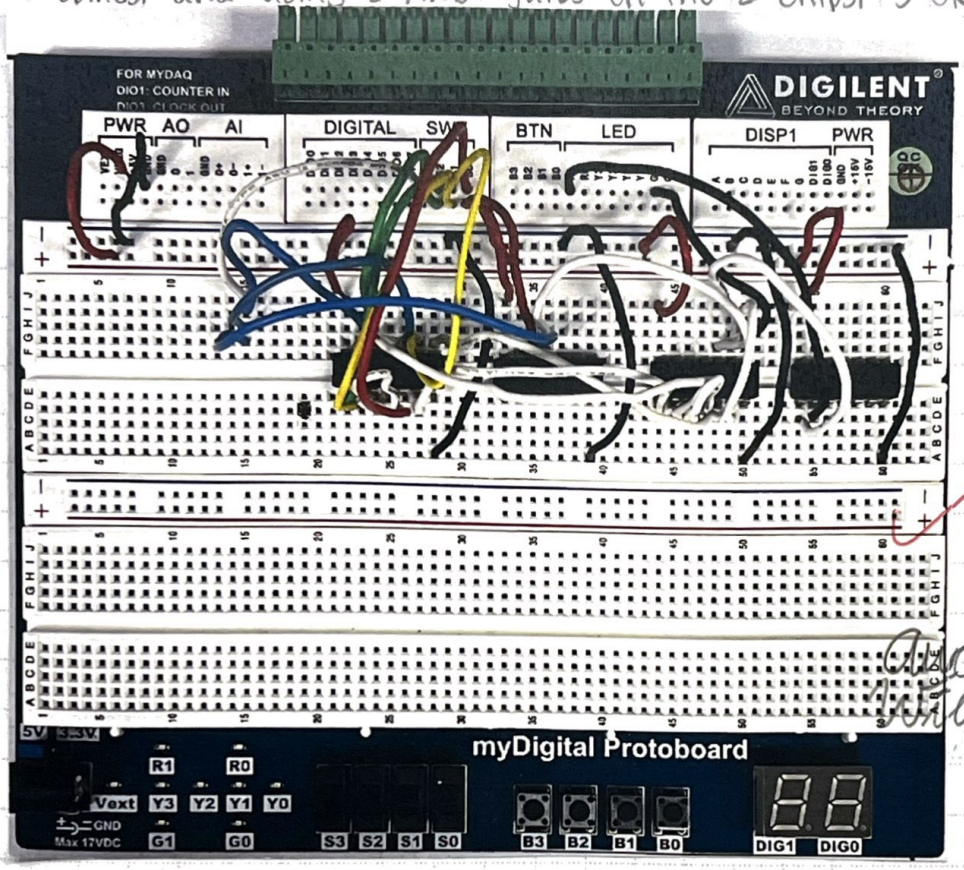
DESIGNED BY:	DATE	
Audrey Wiebe	1/29/2024	**PROPRIETARY INFORMATION**
WITNESSED BY:	DATE	All information is the property of, and solely owned by the Designer.
Cade Nahmer	2/1/2024	

Voting Circuit (6)

1/30/2024

Build Notes (cont.):

- We used black wire to connect outputs to the two LED holes.
- We built following the Tinkercad build, with the chips across the spines, and using 5 AND gates on the 2 chips, 3 OR gates, and one inverter.



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Audrey Wiele

Test Notes:

We were unable to test the MyDAQ board circuit due to technical difficulties.

1/31/2024

Conclusion:

We designed, simulated, and built a circuit that would take four inputs from a vote (P-president, V-vice president, S-secretary, T-treasurer) and output a pass (green light) or a fail (red light). We simplified the equation developed from the truth table using Boolean Algebra, and ended up with 5 2-input AND gates, 3 2-input OR gates, and an inverter to connect to the red light. When building on Tinkercad, we

DID IT WORK? —(

DESIGNED BY: Audrey Wiele DATE 1/31/2024

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Voting Circuit (7)

2/1/2024

Conclusion (cont.):

had a hard time distinguishing which wires were connected to which switches, so we color coded the wires for each of the 4 inputs. ✓ When building on the MyDAQ board, we ran out of inputs for the S3 switch or P. We decided to connect an input to column 15, so any other wires for P could be connected to the holes in column 15. If given more time, we would test our circuit to see if the correct LED turned on according to the truth table. We could also redesign the circuit to account for a third LED that would light up when the votes are tied, symboling to conduct a second vote. ✓

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19/20

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