ECE 310-001

Project #1 Report

Your Name Here

1. Snapshot of the RTL synthesized in Quartus.

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*Part 1: Fill in the synthesis results*

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| **Synthesis Results** |
| Number of logic elements: 29440 |
| Number of registers: 29440 |
|  |
| Number of memory bits: 1105920 |
| Frequency the design can run at: No paths to report? |
| Do you see any synthesis errors? Why? ( One line explanation is fine )  No synthesis errors |

**Name: Calvin Jiang Student ID: 200306705**

I certify that I did not copy the answers to this homework and did not let

anyone copy my answers (sign):

Calvin Jiang

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