1_ La Gal usa Tecnologia EECMOS, de modo que es reprogramable
En cambio la PAL no es reprogramable

2_

a_ V	b_ V	C_ F	d_ V
e_ V	F_ V	G_ F	H_ F

3_

```
entity sumador_completo is
   Port ( A, B, Cin : in Bit;
          suma, Cout : out Bit )
end Sumador_completo;
```

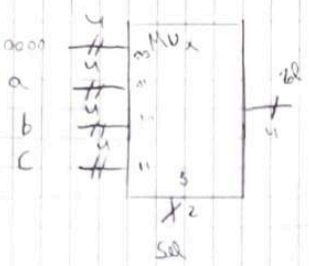
a_

```
architecture Resultado of sumador_completo is
begin
   Suma <= A xor B xor Cin ;
   Cout <= (A and B) or (A and Cin) or (B and Cin);
end Resultado;
```

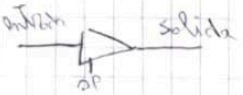
b_

```
architecture Resultado of sumador_completo is
signal X : std_logic_vector (2 downto 0);
begin
  X <= (A & B & Cin) ;
  process (X)
  begin
     Case X is
        When "000" => suma <= '0' ; Cout <= '0' ;
        When "001" => suma <= '1' ; Cout <= '0' ;
        When "010" => Suma <= '1' ; Cout <= '0' ;
        When "011" => suma <= '0' ; Cout <= '1' ;
        When "100" => suma <= '1' ; Cout <= '0' ;
        When "101" => suma <= '0' ; Cout <= '1' ;
        When "110" => suma <= '0' ; Cout <= '1' ;
        When "111" => suma <= '1' ; Cout <= '1' ;
     end case;
  end process;
end Resultado;
```

4. a -



b. Tri-state



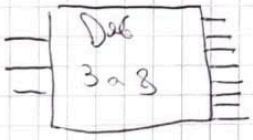
5. 1er Tipo: Lógica. Este bloque es entrega de las publicaciones

2do Tipo: Entradas y salidas

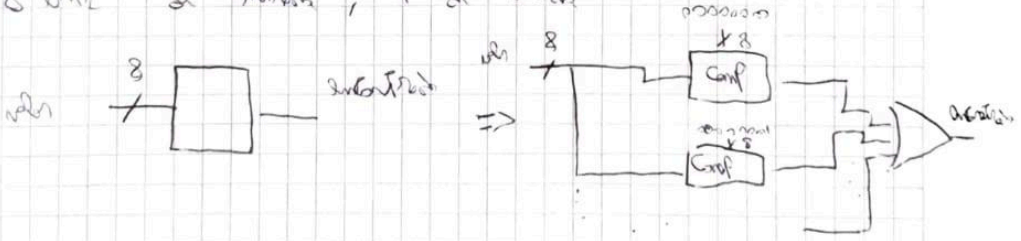
3er Tipo: interconexiones: se programan para conectar la lógica con las entradas y salidas

6. Es un lenguaje programable y no es secuencial

7. -



8. - 8 bits de entrada, 1 de salida



b. Es combinacional ya que no depende de un CLK

c. $f_{max} = 1/\tau_{comp} + \tau_{or}$

d. Se necesitarían 100 registros, uno por cada numero a comparar