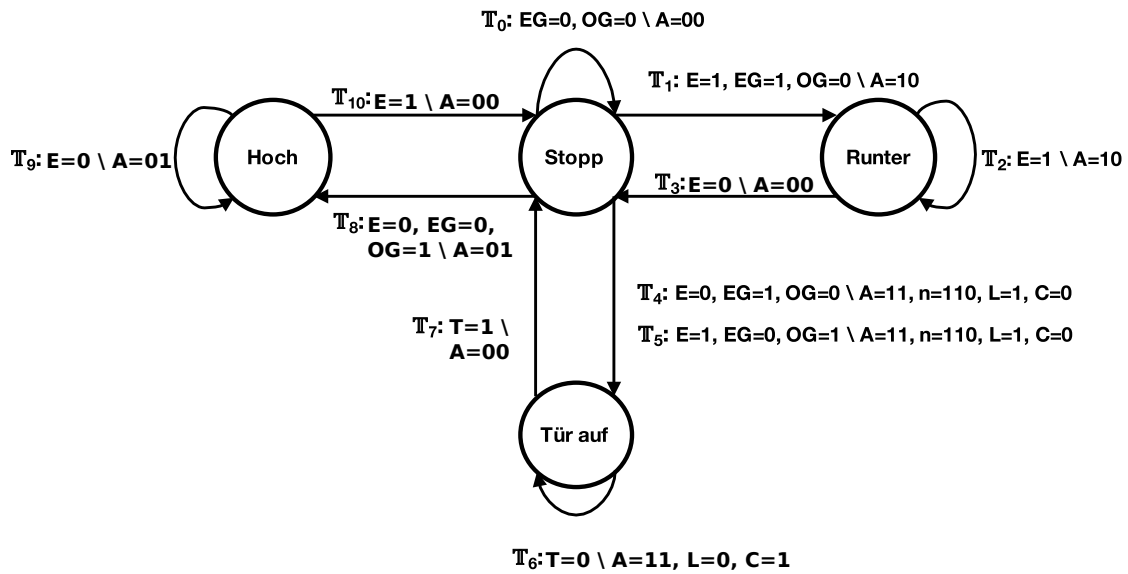


# Grundlagen der Rechnerarchitektur

Tim Luchterhand, Paul Nykiel (Abgabegruppe 117)

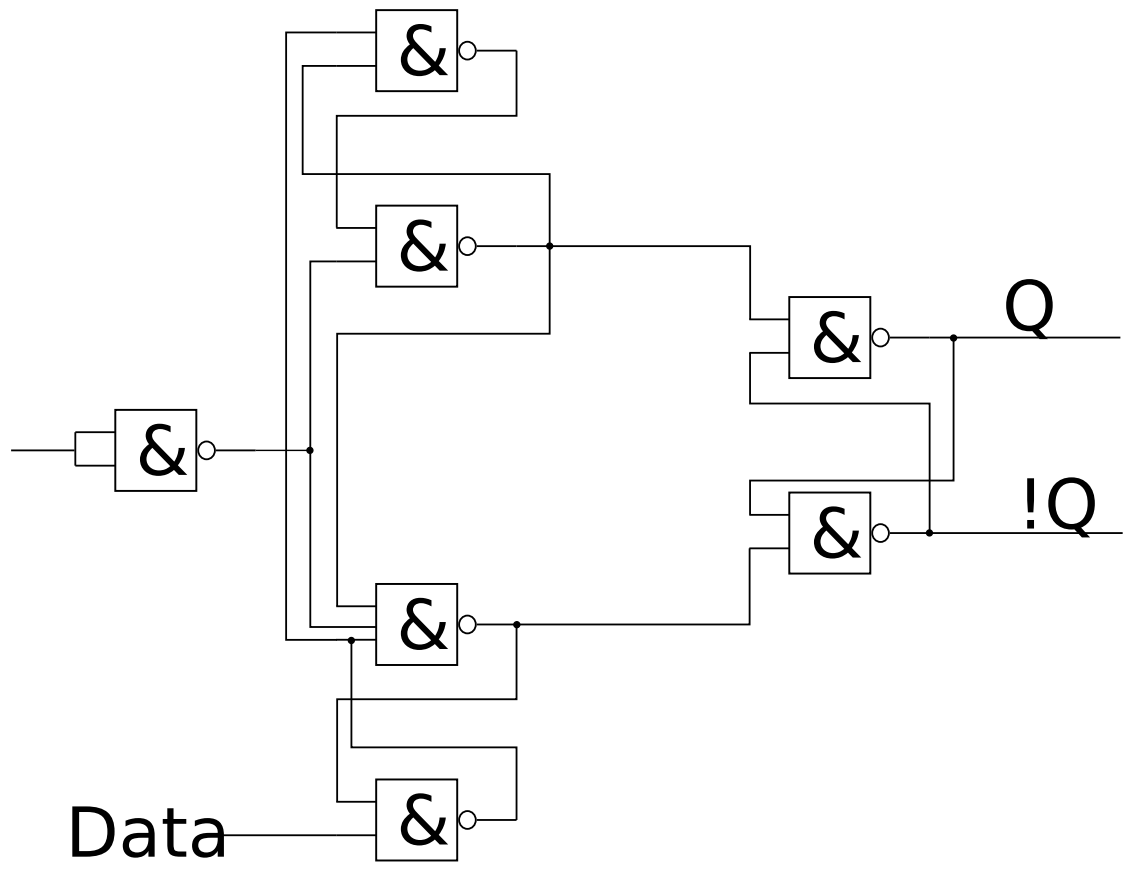
18. Januar 2019

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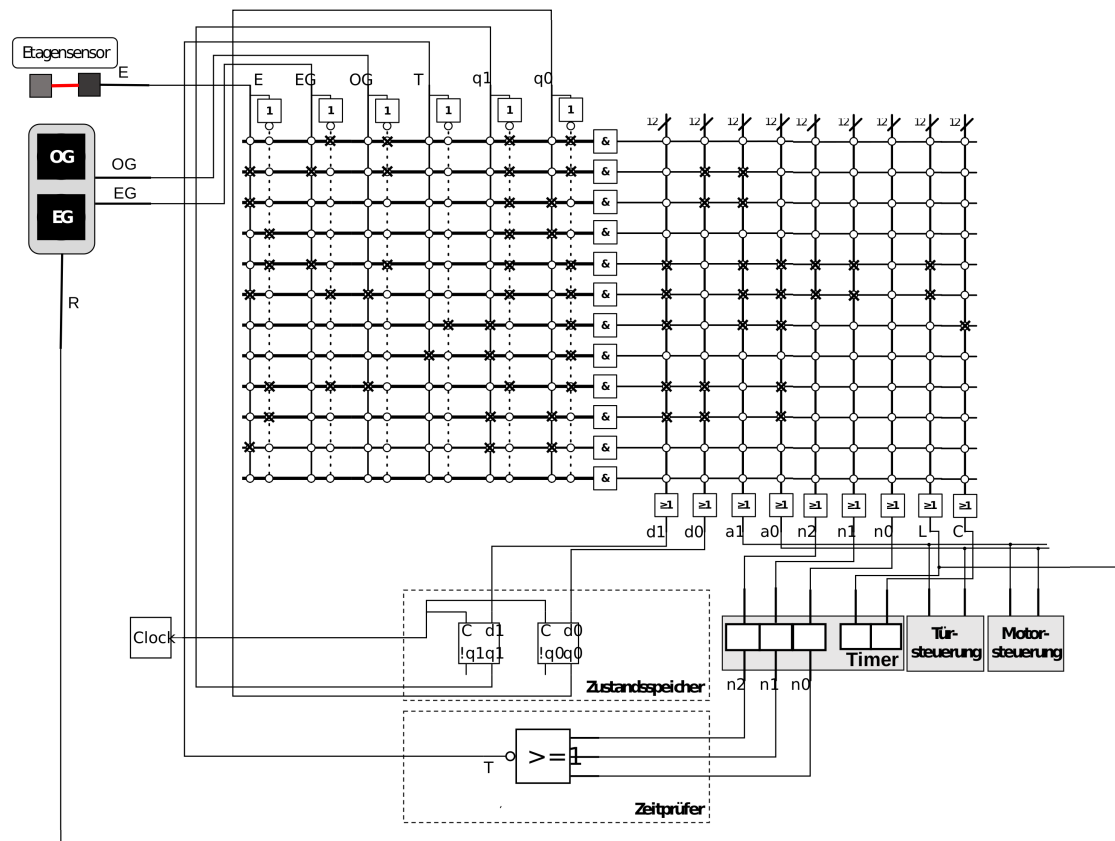


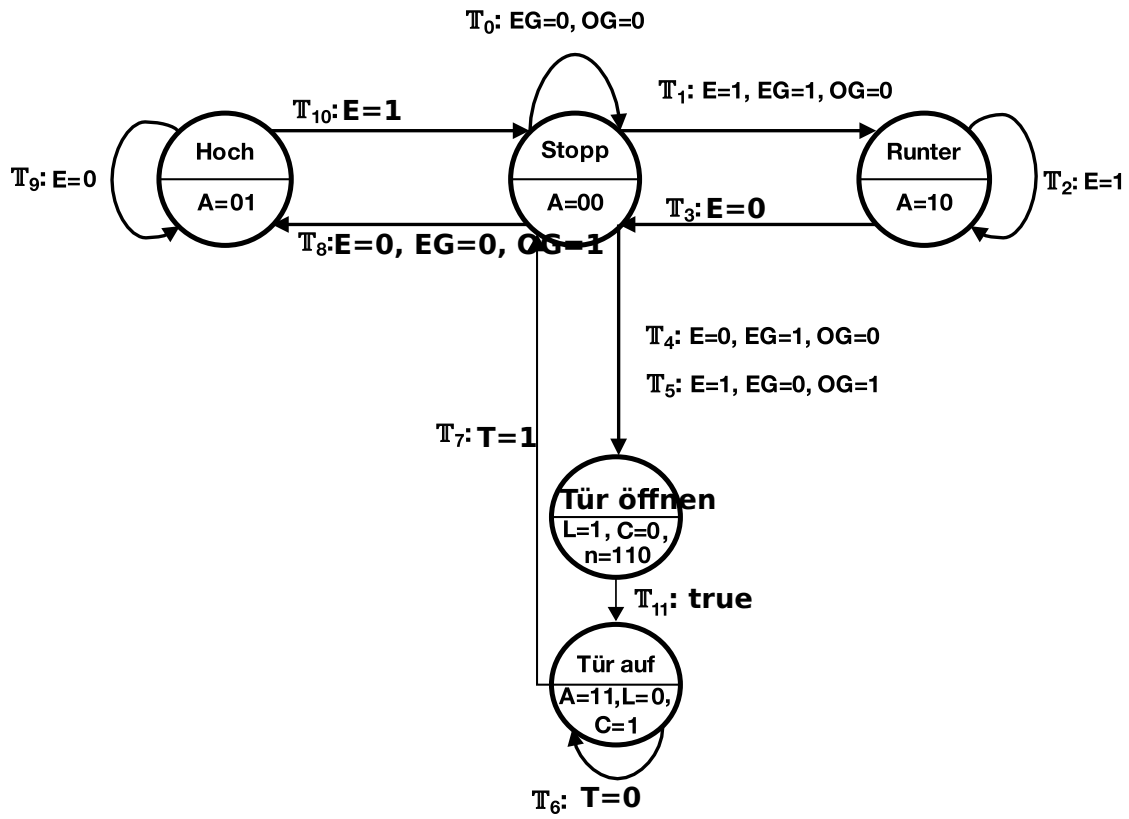
Transition T	Etagen- sensor E	Fahrstuhl- panel		Zeit- Prüfer T	Zustand		Folge- zustand	
		EG	OG		q <sub>1</sub>	q <sub>0</sub>	d <sub>1</sub>	d <sub>0</sub>
T <sub>0</sub>	d	0	0	d	0	0	0	0
T <sub>1</sub>	1	1	0	d	0	0	0	1
T <sub>2</sub>	1	d	d	d	0	1	0	1
T <sub>3</sub>	0	d	d	d	0	1	0	0
T <sub>4</sub>	0	1	0	d	0	0	1	0
T <sub>5</sub>	1	0	1	d	0	0	1	0
T <sub>6</sub>	d	d	d	0	1	0	1	0
T <sub>7</sub>	d	d	d	1	1	0	0	0
T <sub>8</sub>	0	0	1	d	0	0	1	1
T <sub>9</sub>	0	d	d	d	1	1	1	1
T <sub>10</sub>	1	d	d	d	1	1	0	0

Ausgang		Timer					
a <sub>1</sub>	a <sub>0</sub>	n <sub>2</sub>	n <sub>1</sub>	n <sub>0</sub>	L	C	
0	0	d	d	d	d	d	
1	0	d	d	d	d	d	
1	0	d	d	d	d	d	
0	0	d	d	d	d	d	
1	1	1	1	0	1	0	
1	1	1	1	0	1	0	
1	1	d	d	d	0	1	
0	0	d	d	d	d	d	
0	1	d	d	d	d	d	
0	1	d	d	d	d	d	
0	0	d	d	d	d	d	



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Transition	Etagen- sensor	Fahrstuhl- panel		Zeit- Prüfer	Zustand		Folge- zustand	
T	E	EG	OG	T	q <sub>1</sub>	q <sub>0</sub>	d <sub>1</sub>	d <sub>0</sub>
T <sub>0</sub>	d	0	0	d	0	0	0	0
T <sub>1</sub>	1	1	0	d	0	0	0	1
T <sub>2</sub>	1	d	d	d	0	1	0	1
T <sub>3</sub>	0	d	d	d	0	1	0	0
T <sub>4</sub>	0	1	0	d	0	0	1	0
T <sub>5</sub>	1	0	1	d	0	0	1	0
T <sub>6</sub>	d	d	d	0	1	0	1	0
T <sub>7</sub>	d	d	d	1	1	0	0	0
T <sub>8</sub>	0	0	1	d	0	0	1	1
T <sub>9</sub>	0	d	d	d	1	1	1	1
T <sub>10</sub>	1	d	d	d	1	1	0	0

Ausgang		Timer					
a <sub>1</sub>	a <sub>0</sub>	n <sub>2</sub>	n <sub>1</sub>	n <sub>0</sub>	L	C	
0	0	d	d	d	d	d	
1	0	d	d	d	d	d	
1	0	d	d	d	d	d	
0	0	d	d	d	d	d	
1	1	1	1	0	1	0	
1	1	1	1	0	1	0	
1	1	d	d	d	0	1	
0	0	d	d	d	d	d	
0	1	d	d	d	d	d	
0	1	d	d	d	d	d	
0	0	d	d	d	d	d	