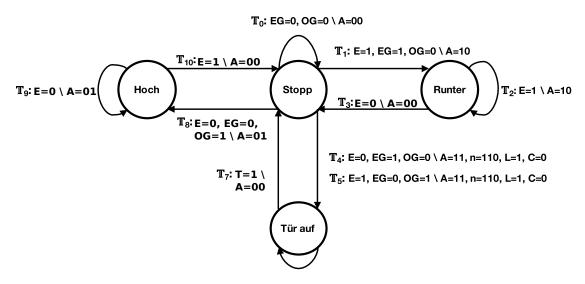
Grundlagen der Rechnerarchitektur

Tim Luchterhand, Paul Nykiel (Abgabegruppe 117)

18. Januar 2019

1



Transition	Etagen- sensor	Fahrstuhl- panel		Zeit- Prüfer	Zustand		Folge- zustand	
T	E	EG	OG	Т	q ₁	\mathbf{q}_{0}	d₁	d_0
To	d	0	0	d	0	0	0	0
\mathbf{T}_1	1	1	0	d	0	0	0	1
\mathbb{T}_2	1	d	d	d	0	1	0	1
Т3	0	d	d	d	0	1	0	0
T ₄	0	1	0	d	0	0	1	0
T ₅	1	0	1	d	0	0	1	0
\mathbb{T}_6	d	d	d	0	1	0	1	0
${f T}_7$	d	d	d	1	1	0	0	0
Т8	0	0	1	d	0	0	1	1
Т9	0	d	d	d	1	1	1	1
T ₁₀	1	d	d	d	1	1	0	0

Ausgang		Timer							
a ₁	\mathbf{a}_0	n ₂	n ₁	n ₀	L	С			
0	0	d	d	d	d	d			
1	0	d	d	d	d	d			
1	0	d	d	d	а	d			
0	0	d	d	d	d	d			
1	1	1	1	0	1	0			
1	1	1	1	0	1	0			
1	1	d	d	d	0	1			
0	0	d	d	d	d	d			
0	1	d	d	d	d	d			
0	1	d	d	d	d	d			
0	0	d	d	d	d	d			