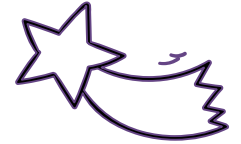
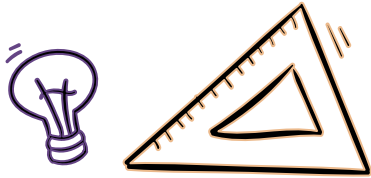




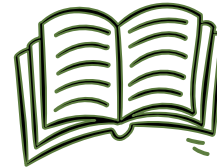
تصميم الدارات الإلكترونية بالحاسوب



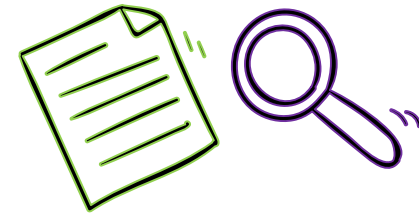
Computer Design of Electronic Circuits



إعداد: د. علا جزماتي



السنة الرابعة قسم التحكم والأتمتة
العام الدراسي 2023-2024



المحاضرة السابعة

محتويات المقرر

1. مدخل إلى أهمية تطوير أدوات التصميم باستخدام الحاسب (Introduction to The Need of Developing CAD Tools)
2. تصنيف عام لأنواع أدوات التصميم (General Classification of CAD Tools Used in Electronic Systems Design)
3. مدخل إلى اللغات المستخدمة في التصميم (Introduction to Design Languages VHDL, Verilog, Verilog System, ..)
4. مدخل إلى مراحل بناء النظم الرقمية (Introduction to Digital Systems Synthesis)
5. مرحلة البناء منخفض المستوى (Low Level Synthesis)
6. تصميم الدارات المتكاملة للنظم عالية التكامل (Layout Design for VLSI Systems)
7. تطبيقات تصميمية (Design Applications)
8. اتجاهات التطور الحديثة (Trends and New Directions)



من أهم أدوات تصميم
ومحاكاة دارات CMOS
باستخدام الحاسب

Microwind

...CMOS layout design & simulation tool



...giving you the squeeze of
nanometer technology

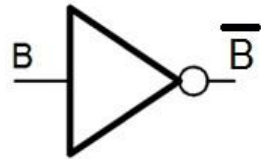
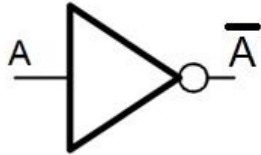
μ wind[®]

A Layout and Simulation tool for deep sub-micron CMOS design

دائرة نصف الجامع (Half Adder)

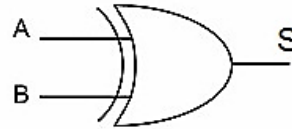


Sum-CMOS design

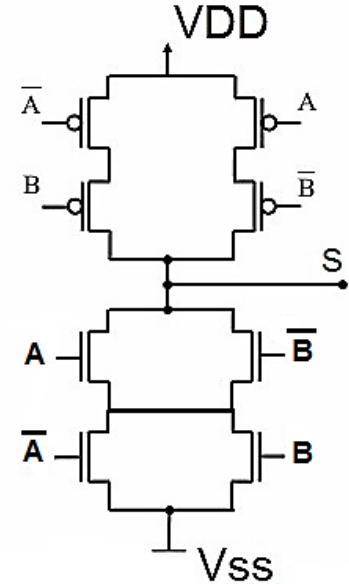


Truth Table

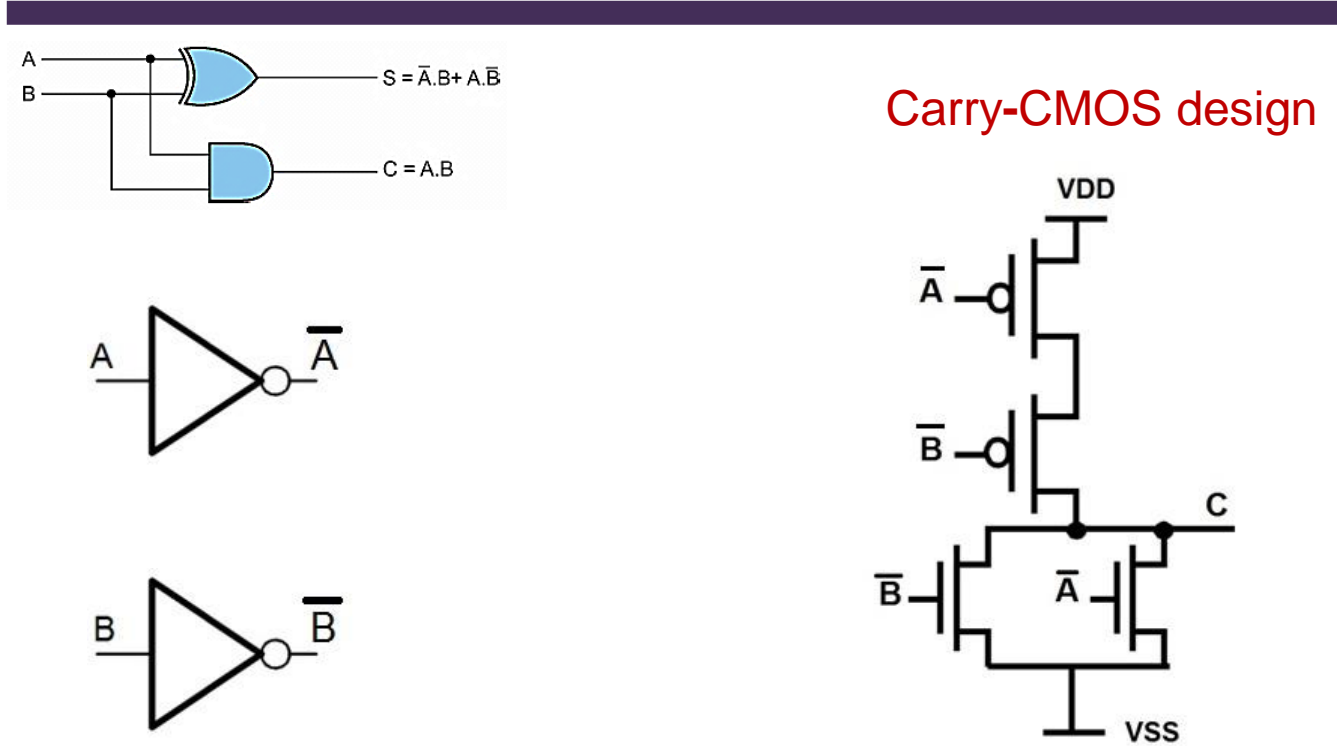
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0



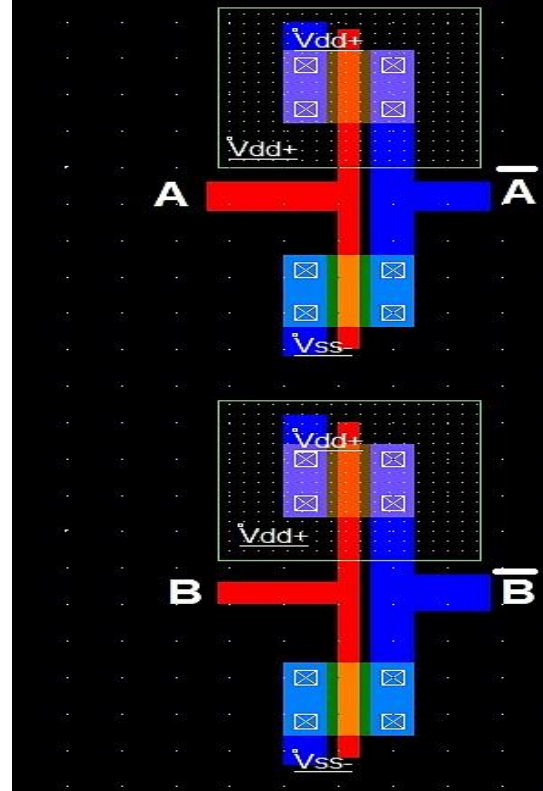
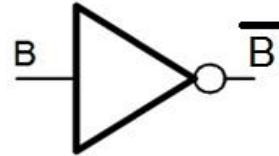
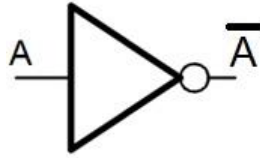
$$S = \bar{A} \cdot B + A \cdot \bar{B} = A \oplus B$$

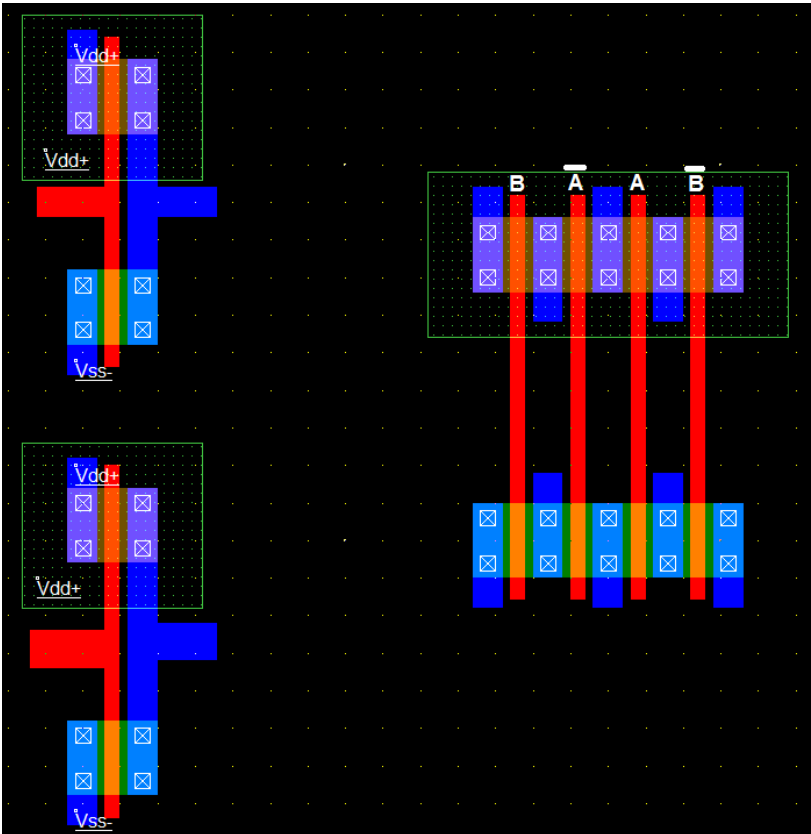
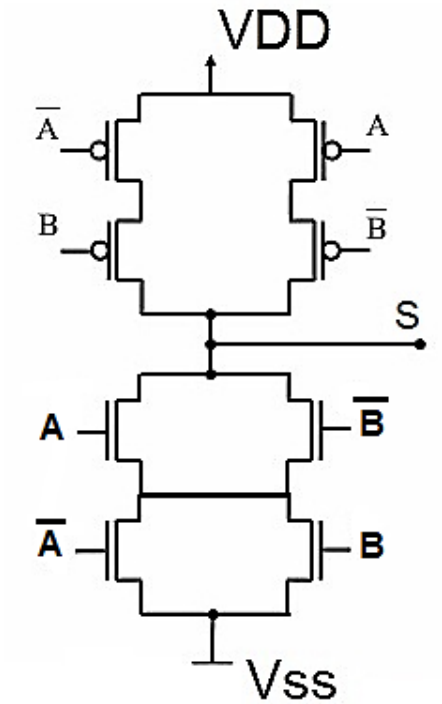


دائرة نصف الجامع (Half Adder)

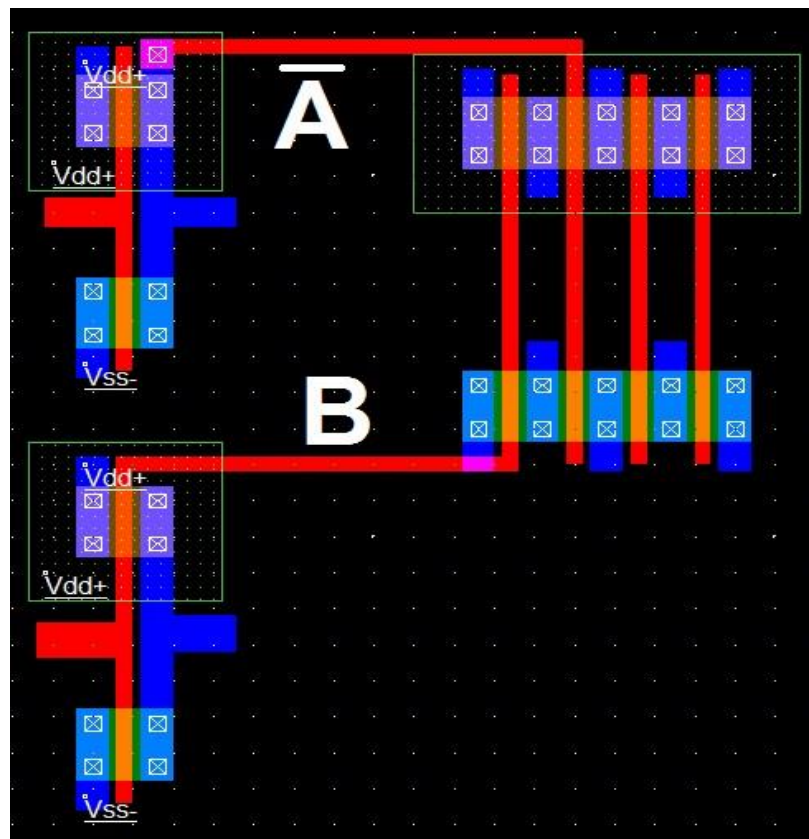
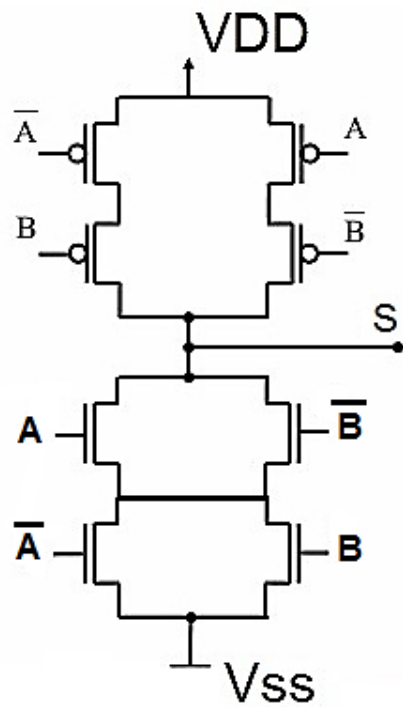


بوابة العاكس (Inverter)

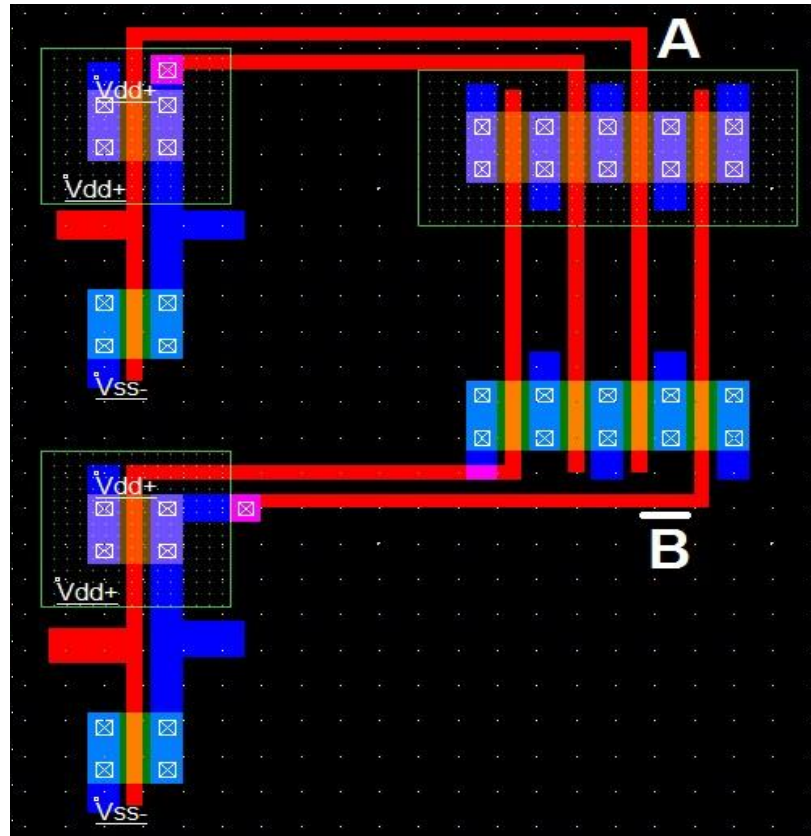
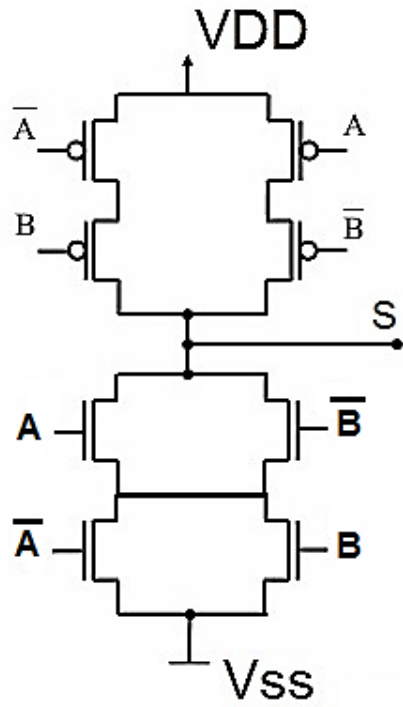




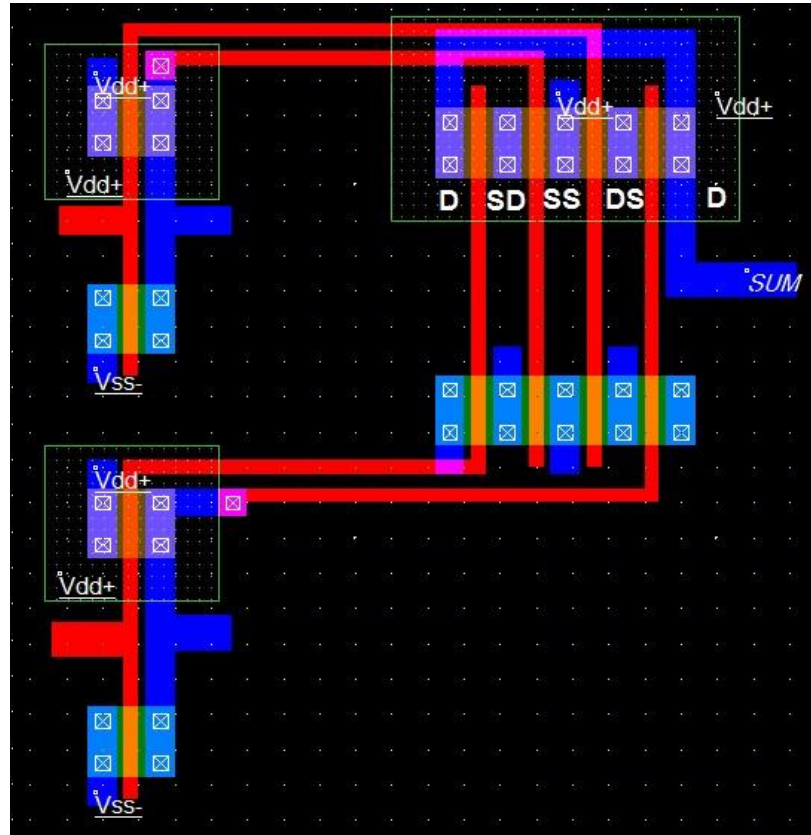
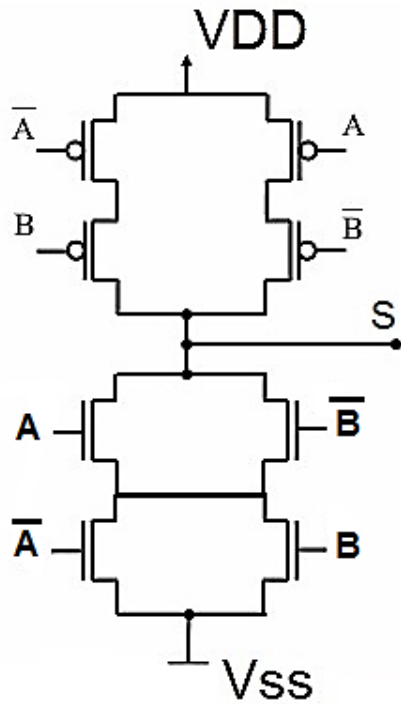
(Sum)



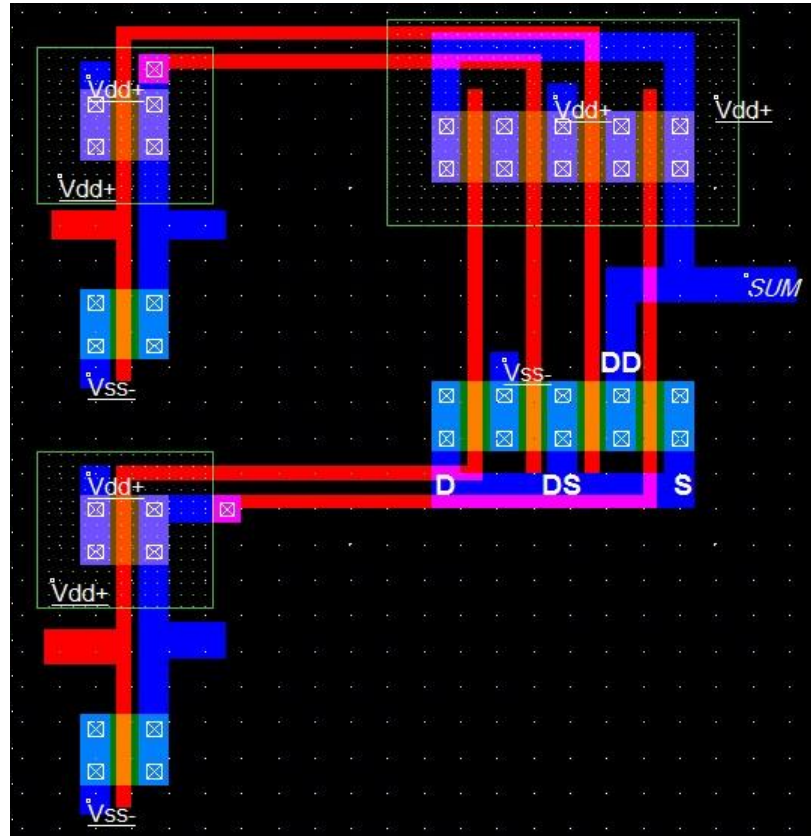
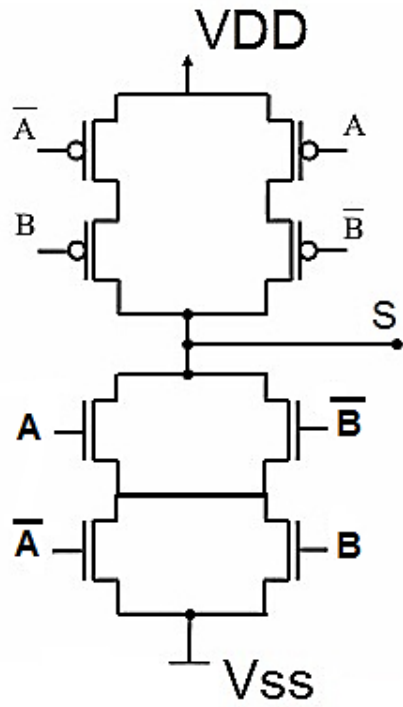
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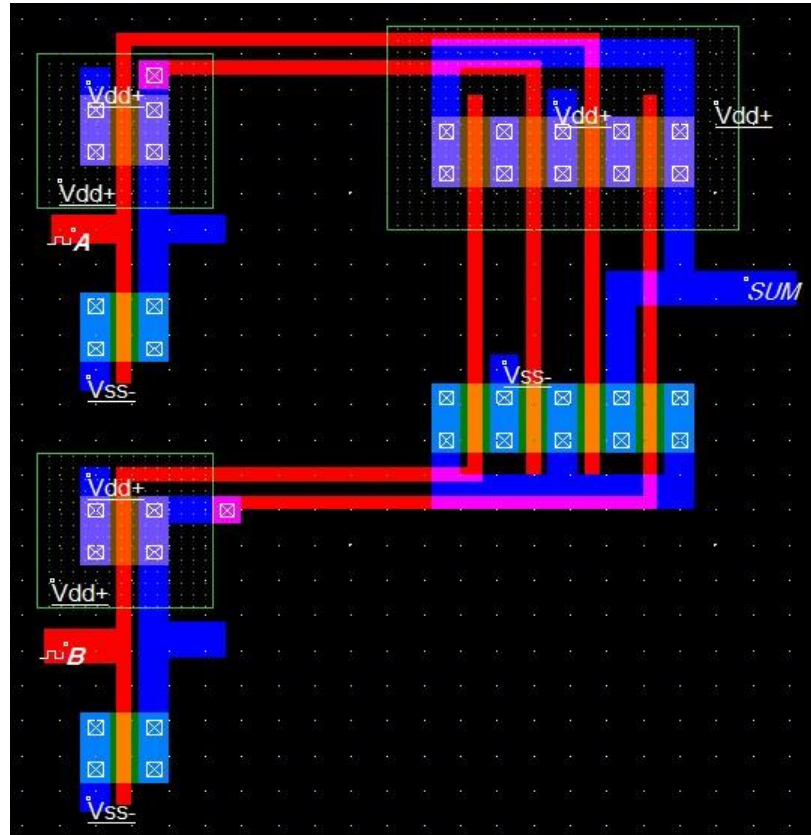
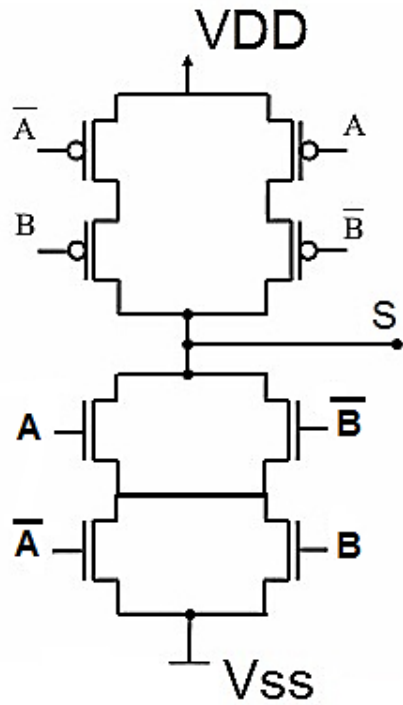
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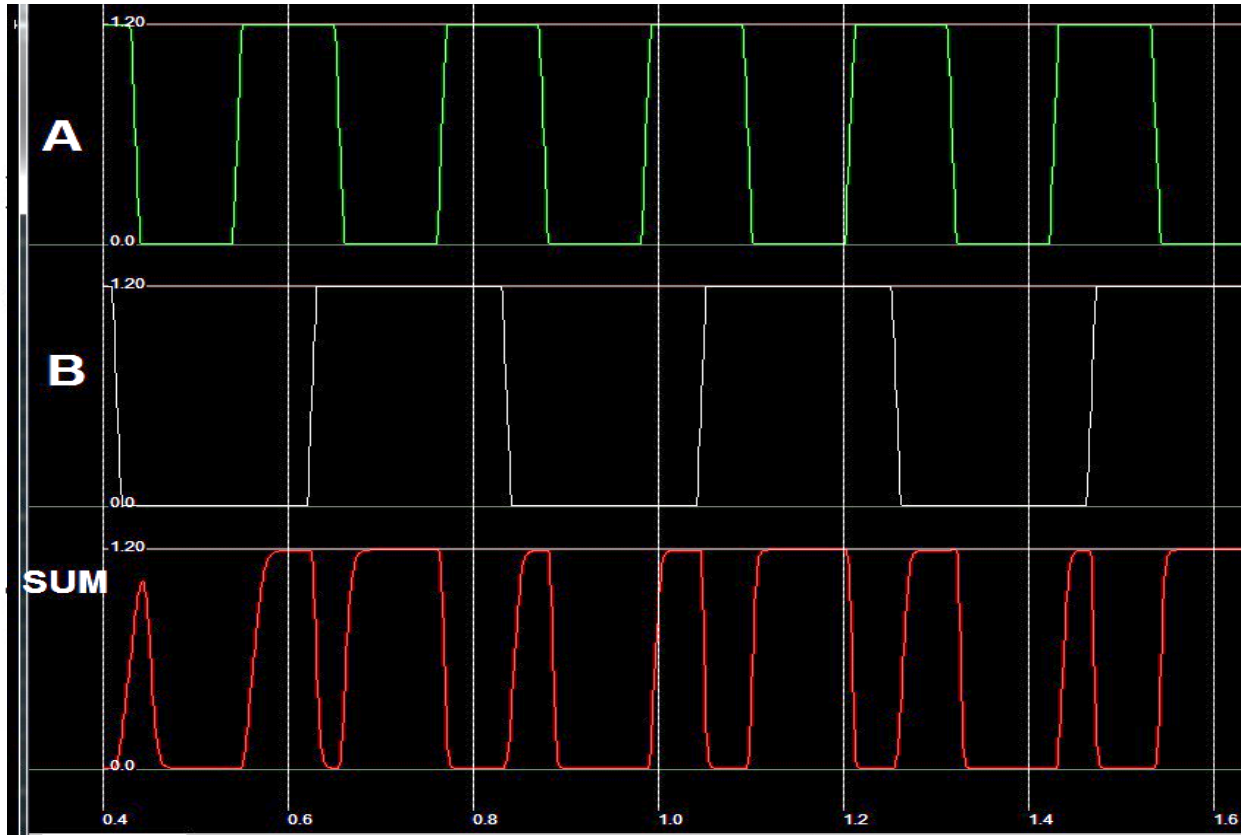
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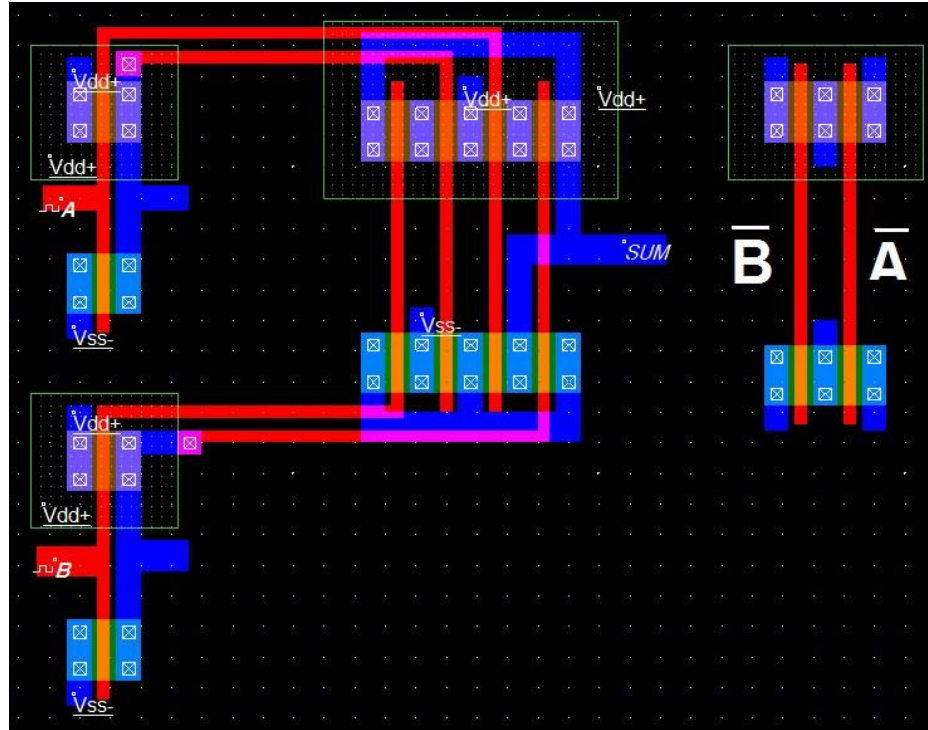
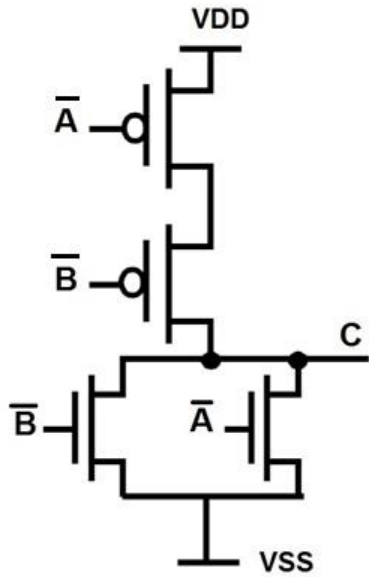
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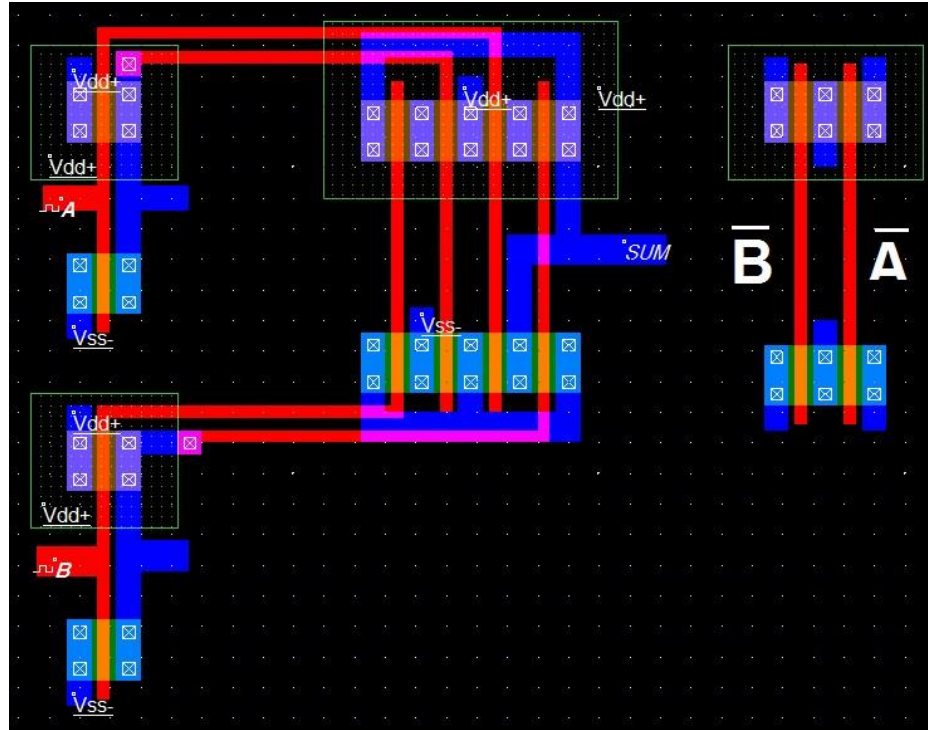
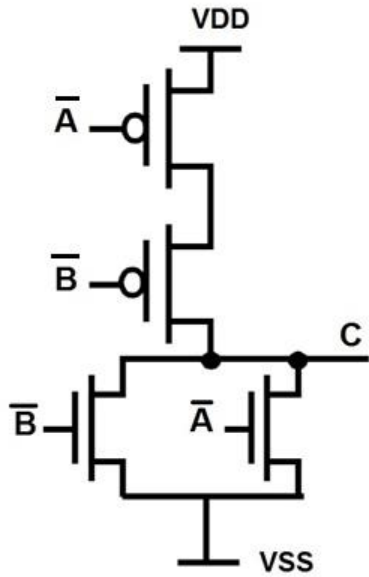
(Sum)



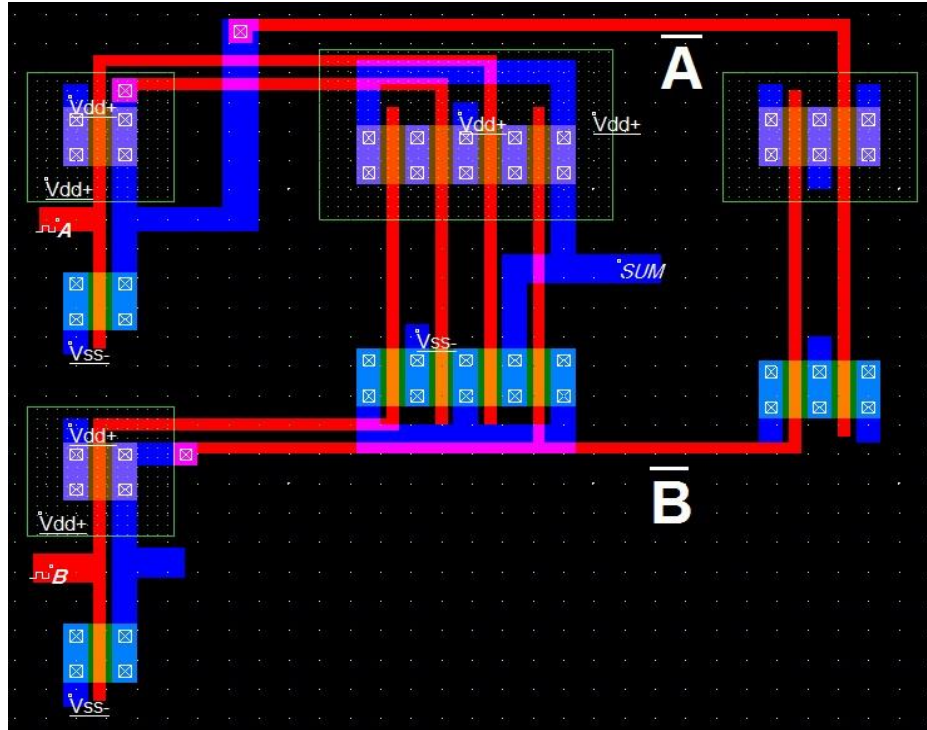
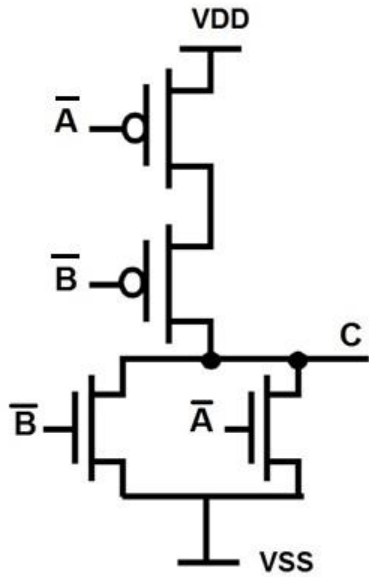
(Carry)



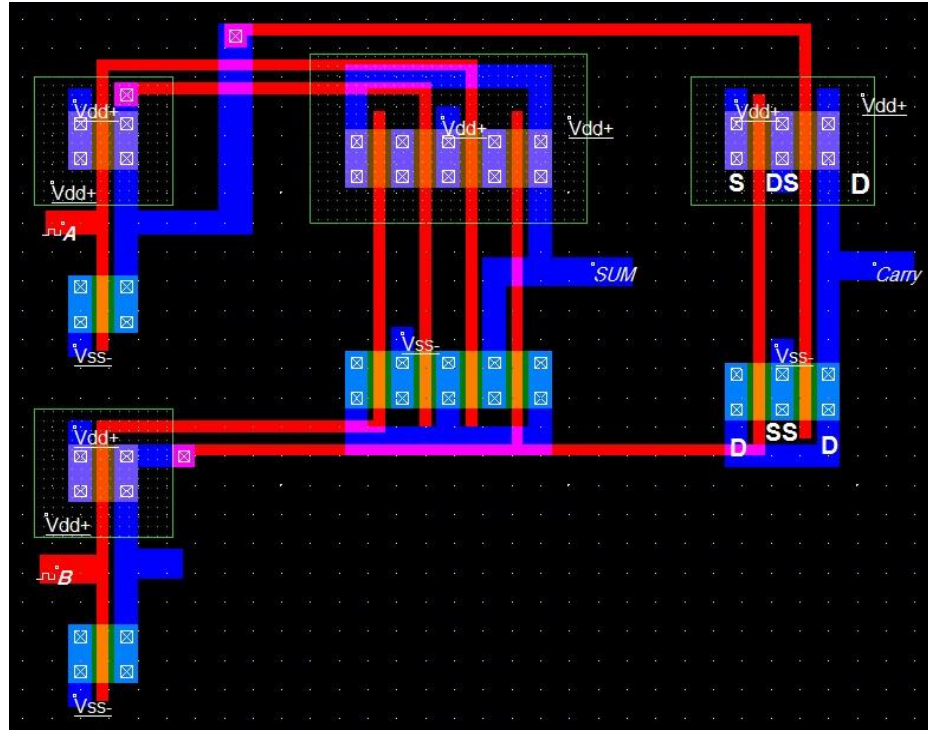
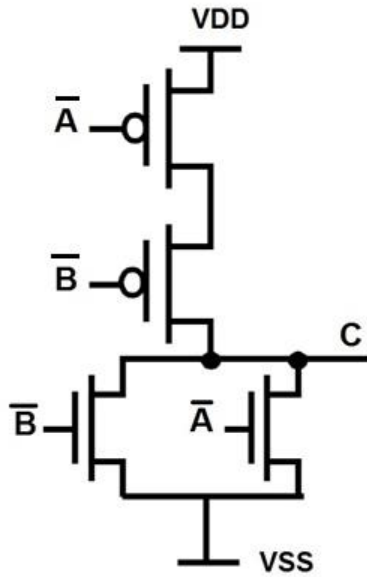
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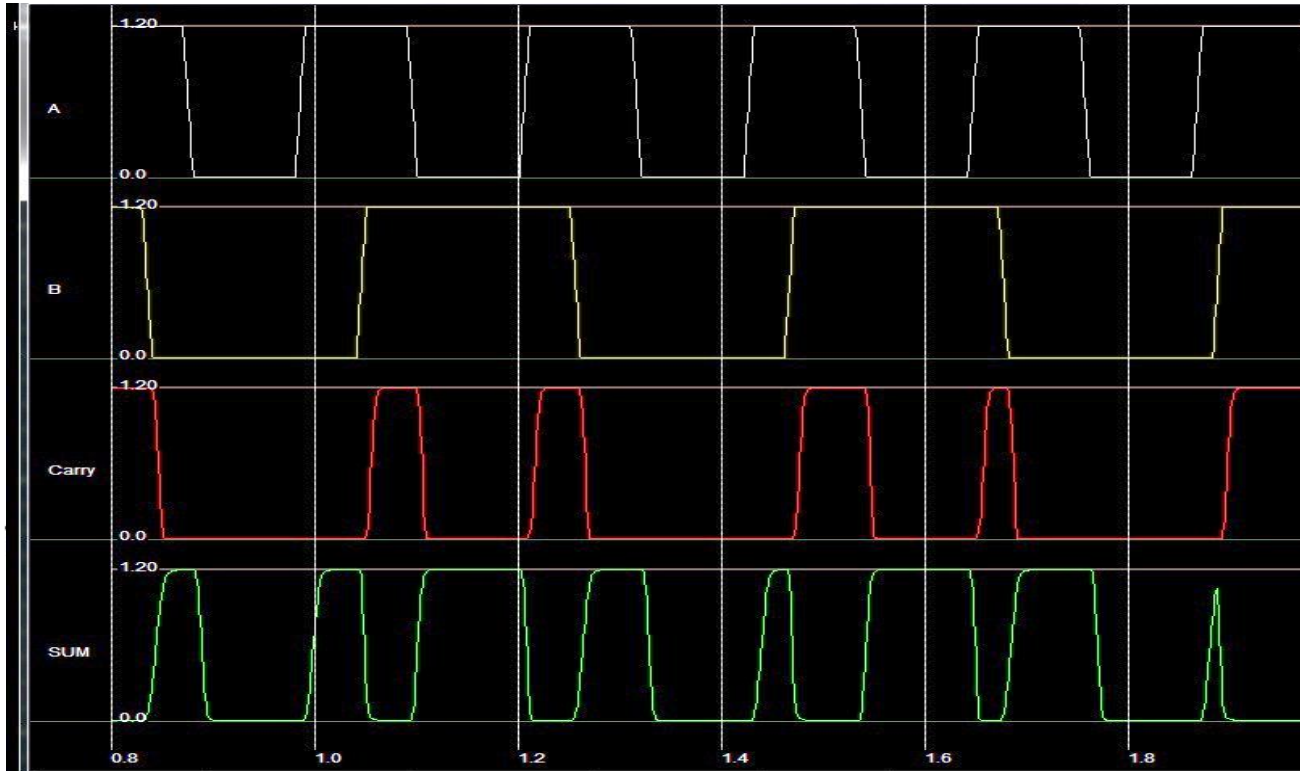
(Carry)



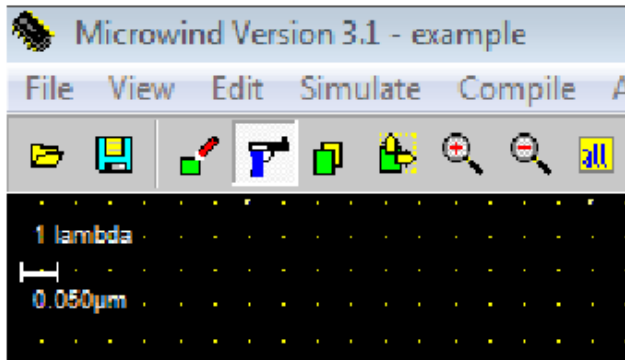
(Carry)



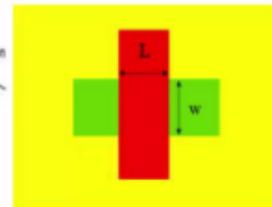
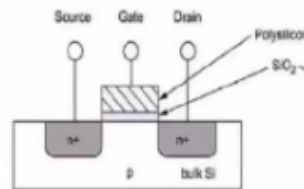
(Carry)



كلما التزمنا بقواعد التصميم الصحيح نستهلك سيليكون أقل



↑ عدد العناصر على الشريحة:



CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V, 2.50V)

The Microwind main screen shown in Figure 2.19 includes two windows: one for the main menu and the layout display, and the other for the icon menu and the layer palette. The main layout window features a grid, scaled in lambda (λ) units. The size of the grid constantly adapts to the layout. In Figure 2.19, the grid is 5 lambda. The lambda unit is fixed to half of the minimum available lithography of the technology, i.e. $L_{min}/2$. For example, the default technology is a CMOS six-metal layers 0.12 μm technology, consequently lambda is 0.06 μm .

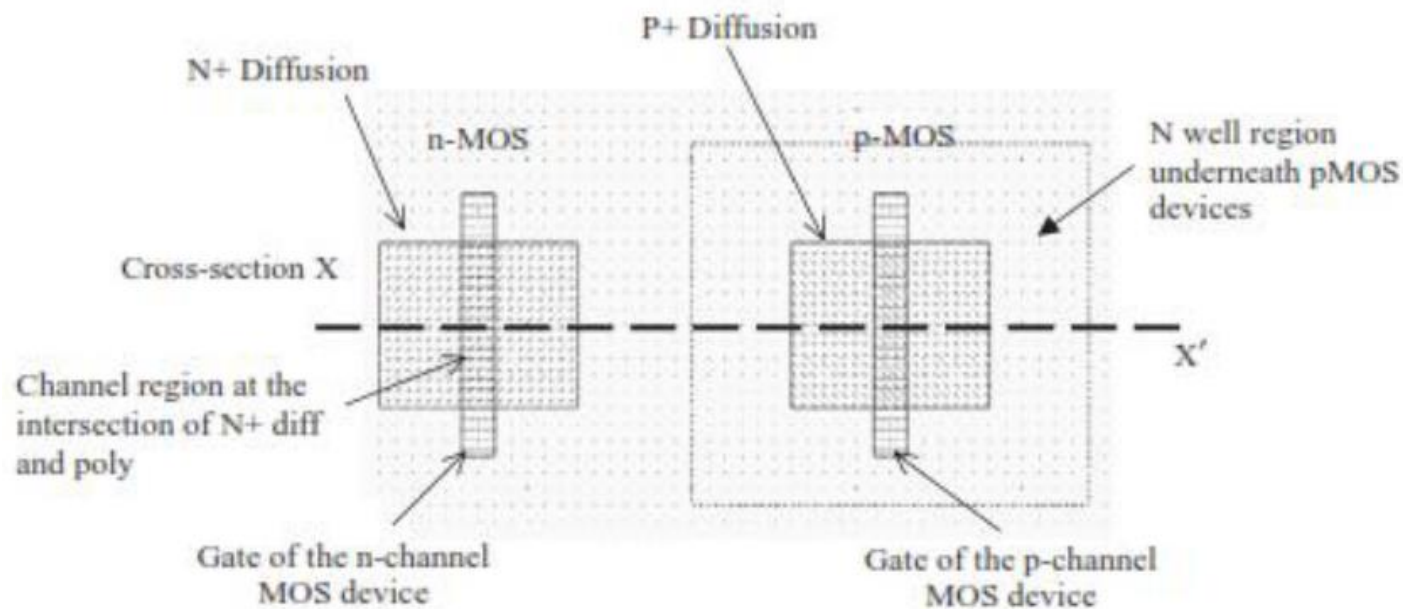
$$\lambda = \frac{L_{min}}{2}$$

(Equation 2.2)

$$F = V/\lambda$$

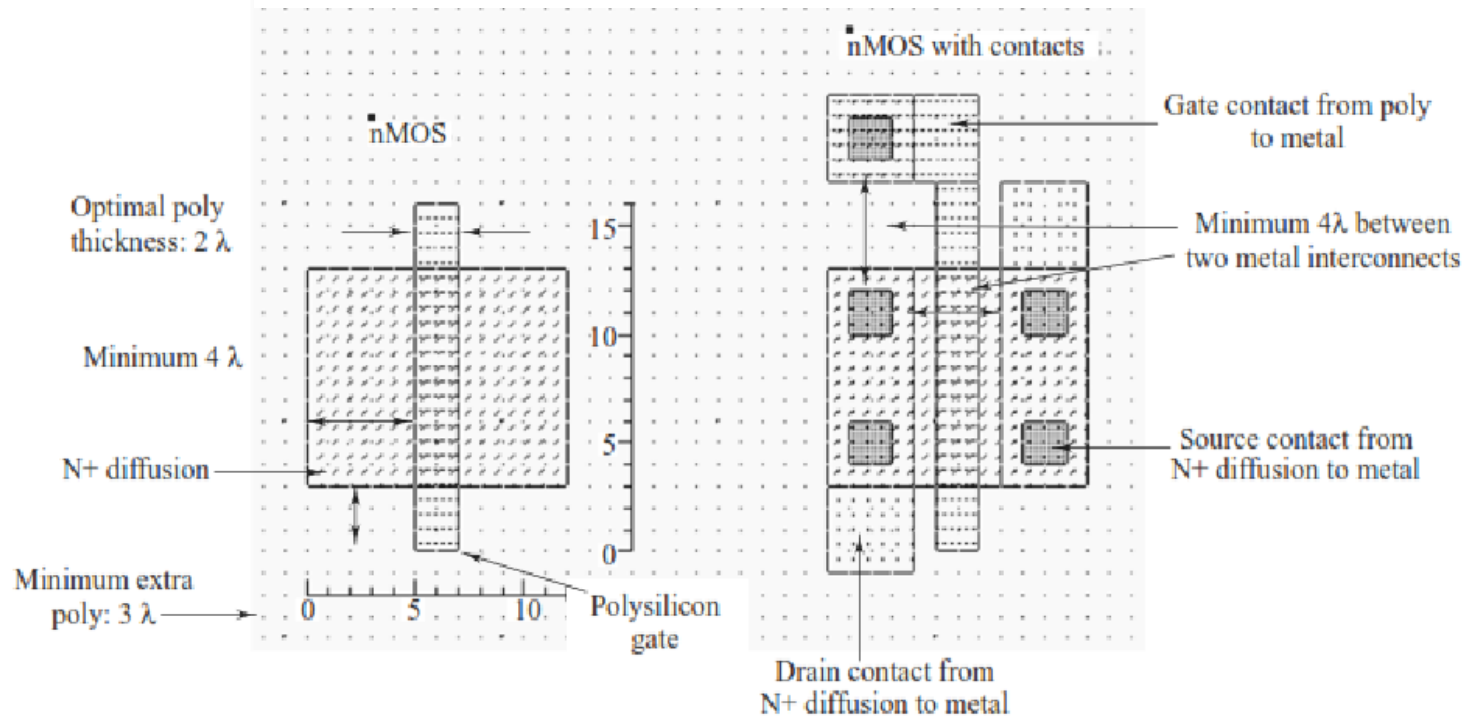
↑ التردد:

Layout



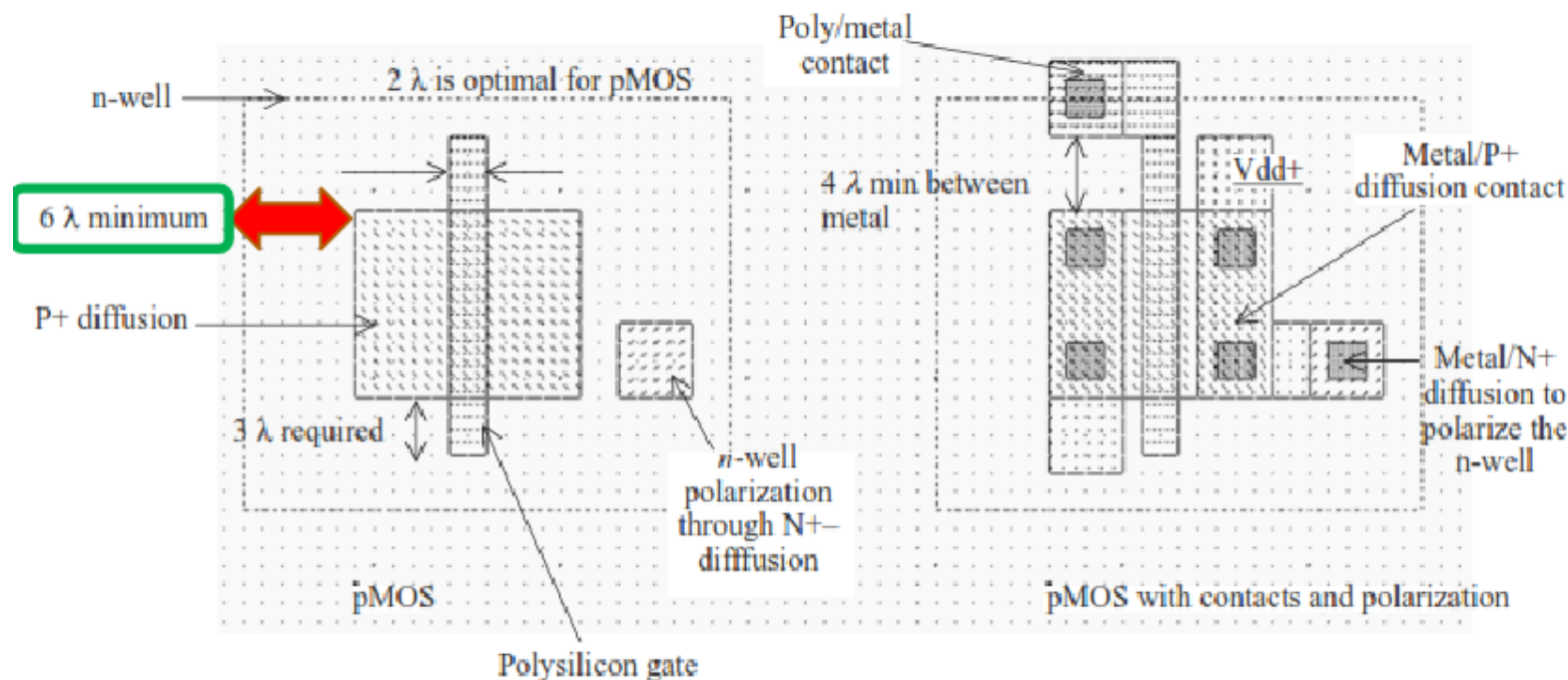
Bird's eye view of the n-channel and p-channel MOS device layout (allMosDevices.MSK)

الأبعاد المثالية للترانزستور nmos

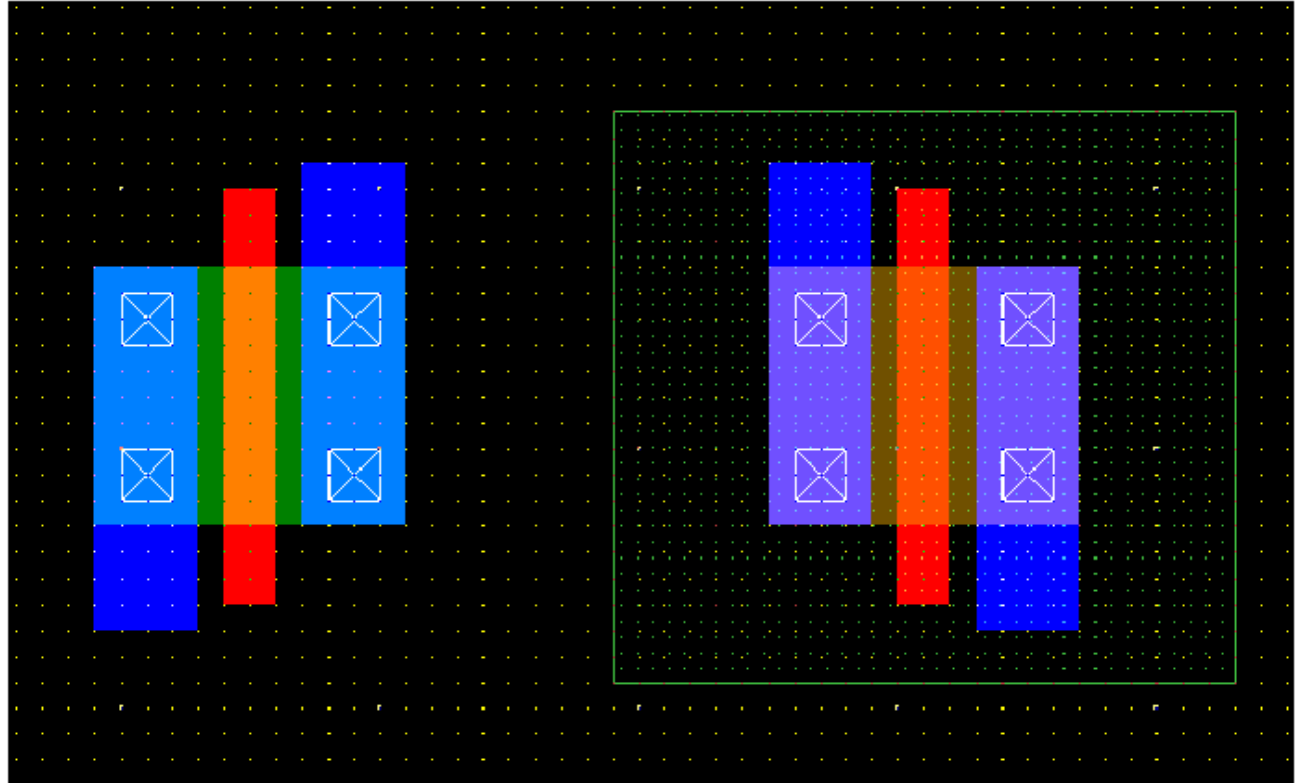
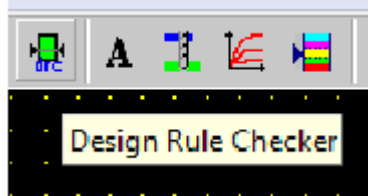
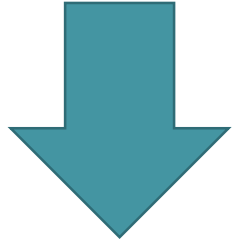


Creating the n-channel MOS transistor and adding contacts (AllMosDevices.MSK)

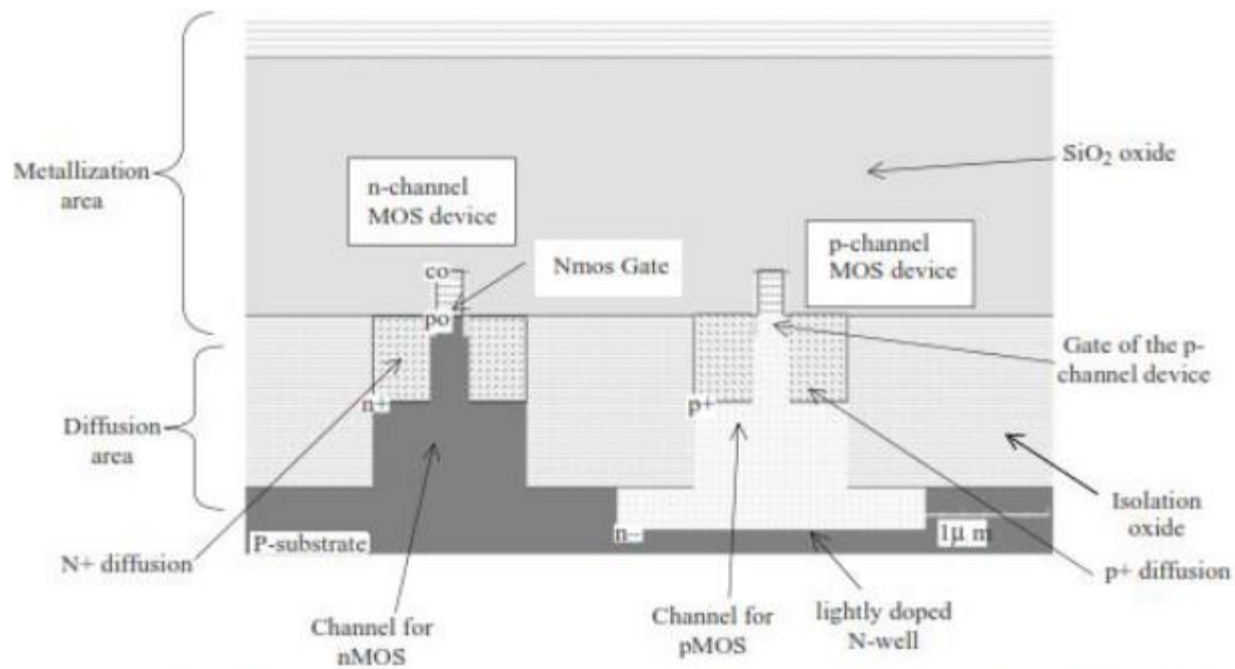
الأبعاد المثالية للترانزستور pmos



الأبعاد المثالية

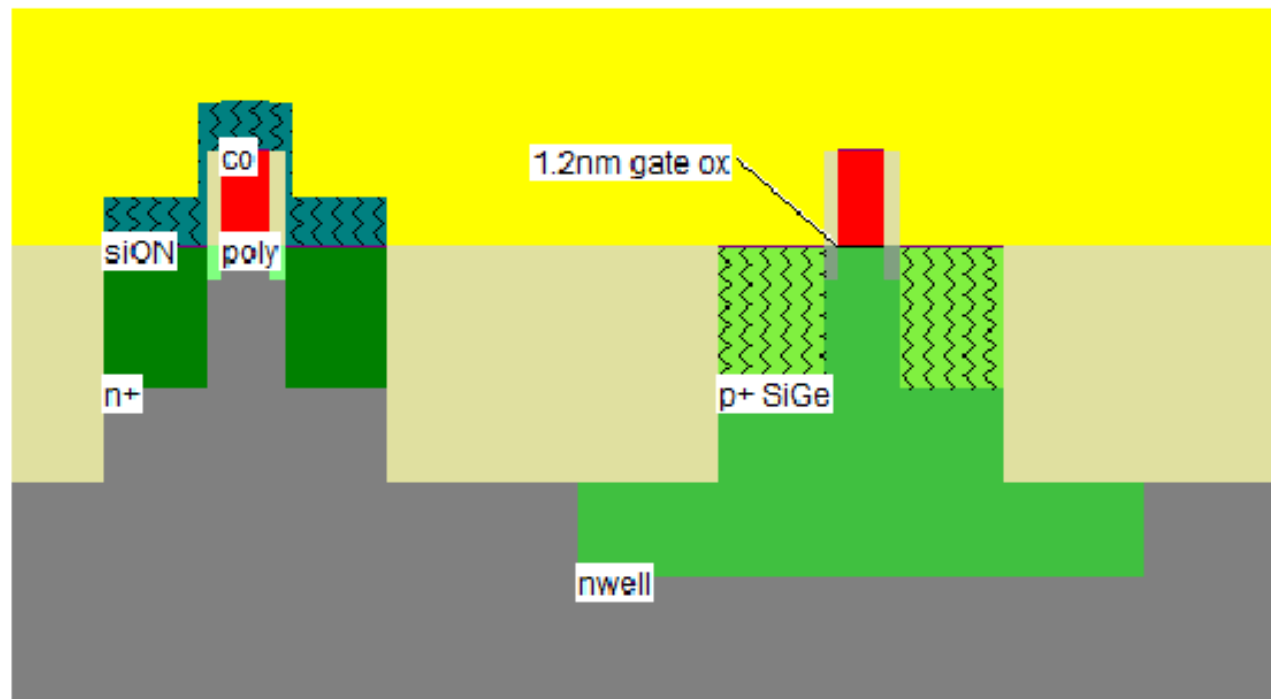


مقطع ثنائي البعد للترانزستورين

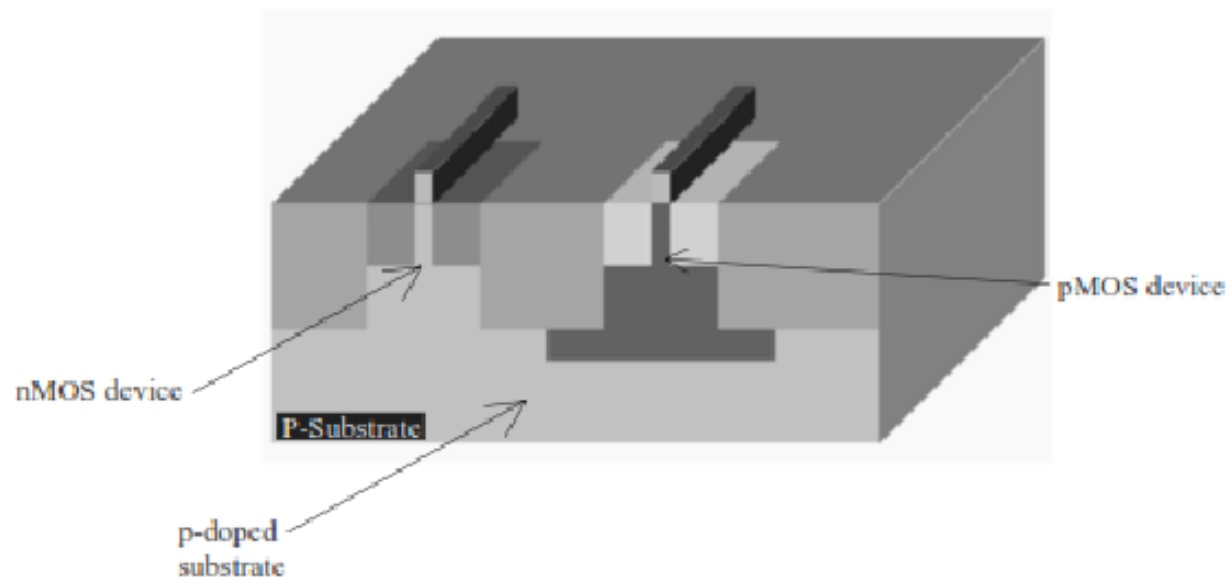


Vertical cross-section of an n-channel and p-channel MOS devices in 0.12 μm technology (allMosDevices.MSK)

مقطع ثنائي البعد للترانزستورين

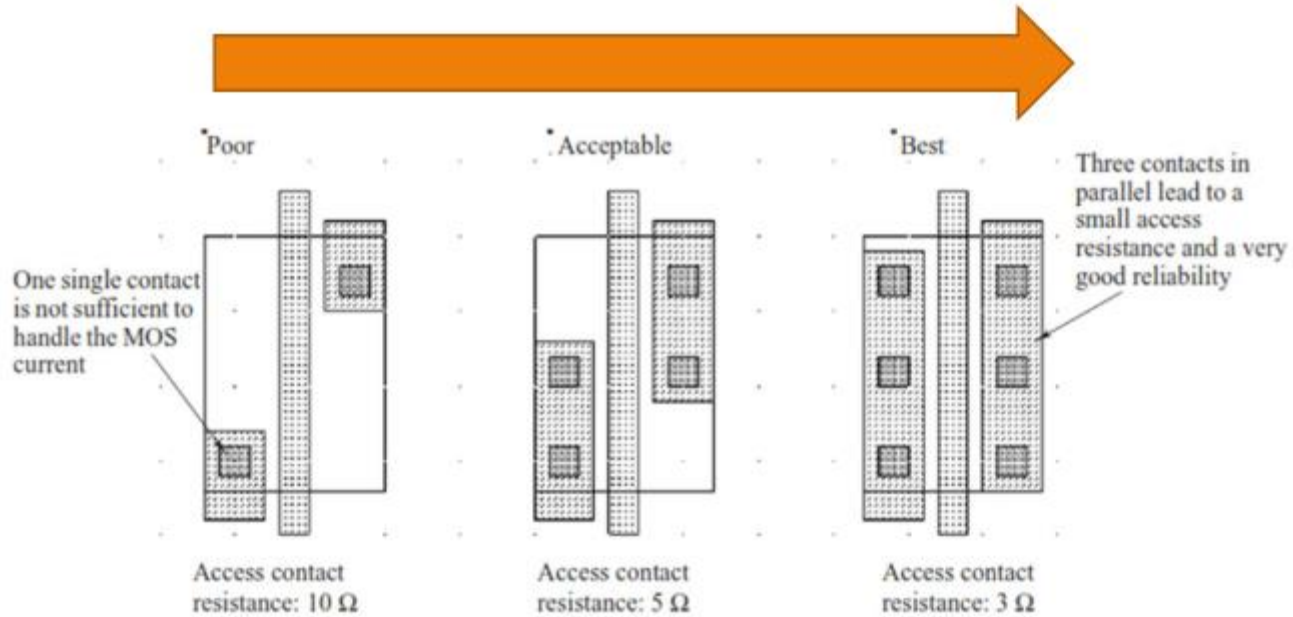


مقطع ثلاثي البعد للترانزستورين



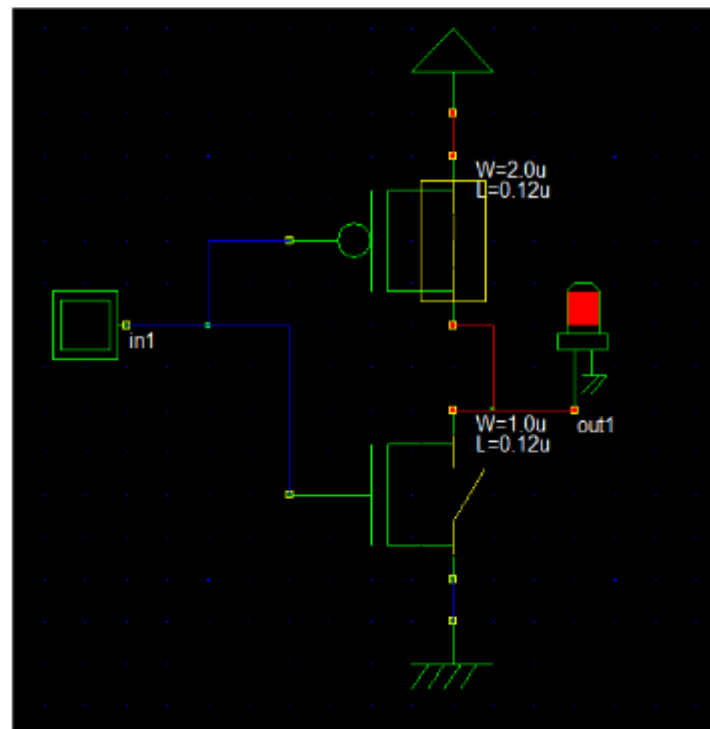
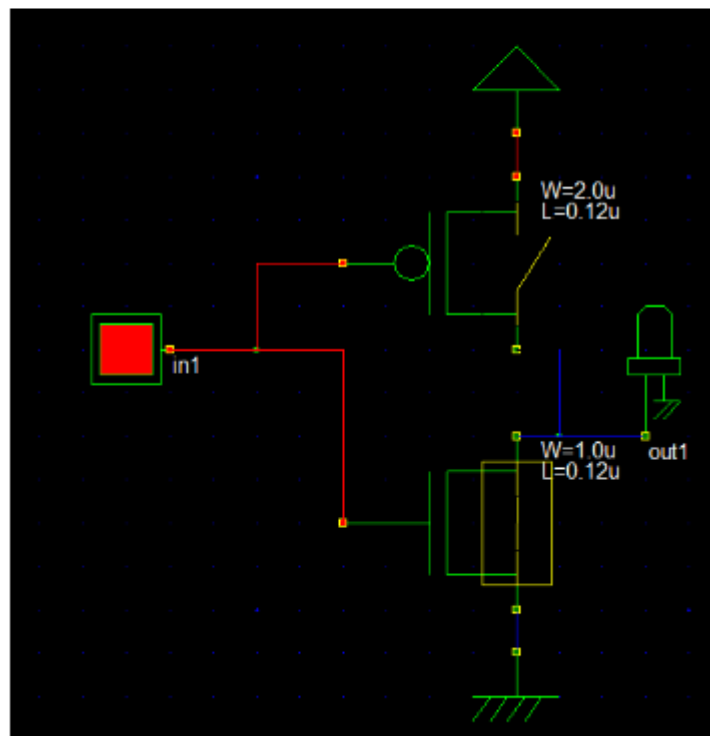
3D view of the n-channel and p-channel MOS devices (AllMosDevices.MSK)

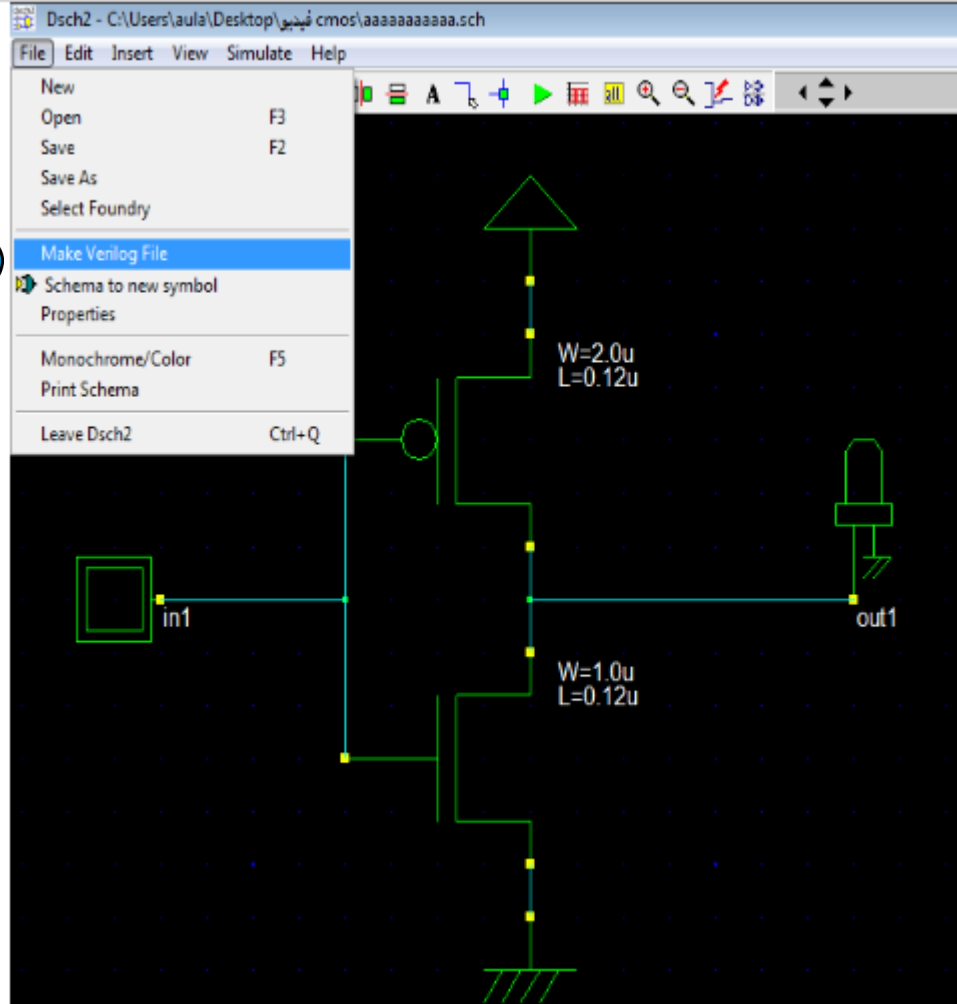
ملاحظة مهمة:



A series of contacts also reduced the serial access resistance (MosContacts.MSK)

أداة Dsch2 ضمن سلسلة برنامج micro wind





الأسئلة والمناقشة

