PLAZA, ELMO L.

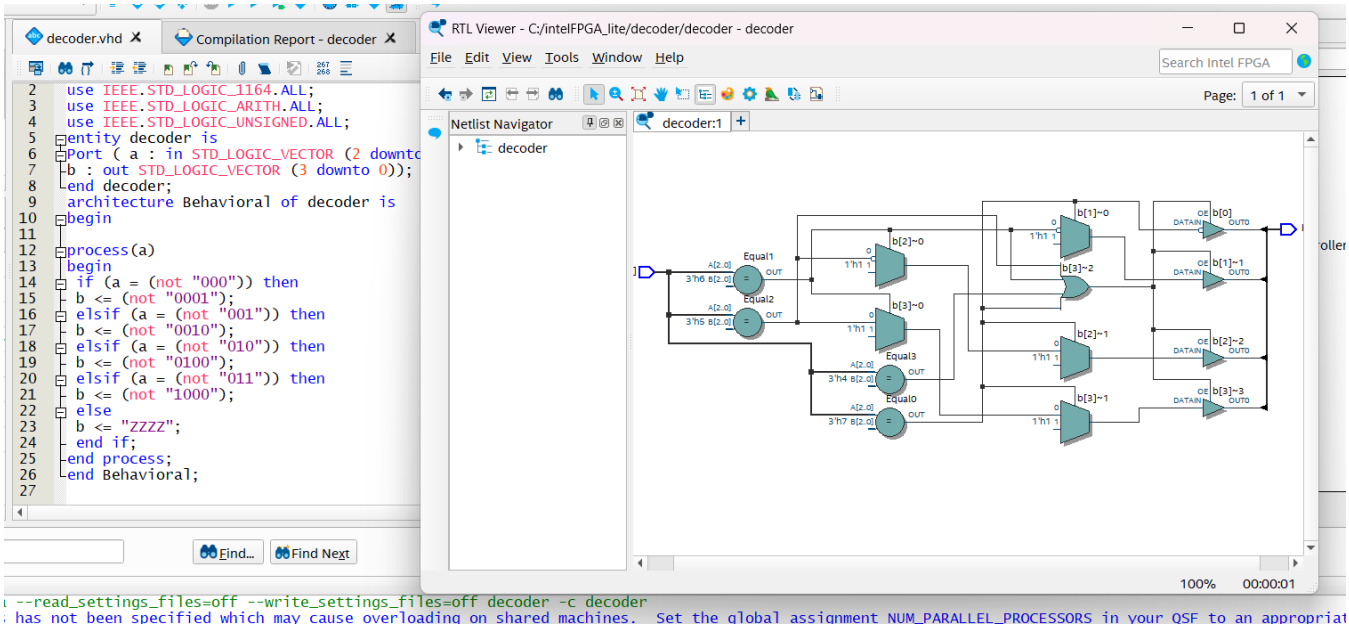
7. VHDL CODE FOR 3:8 DECODER:

CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Decoder is
Port ( a : in STD_LOGIC_VECTOR (2 downto 0);
b : out STD_LOGIC_VECTOR (3 downto 0));
end Decoder;
architecture Behavioral of Decoder is
begin

process(a)
begin
 if (a = (not "000")) then
 b <= (not "0001");
 elsif (a = (not "001")) then
 b <= (not "0010");
 elsif (a = (not "010")) then
 b <= (not "0100");
 elsif (a = (not "011")) then
 b <= (not "1000");
 else
 b <= "ZZZZ";
 end if;
end process;
end Behavioral;
```

OUTPUT:


decoder.vhd
Compilation Report - decoder
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity decoder is
Port (a : in STD_LOGIC_VECTOR (2 downto
b : out STD_LOGIC_VECTOR (3 downto 0));
end decoder;
architecture Behavioral of decoder is
begin
process(a)
begin
if (a = (not "000")) then
b <= (not "0001");
elsif (a = (not "001")) then
b <= (not "0010");
elsif (a = (not "010")) then
b <= (not "0100");
elsif (a = (not "011")) then
b <= (not "1000");
else
b <= "ZZZZ";
end if;
end process;
end Behavioral;
Find...
Find Next
RTL Viewer - C:/intelFPGA_lite/decoder/decoder - decoder
File Edit View Tools Window Help
Search Intel FPGA
Page: 1 of 1
Netlist Navigator
decoder
decoder:1
Equal1
Equal2
Equal3
Equal0
b[2]~0
b[3]~0
b[1]~0
b[3]~2
b[2]~1
b[3]~1
b[0]
b[1]~1
b[2]~2
b[3]~3
100%
00:00:01
--read_settings_files=off --write_settings_files=off decoder -c decoder
has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriat