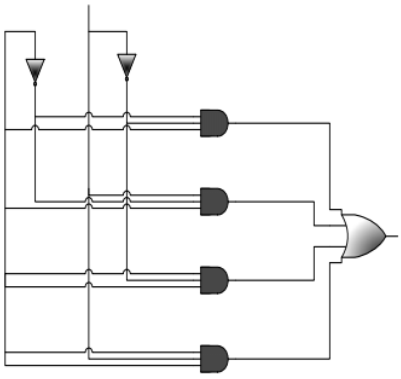
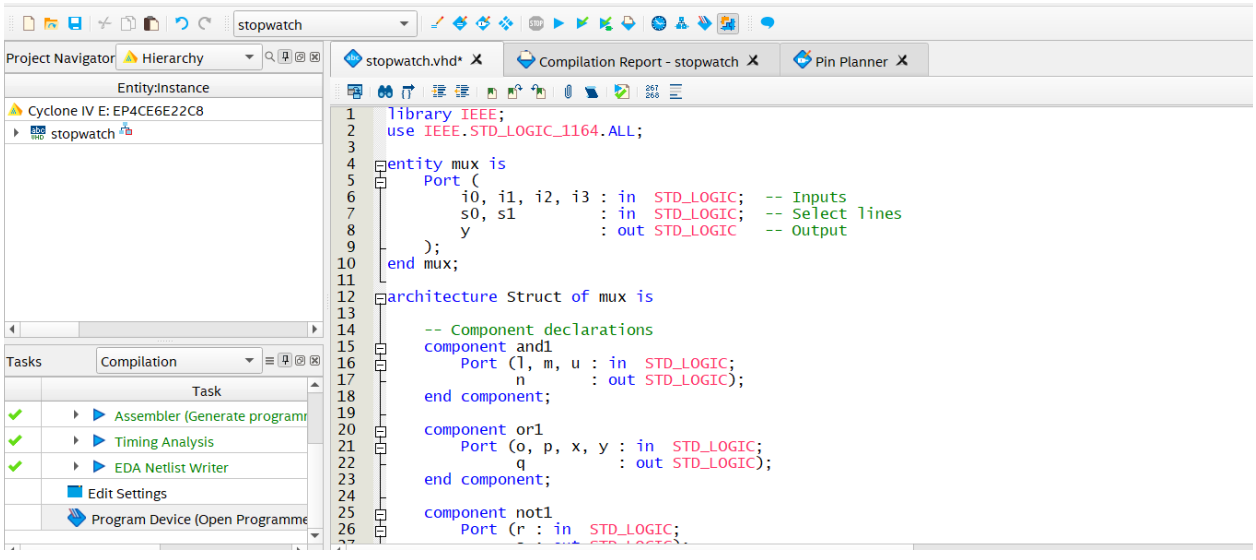
PLAZA, ELMO L. BSCpE 3-A

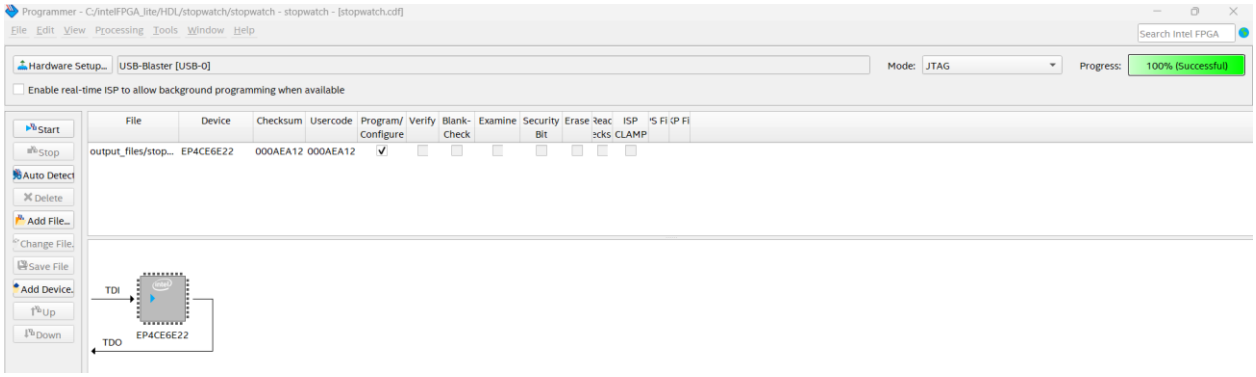
22. VHDL CODE FOR MULTIPLEXER (4:1)(STRUCTURAL):

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux is
   Port (
      i0, i1, i2, i3 : in  STD_LOGIC;  -- Inputs
      s0, s1         : in  STD_LOGIC;  -- Select lines
      y              : out STD_LOGIC   -- Output
   );
end mux;

architecture Struct of mux is

   -- Component declarations
   component and1
      Port (l, m, u : in  STD_LOGIC;
            n       : out STD_LOGIC);
   end component;

   component or1
      Port (o, p, x, y : in  STD_LOGIC;
            q          : out STD_LOGIC);
   end component;

   component not1
      Port (r : in  STD_LOGIC;
            s : out STD_LOGIC);
```



```
    end component;

    -- Internal signals
    signal s2, s3, s4, s5, s6, s7 : STD_LOGIC;

begin
    -- Instantiate NOT gates
    u5: not1 port map(s0, s2);
    u6: not1 port map(s1, s3);

    -- Instantiate AND gates
    u1: and1 port map(i0, s2, s3, s4);
    u2: and1 port map(i1, s2, s1, s5);
    u3: and1 port map(i2, s0, s3, s6);
    u4: and1 port map(i3, s0, s1, s7);

    -- Instantiate OR gate
    u7: or1 port map(s4, s5, s6, s7, y);

end Struct;
```

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Search Intel FPGA
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USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
output_files/stop...
EP4CE6E22
000AEA12
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