```
PLAZA, ELMO L.
                                                             BSCpE 3-A
22. VHDL CODE FOR BINARY-GRAY (STRUCTURAL):
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
                                                                                  7486
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
                                                                                  7486
entity gb is
  Port (g:in STD_LOGIC_VECTOR (3 downto 0);
                                                                                  7486
     b : out STD_LOGIC_VECTOR (3 downto 0));
end gb;
architecture struct of gb is
  component xor1
    port(a, b : in std_logic;
      c : out std_logic);
  end component;
  component and1
    port(d, e : in std_logic;
      f : out std_logic);
  end component;
  component xor12
    port(g, h, i : in std_logic;
       k : out std_logic);
  end component;
  component xor13
```

```
port(l, m, n, o: in std_logic;
             p : out std_logic);
    end component;
begin
    u1: and1 port map(g(3), g(3), b(3));
    u2: xor1 port map(g(3), g(2), b(2));
    u3 : xor12 port map(g(3), g(2), g(1), b(1));
    u4 : xor13 port map(g(3), g(2), g(1), g(0), b(0));
end struct;
       Quartus Prime Lite Edition - C:/intelFPGA_lite/HDL/stopwatch/stopwatch - stopwatch
       <u>File Edit View Project Assignments Processing Tools Window Help</u>
         ☐ 🔚 🛩 🖺 🖒 🖺 🤊 C stopwatch
                                                                    ▼ | ∠ ♦ ♦ ♦ № № № № № ♣ № 🚂 | 🤜
       Project Navigator 🔥 Hierarchy 🔻 🔍 🖳 😸 🔝 stopwatch.vhd* 🗶 💝 Compilation Report - stopwatch 🗶 🗳 Pin Planner 🗶
                                                            曜 | 66 (7 ) | 課 課 | 四 🗗 10 🖜 | 0 🖜 | 20 | 20 | 三
                     Entity:Instance
       △ Cyclone IV E: EP4CE6E22C8
                                                                 library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
        stopwatch 4
                                                               pentity gb is
Port (g: in STD_LOGIC_VECTOR (3 downto 0);
b: out STD_LOGIC_VECTOR (3 downto 0));
                                                               parchitecture struct of gb is
component xor1
port(a, b : in std_logic;
c : out std_logic);
end component;

component and1
port(d, e : in std_logic);
end component;
component xor12
port(g, h, i : in std_logic)
k : out std_logic);
end component;
                                                         10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
                                            ▼ □ □ □ ⋈
       Tasks
                     Compilation
                               Task
                    Assembler (Generate programm
                 ► ► Timing Analysis
                                                                       component xor12
  port(g, h, i : in std_logic;
     k : out std_logic);
end component;
                Edit Settings
                Program Device (Open Programme
           ≡ Type ID Message
      File <u>E</u>dit <u>V</u>iew P<u>r</u>ocessing <u>T</u>ools <u>W</u>indow <u>H</u>elp
                                                                                                                                                                                            Search Intel FPGA
      AHardware Setup... USB-Blaster [USB-0]
       Enable real-time ISP to allow background programming when available
                 File Device Checksum Usercode Program/ Verify Blank- Examine Security Erase Reac ISP Configure Check Bit Seks CLAMP
        ™ Stop
     BAuto Detect
     Add File...
      Change File
     Save File
     Add Device.
        t<sup>№</sup>Up
```

TDO EP4CE6E22