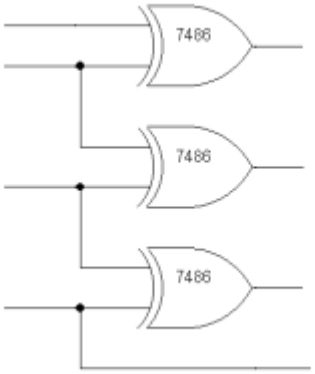
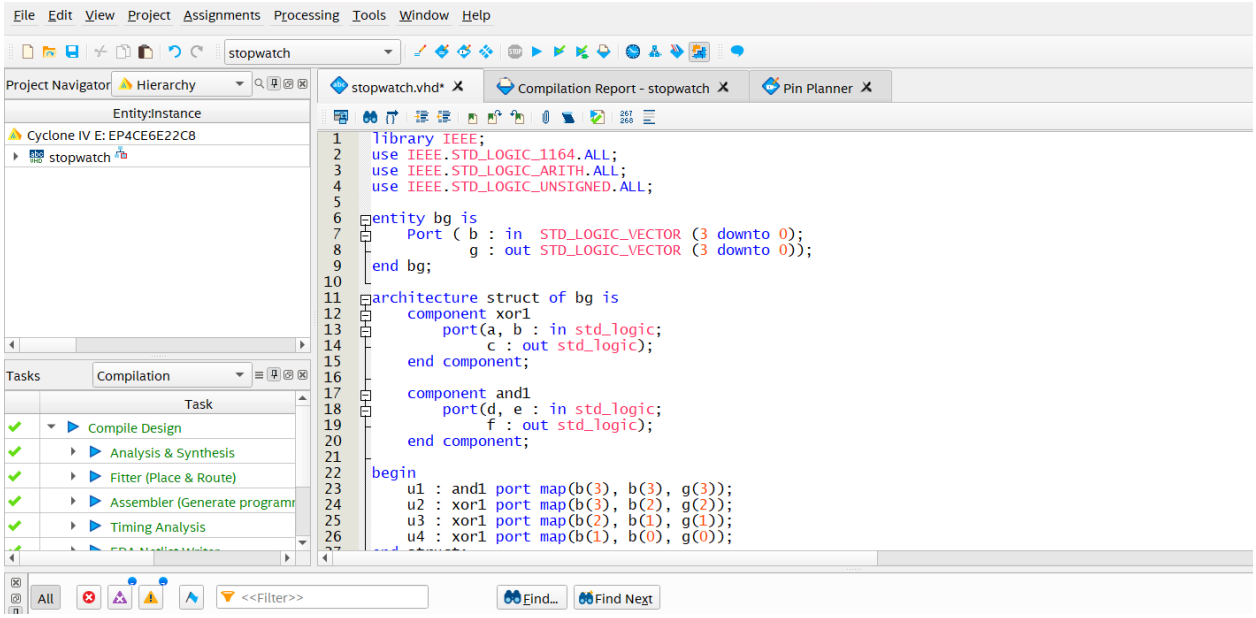
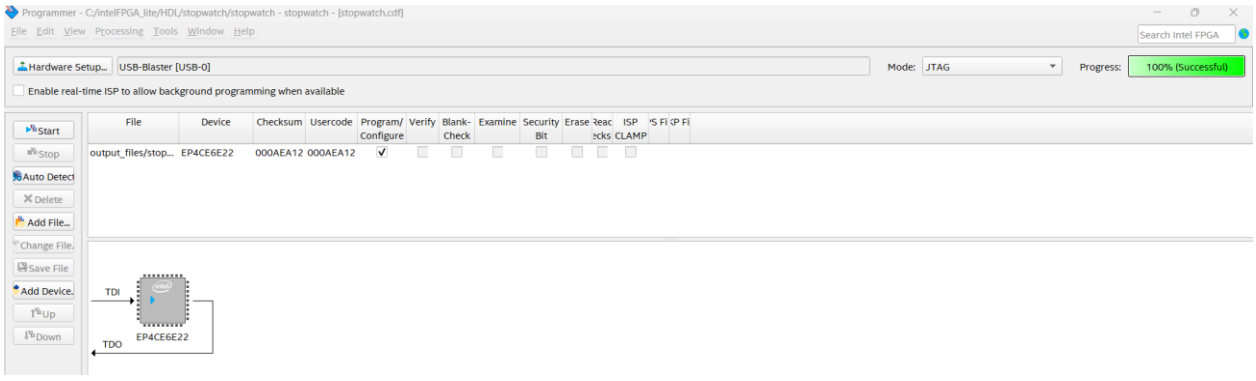
PLAZA, ELMO L. BSCpE 3-A

22. VHDL CODE FOR BINARY-GRAY (STRUCTURAL):

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


entity bg is
   Port ( b : in  STD_LOGIC_VECTOR (3 downto 0);
          g : out STD_LOGIC_VECTOR (3 downto 0));
end bg;

architecture struct of bg is
   component xor1
      port(a, b : in std_logic;
           c : out std_logic);
   end component;

   component and1
      port(d, e : in std_logic;
           f : out std_logic);
   end component;

begin
   u1 : and1 port map(b(3), b(3), g(3));
   u2 : xor1 port map(b(3), b(2), g(2));
   u3 : xor1 port map(b(2), b(1), g(1));
   u4 : xor1 port map(b(1), b(0), g(0));
end struct;
```




File Edit View Project Assignments Processing Tools Window Help
stopwatch
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22C8
stopwatch
stopwatch.vhd*
Compilation Report - stopwatch
Pin Planner
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_ARITH.ALL;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6 entity bg is
7 Port (b : in STD_LOGIC_VECTOR (3 downto 0);
8 g : out STD_LOGIC_VECTOR (3 downto 0));
9 end bg;
10
11 architecture struct of bg is
12 component xor1
13 port(a, b : in std_logic;
14 c : out std_logic);
15 end component;
16
17 component and1
18 port(d, e : in std_logic;
19 f : out std_logic);
20 end component;
21
22 begin
23 u1 : and1 port map(b(3), b(3), g(3));
24 u2 : xor1 port map(b(3), b(2), g(2));
25 u3 : xor1 port map(b(2), b(1), g(1));
26 u4 : xor1 port map(b(1), b(0), g(0));
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programr
Timing Analysis
All
<<Filter>>
Find...
Find Next


Programmer - C:/intelFPGA_lite/HDL/stopwatch/stopwatch - stopwatch - [stopwatch.cdf]
File Edit View Processing Tools Window Help
Search Intel FPGA
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
output_files/stop...
EP4CE6E22
000AEA12
000AEA12
TDI
TDO
EP4CE6E22