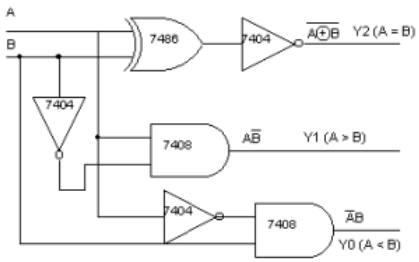
PLAZA, ELMO L. BSCpE 3-A

22. VHDL CODE FOR 1-BIT COMPARATOR (STRUCTURAL):

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL; use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```



A	B	Y1 (A>B)	Y2 (A = B)	Y3 (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

```
entity comp is
   Port (
      a, b : in  STD_LOGIC;
      y    : out STD_LOGIC_VECTOR (2 downto 0)
   );
end comp;

architecture struct of comp is

   -- Component Declarations
   component and1
      port(l, m : in  std_logic; n : out std_logic);
   end component;

   component xnor1
      port(p, q : in  std_logic; r : out std_logic);
   end component;

   component notgate1
      port(s : in std_logic; t : out std_logic);
   end component;

   -- Internal Signals
```

```
    signal s1, s2 : std_logic;

begin

    -- Logic for comparator output
    u1 : and1    port map(a, s2, y(0));   -- a > b
    u2 : and1    port map(s1, b, y(1));   -- a < b
    u3 : xnor1   port map(a, b, y(2));    -- a = b
    u4 : notgate1 port map(a, s1);
    u5 : notgate1 port map(b, s2);

end struct;
```