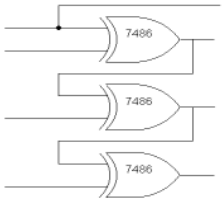
PLAZA, ELMO L. BSCpE 3-A

VHDL CODE FOR GRAY TO BINARY:




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity gb1 is
    Port (
        g : in  STD_LOGIC_VECTOR(3 downto 0);  -- Gray Code Input
        b : out STD_LOGIC_VECTOR(3 downto 0)   -- Binary Output
    );  end gb1;


architecture Behavioral of gb1 is
begin
    b(3) <= g(3);
    b(2) <= g(3) xor g(2);
    b(1) <= g(3) xor g(2) xor g(1);
    b(0) <= g(3) xor g(2) xor g(1) xor g(0);
end Behavioral;
```

INPUT				OUTPUT			
G(3)	G(2)	G(1)	G(0)	B (3)	B (2)	B (1)	B (0)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1