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VHDL CODE FOR Binary to gray (USING EXOR GATES):

CODE:

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

entity Binary_Gray is

Port (

b: in STD_LOGIC_VECTOR(3 downto 0); -- Binary Input

g : out STD_LOGIC_VECTOR(3 downto 0) -- Gray Output

);

end Binary_Gray;

architecture Behavioral of Binary_Gray is begin

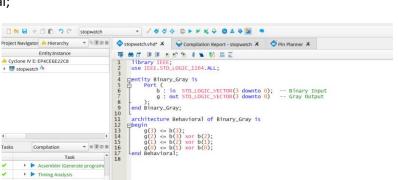
```
g(3) \le b(3);
```

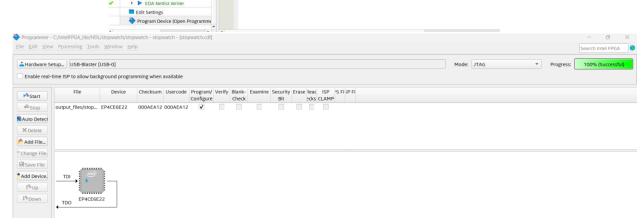
 $g(2) \le b(3) xor b(2);$

 $g(1) \le b(2) xor b(1);$

 $g(0) \le b(1) xor b(0);$

end Behavioral;





BSCpE 3-A

Inputs				Outputs			
B (3)	B (2)	B (1)	B (0)	G (3)	G (2)	G (1)	G (0)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

