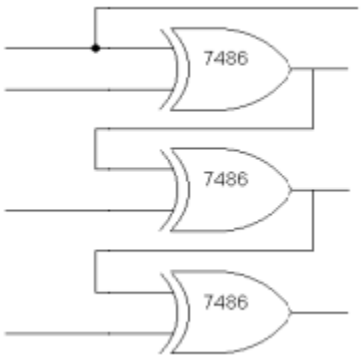
PLAZA, ELMO L. BSCpE 3-A

22. VHDL CODE FOR BINARY-GRAY (STRUCTURAL):




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity gb is
   Port ( g : in  STD_LOGIC_VECTOR (3 downto 0);
          b : out STD_LOGIC_VECTOR (3 downto 0));
end gb;

architecture struct of gb is
   component xor1
      port(a, b : in std_logic;
           c : out std_logic);
   end component;

   component and1
      port(d, e : in std_logic;
           f : out std_logic);
   end component;

   component xor12
      port(g, h, i : in std_logic;
           k : out std_logic);
   end component;

   component xor13
```

```
    port(l, m, n, o : in std_logic;
         p : out std_logic);
  end component;

begin
  u1 : and1 port map(g(3), g(3), b(3));
  u2 : xor1 port map(g(3), g(2), b(2));
  u3 : xor12 port map(g(3), g(2), g(1), b(1));
  u4 : xor13 port map(g(3), g(2), g(1), g(0), b(0));
end struct;
```