

PLAZA, ELMO L.
BSCPE 3A

20. VHDL CODE FOR SEVEN SEGMENT DISPLAY INTERFACE

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity SEVEN_SEGMENT_DISPLAY_INTERFACE is
Port (
    clk    : in  STD_LOGIC; -- 4MHz clock (PIN_23)
    rst    : in  STD_LOGIC; -- Active-high reset (PIN_25)
    seg    : out STD_LOGIC_VECTOR(6 downto 0); -- Active-low segments a-g
    dig    : out STD_LOGIC_VECTOR(3 downto 0) -- Active-low digit enables
);
end SEVEN_SEGMENT_DISPLAY_INTERFACE;

architecture Behavioral of SEVEN_SEGMENT_DISPLAY_INTERFACE is
    -- Clock divider signals
    signal counter    : unsigned(23 downto 0) := (others => '0');
    signal clk_1hz    : STD_LOGIC := '0';

    -- Hex counter
    signal hex_value  : unsigned(3 downto 0) := "0000";

    -- Display signals
    signal dig_sel    : unsigned(1 downto 0) := "00";
begin

    process(clk, rst)
    begin
        if rst = '1' then
            counter <= (others => '0');
            hex_value <= "0000";
        elsif rising_edge(clk) then
            if counter = x"F42400" then -- 0.25Hz (4 seconds per count)
                counter <= (others => '0');
                hex_value <= hex_value + 1;
            end if;
        end if;
    end process;
end Behavioral;
```

```

    else
        counter <= counter + 1;
    end if;
end if;
end process;

```

```

-- Digit scanner (244Hz refresh)
dig_sel <= counter(15 downto 14); -- 4MHz/2^16 = ~244Hz

```

```

-- Single-digit display (all digits show same value)
dig <= "1110" when dig_sel = "00" else -- DIG1
      "1101" when dig_sel = "01" else -- DIG2
      "1011" when dig_sel = "10" else -- DIG3
      "0111"; -- DIG4

```

```

-- Active-low hex decoder (common cathode)
with hex_value select

```

```

    seg <= "0000001" when x"0", -- 0
          "1001111" when x"1", -- 1
          "0010010" when x"2", -- 2
          "0000110" when x"3", -- 3
          "1001100" when x"4", -- 4
          "0100100" when x"5", -- 5
          "0100000" when x"6", -- 6
          "0001111" when x"7", -- 7
          "0000000" when x"8", -- 8
          "0000100" when x"9", -- 9
          "0001000" when x"A", -- A
          "1100000" when x"B", -- B
          "0110001" when x"C", -- C
          "1000010" when x"D", -- D
          "0110000" when x"E", -- E
          "0111000" when others; -- F

```

```

end Behavioral;

```

Quartus Prime Lite Edition - D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SEVEN_SEGMENT_DISPLAY_INTERFACE/SEVEN_SEGMENT_DISPLAY_INTERFACE - SEVEN_SEGMENT_DISPLAY_INTERFACE

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity/Instance

Logic

SEVEN_SEGMENT_DISPLAY_INTERFACE

Compilation Report - SEVEN_SEGMENT_DISPLAY_INTERFACE

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Processors and Peripherals

University Program

Search for Partner IP

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5 entity SEVEN_SEGMENT_DISPLAY_INTERFACE is
6 port (
7     clk : in STD_LOGIC; -- 4MHz clock (PIN_23)
8     rst : in STD_LOGIC; -- Active-high reset (PIN_25)
9     seg : out STD_LOGIC_VECTOR(6 downto 0); -- Active-low segments a-g
10    dig : out STD_LOGIC_VECTOR(3 downto 0) -- Active-low digit enables
11 );
12 end SEVEN_SEGMENT_DISPLAY_INTERFACE;
13
14 architecture Behavioral of SEVEN_SEGMENT_DISPLAY_INTERFACE is
15     -- Clock divider signals
16     signal counter : unsigned(23 downto 0) := (others => '0');
17     signal clk_1hz : STD_LOGIC := '0';
18
19     -- Hex counter
20     signal hex_value : unsigned(3 downto 0) := "0000";
21
22     -- Display signals
23     signal dig_sel : unsigned(1 downto 0) := "00";
24
25 begin
26
27     process(clk, rst)
28     begin
29         rst = '1' then
30             counter <= (others => '0');
31             hex_value <= "0000";
32         else
33             -- Clock divider logic
34             counter <= counter + 1;
35             -- 1Hz clock divider
36             if counter = 24 then
37                 clk_1hz <= not clk_1hz;
38                 counter <= (others => '0');
39             end if;
40
41             -- Hex counter logic
42             if counter(23) = 1 then
43                 hex_value <= hex_value + 1;
44                 if hex_value = 16 then
45                     hex_value <= (others => '0');
46                 end if;
47             end if;
48
49             -- Digit select logic
50             dig_sel <= dig_sel + 1;
51             if dig_sel = 4 then
52                 dig_sel <= (others => '0');
53             end if;
54         end if;
55     end process;
56
57     -- Output logic
58     dig(0) <= not (dig_sel = 0);
59     dig(1) <= not (dig_sel = 1);
60     dig(2) <= not (dig_sel = 2);
61     dig(3) <= not (dig_sel = 3);
62
63     seg(0) <= hex_value(0);
64     seg(1) <= hex_value(1);
65     seg(2) <= hex_value(2);
66     seg(3) <= hex_value(3);
67     seg(4) <= hex_value(4);
68     seg(5) <= hex_value(5);
69     seg(6) <= hex_value(6);
70 end Behavioral;
```

Tasks

Compilation

Task

Compile Design

Analysis & Synthesis

Fitter (Place & Route)

Assembler (Generate programming files)

Timing Analysis

EDA Netlist Writer

Edit Settings

Program Device (Open Programmer)

Messages

Type ID Message

Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings

Running Quartus Prime EDA Netlist Writer

Command: quartus_edu --read_settings_files=off --write_settings_files=off SEVEN_SEGMENT_DISPLAY_INTERFACE

18236 Number of processors has not been specified which may cause overloading on shared machine

204019 Generated File SEVEN_SEGMENT_DISPLAY_INTERFACE.vho in folder "D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SEVEN_SEGMENT_DISPLAY_INTERFACE"

Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning

293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings

System (40) Processing (112)

Programmer - D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SEVEN_SEGMENT_DISPLAY_INTERFACE/SEVEN_SEGMENT_DISPLAY_INTERFACE.vho

File Edit View Processing Tools Window Help

Hardware Setup

USB-Blaster (USB-0)

Mode: JTAG

Progress: 100% (Successful)

Enable real-time ISP to allow background programming when available

Start

Stop

Auto Detect

Delete

Add File...

Change File

Save File

Add Device

Up

Down

File	Device	Checksum	Usercode	Program/Verify	Blank/Check	Examine	Security	Erase
output_files/SEVEN_SEGMENT_DISPLAY_INTERFACE.vho	EP4CE6E22	0009AAC5	0009AAC5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

TDO

TDO

EP4CE6E22

