## 6. VHDL CODE FOR ENCODER WITH PRIORITY (4:2):

```
CODE:
library IEEE;
use IEEE.STD LOGIC 1164.all;
entity w1 is
   port(
        a : in STD LOGIC VECTOR(3 downto 0);
        b : out STD LOGIC VECTOR(1 downto 0)
    );
end w1;
architecture bhv of w1 is
begin
process(a)
begin
    if (a = (not "0111")) then
       b <= (not "00") ;
    elsif (a = ("0110")) then
       b <= "01";
    elsif (a = (not "0101")) then
        b <= "10";
    elsif (a = (not "0100")) then
       b <= (not "11");
    else
        b <= "ZZ"; -- If no inputs are active
    end if;
end process;
end bhv;
```

## **OUTPUT:**

