PLAZA, ELMO L.

2.VHDL CODE FOR FULL ADDER STRUCTURAL:

CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity fa1 is
    Port ( a, b, cin : in  STD_LOGIC;
           s, cout : out  STD_LOGIC);
end fa1;

architecture struct of fa1 is
    component and21
        port(a, b: in std_logic;
             c: out std_logic);
    end component;

    component xor21
        port(a, b: in std_logic;
             c: out std_logic);
    end component;

    component or31
        port(a, b: in std_logic;
             d: out std_logic);
    end component;

    signal s1, s2, s3: std_logic;
```

```
begin
    u1: xor21 port map(a, b, s1);
    u2: xor21 port map(s1, cin, s);
    u3: and21 port map(a, b, s2);
    u4: and21 port map(s1, cin, s3);
    u6: or31 port map(s2, s3, cout);
end struct;
```

OUTPUT: