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1. VHDL CODE FOR FULL ADDER DATA FLOW

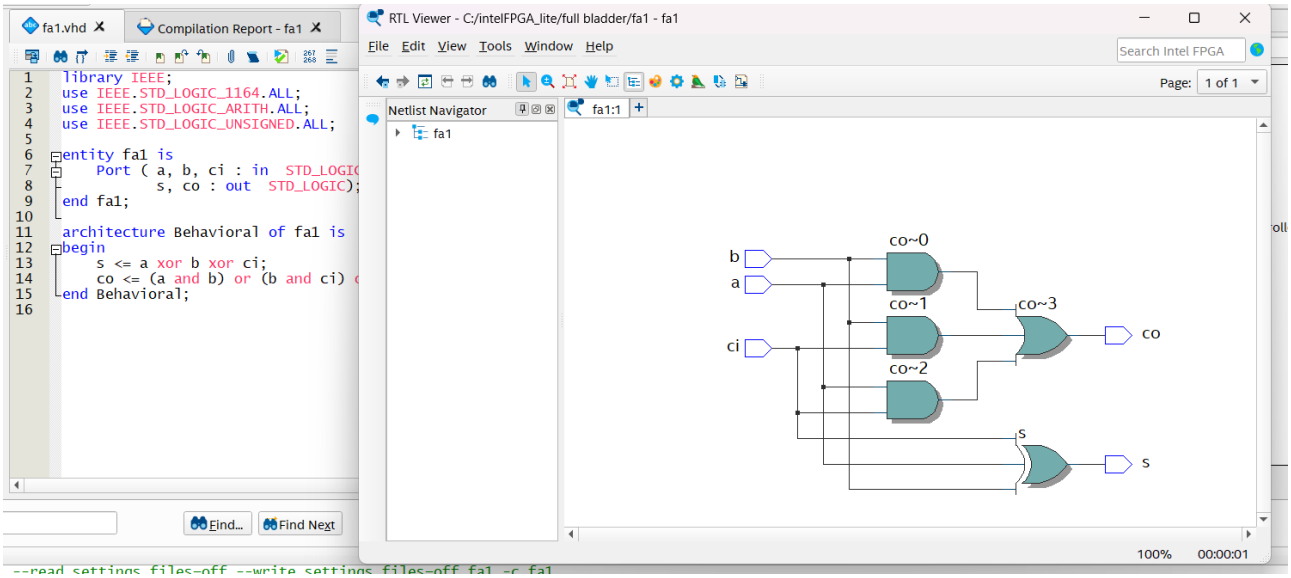
CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


entity fa1 is
    Port ( a, b, ci : in  STD_LOGIC;
           s, co : out  STD_LOGIC);
end fa1;


architecture Behavioral of fa1 is
begin
    s <= a xor b xor ci;
    co <= (a and b) or (b and ci) or (ci and a);
end Behavioral;
```

OUTPUT:



VHDL CODE FOR FULL ADDER BEHAVIORAL:

CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity fa1 is
    Port ( a, b, ci : in  STD_LOGIC;
           s, co : out  STD_LOGIC);
end fa1;

architecture Behavioral of fa1 is
begin
    process(a, b, ci)
    begin
        s <= a xor b xor ci;
        co <= (a and b) or (b and ci) or (ci and a);
    end process;
end Behavioral;
```

OUTPUT: