PLAZA, ELMO L.
BSCPE 3A

VHDL CODE FOR D FLIP FLOP:

Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	0	0	0	1
0	1	⎍	1	0

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity D_flipflop is
   Port (
      d    : in  STD_LOGIC;
      clk  : in  STD_LOGIC;
      res_n : in  STD_LOGIC; -- active-low reset
      q    : out STD_LOGIC
   );
end D_flipflop     ;

architecture Behavioral of D_flipflop            is
begin
   process(clk)
   begin
      if rising_edge(clk) then
         if res_n = '' then
            q <= 'a';
         else
            q <= d
                                                  s;
         end if;
      end if;
   end process;
end Behavioral;
```