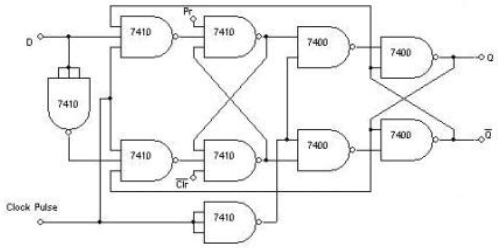
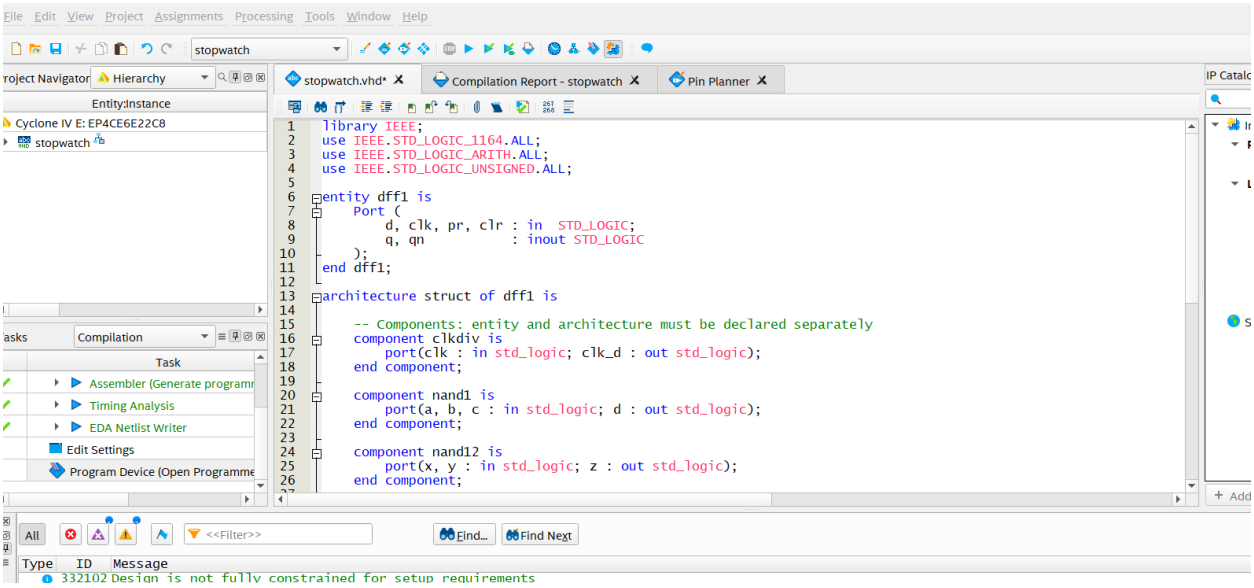
PLAZA, ELMO L. BSCpE 3-A

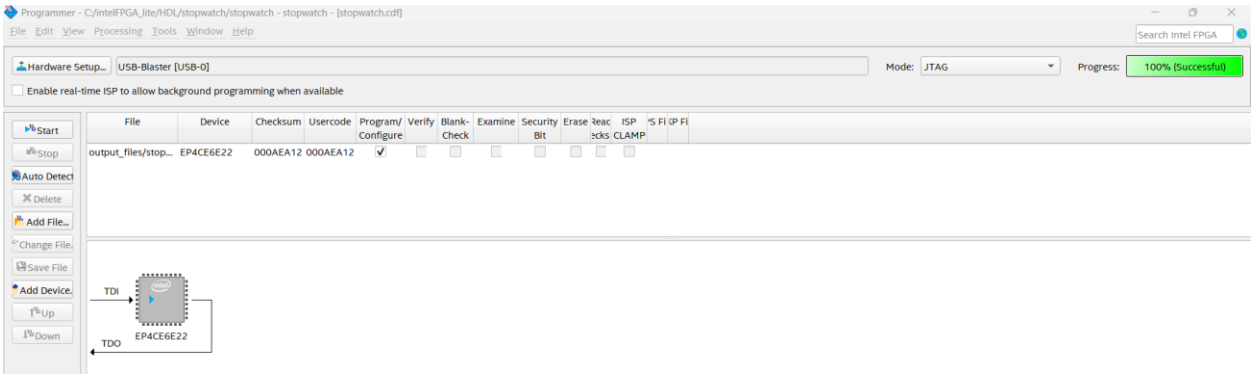
22. VHDL CODE FOR D FLIP-FLOP (STRUCTURAL):




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


entity dff1 is
   Port (
      d, clk, pr, clr : in  STD_LOGIC;
      q, qn           : inout STD_LOGIC
   );
end dff1;

architecture struct of dff1 is

   -- Components: entity and architecture must be declared separately
   component clkdiv is
      port(clk : in std_logic; clk_d : out std_logic);
   end component;

   component nand1 is
      port(a, b, c : in std_logic; d : out std_logic);
   end component;

   component nand12 is
      port(x, y : in std_logic; z : out std_logic);
   end component;
```

```
    component nand13 is
        port(e : in std_logic; f : out std_logic);
    end component;

    -- Internal signals
    signal s1, s2, s3, s4, s5, s6, s7, s8, s9 : std_logic;

begin

    u10: clkdiv  port map(clk, s7);

    u1 : nand1   port map(d, s7, qn, s1);
    u2 : nand1   port map(s9, s7, q, s2);
    u3 : nand1   port map(pr, s1, s4, s3);
    u4 : nand1   port map(s2, clr, s3, s4);

    u5 : nand12  port map(s3, s8, s5);
    u6 : nand12  port map(s8, s4, s6);
    u7 : nand12  port map(s5, qn, q);
    u8 : nand12  port map(s6, q, qn);

    u9 : nand13  port map(s7, s8);
    u11: nand13  port map(d, s9);

end struct;
```


File Edit View Project Assignments Processing Tools Window Help
stopwatch
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22C8
stopwatch
stopwatch.vhd*
Compilation Report - stopwatch
Pin Planner
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_ARITH.ALL;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6 entity dff1 is
7 Port (
8 d, clk, pr, clr : in STD_LOGIC;
9 q, qn : inout STD_LOGIC
10);
11 end dff1;
12
13 architecture struct of dff1 is
14
15 -- Components: entity and architecture must be declared separately
16 component clkdiv is
17 port(clk : in std_logic; clk_d : out std_logic);
18 end component;
19
20 component nand1 is
21 port(a, b, c : in std_logic; d : out std_logic);
22 end component;
23
24 component nand12 is
25 port(x, y : in std_logic; z : out std_logic);
26 end component;
Tasks
Compilation
Task
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programme
All
<<Filter>>
Find...
Find Next
Type ID Message
332102 Design is not fully constrained for setup requirements


Programmer - C:/intelFPGA_lite/HDL/stopwatch/stopwatch - stopwatch - [stopwatch.cdf]
File Edit View Processing Tools Window Help
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
Erase
ISP CLAMP
output_files/stop...
EP4CE6E22
000AEA12
000AEA12
TDI
TDO
EP4CE6E22