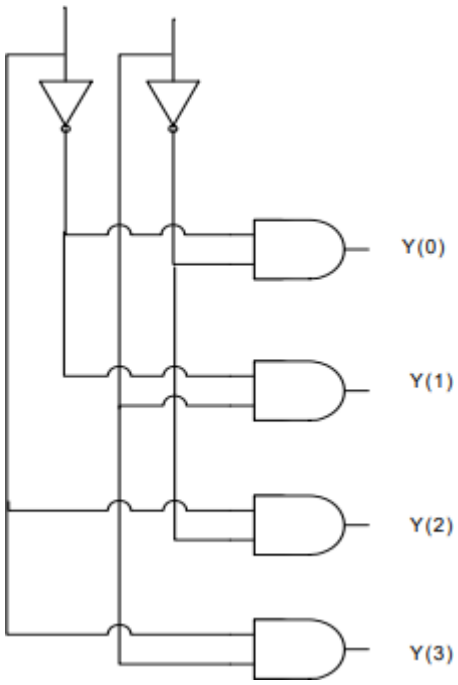
PLAZA, ELMO L. BSCpE 3-A

22. VHDL CODE FOR DECODER 3:8 (STRUCTURAL):




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity dec is
   Port (       a, b : in  STD_LOGIC;
      y    : out STD_LOGIC_VECTOR (3 downto 0)
   );
end dec;

architecture Behavioral of dec is

   -- Components, entity and architecture must be declared separately
   component and1 is
      port(p, q : in std_logic; r : out std_logic);
   end component;

   component not1 is
      port(d : in std_logic; e : out std_logic);
   end component;

   signal s1, s2 : std_logic;

begin
   u1: and1 port map(s1, s2, y(0));
   u2: and1 port map(s1, b,   y(1));
```

```
    u3: and1 port map(a, s2,   y(2));
    u4: and1 port map(a, b,    y(3));

    u5: not1 port map(a, s1);
    u6: not1 port map(b, s2);

end Behavioral;
```