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BSCPE 3A

VHDL CODE FOR JK FLIP FLOP WITH ASYNCHRONOUS RESET: (Master Slave JK Flip-Flop)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity JK_Flipflop is
    Port (
        j   : in  STD_LOGIC;
        k   : in  STD_LOGIC;
        clk  : in  STD_LOGIC;
        reset : in  STD_LOGIC; -- Active-low reset
        Q    : out STD_LOGIC
    );
end JK_Flipflop;

architecture Behavioral of JK_Flipflop is
    signal div  : unsigned(22 downto 0) := (others => '0');
    signal clkd : STD_LOGIC := '0';
    signal q_int : STD_LOGIC := '0';
begin

    -- Clock divider: divide clk down to a slower clkd
    process(clk)
    begin
        if rising_edge(clk) then
            div <= div + 1;
        end if;
    end process;

    clkd <= div(22); -- Slow clock

    -- JK Flip-Flop with active-low reset and slower clock
    process(clkd, reset)
    begin
        if reset = '0' then -- Active-low reset
            q_int <= '0';
        elsif rising_edge(clkd) then
            if (j = '0' and k = '0') then
                -- No change
                null;
            elsif (j = '0' and k = '1') then
                q_int <= '0'; -- Reset
            elsif (j = '1' and k = '0') then
                q_int <= '1'; -- Set
            end if;
        end if;
    end process;

    Q <= q_int;

end Behavioral;
```

```

    elsif (j = '1' and k = '1') then
        q_int <= not q_int; -- Toggle
    end if;
end if;
end process;

```

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Q <= q_int;

```

```

end Behavioral;

```

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows the VHDL code for the JK_Flipflop.vhd file. The code defines a JK Flip-Flop with inputs k, clk, and reset, and output Q. It includes a clock divider and a JK Flip-Flop with active-low reset. The compilation process is shown in the left pane, with tasks like Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate programming), Timing Analysis, EDA Netlist Writer, and Program Device (Open Programmer) all completed successfully.

The right pane shows the Programmer window, which is configured for the USB-Blaster [USB-0] in JTAG mode. The progress bar indicates 100% (Successful). The hardware setup table shows the device EP4CE6E22, checksum 0009558C, and usercode 0009558C. The file output is output_files/JK_F... EP4CE6E22. The hardware setup table also includes columns for Verify, Blank-Check, Examine, Security, and Bit.

The bottom pane shows the Messages window, which displays the compilation results. The messages indicate that the Quartus Prime EDA Netlist Writer was successful, 0 errors, 1 warning. The Quartus Prime Full Compilation was successful, 0 errors, 13 warnings. The Quartus Prime Netlist Viewers Preprocess was successful, 0 errors, 1 warning. The Quartus Prime Netlist Viewers Preprocess was successful, 0 errors, 1 warning.