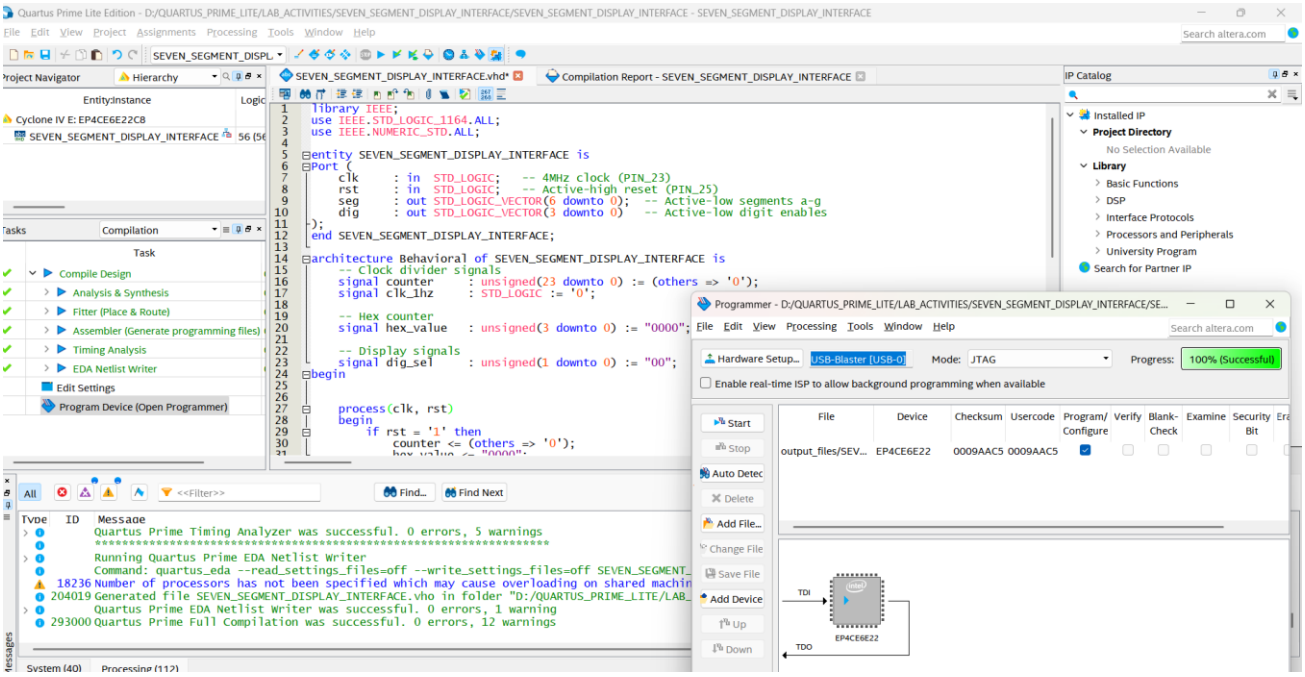
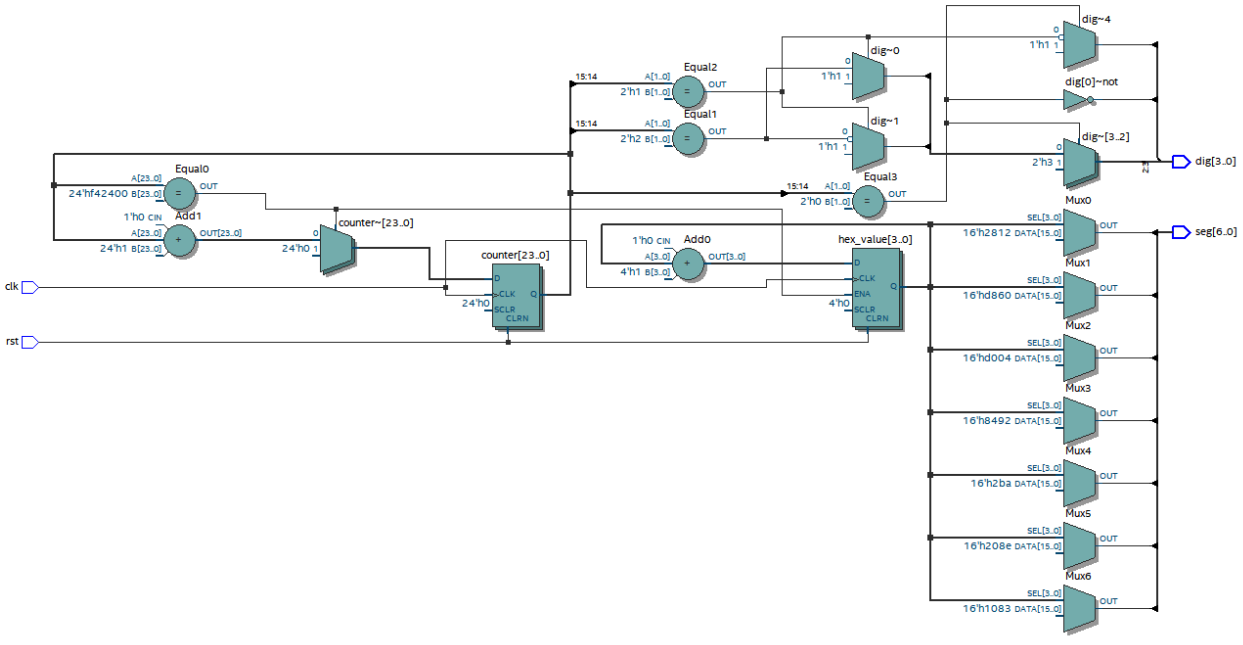
PLAZA, ELMO L.
BSCPE 3A

20. VHDL CODE FOR SEVEN SEGMENT DISPLAY INTERFACE

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity SEVEN_SEGMENT_DISPLAY_INTERFACE        is
Port (
   clk     : in  STD_LOGIC;   -- 4MHz clock (PIN_23)
   rst     : in  STD_LOGIC;   -- Active-high reset (PIN_25)
   seg     : out STD_LOGIC_VECTOR(6 downto 0);  -- Active-low segments a-g
   dig     : out STD_LOGIC_VECTOR(3 downto 0)   -- Active-low digit enables
);
end SEVEN_SEGMENT_DISPLAY_INTERFACE;

architecture Behavioral of SEVEN_SEGMENT_DISPLAY_INTERFACE is
   -- Clock divider signals
   signal counter     : unsigned(23 downto 0) := (others => '0');
   signal clk_1hz     : STD_LOGIC := '0';

   -- Hex counter
   signal hex_value   : unsigned(3 downto 0) := "0000";

   -- Display signals
   signal dig_sel     : unsigned(1 downto 0) := "00";
begin


   process(clk, rst)
   begin
      if rst = '1' then
         counter <= (others => '0');
         hex_value <= "0000";
      elsif rising_edge(clk) then
         if counter = x"F42400" then -- 0.25Hz (4 seconds per count)
            counter <= (others => '0');
            hex_value <= hex_value + 1;
```

```
        else
           counter <= counter + 1;
        end if;
     end if;
  end process;

  -- Digit scanner (244Hz refresh)
  dig_sel <= counter(15 downto 14);  -- 4MHz/2^16 = ~244Hz

  -- Single-digit display (all digits show same value)
  dig <= "1110" when dig_sel = "00" else  -- DIG1
        "1101" when dig_sel = "01" else  -- DIG2
        "1011" when dig_sel = "10" else  -- DIG3
        "0111";                          -- DIG4

  -- Active-low hex decoder (common cathode)
  with hex_value select
     seg <= "0000001" when x"0",  -- 0
           "1001111" when x"1",  -- 1
           "0010010" when x"2",  -- 2
           "0000110" when x"3",  -- 3
           "1001100" when x"4",  -- 4
           "0100100" when x"5",  -- 5
           "0100000" when x"6",  -- 6
           "0001111" when x"7",  -- 7
           "0000000" when x"8",  -- 8
           "0000100" when x"9",  -- 9
           "0001000" when x"A",  -- A
           "1100000" when x"B",  -- B
           "0110001" when x"C",  -- C
           "1000010" when x"D",  -- D
           "0110000" when x"E",  -- E
           "0111000" when others; -- F
end Behavioral;
```


Quartus Prime Lite Edition - D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SEVEN_SEGMENT_DISPLAY_INTERFACE/SEVEN_SEGMENT_DISPLAY_INTERFACE - SEVEN_SEGMENT_DISPLAY_INTERFACE
SEVEN_SEGMENT_DISPLAY_INTERFACE.vhd*
Compilation Report - SEVEN_SEGMENT_DISPLAY_INTERFACE
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity SEVEN_SEGMENT_DISPLAY_INTERFACE is
Port (
clk : in STD_LOGIC; -- 4MHz clock (PIN_23)
rst : in STD_LOGIC; -- Active-high reset (PIN_25)
seg : out STD_LOGIC_VECTOR(6 downto 0); -- Active-low segments a-g
dig : out STD_LOGIC_VECTOR(3 downto 0) -- Active-low digit enables
);
end SEVEN_SEGMENT_DISPLAY_INTERFACE;
architecture Behavioral of SEVEN_SEGMENT_DISPLAY_INTERFACE is
-- Clock divider signals
signal counter : unsigned(23 downto 0) := (others => '0');
signal clk_1hz : STD_LOGIC := '0';
-- Hex counter
signal hex_value : unsigned(3 downto 0) := "0000";
-- Display signals
signal dig_sel : unsigned(1 downto 0) := "00";
begin
process(clk, rst)
begin
if rst = '1' then
counter <= (others => '0');
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Programmer - D:/QUARTUS_PRIME_LITE/LAB_ACTIVITIES/SEVEN_SEGMENT_DISPLAY_INTERFACE/SE...
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detec
Delete
Add File...
Change File
Save File
Add Device
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
output_files/SEV...
EP4CE6E22
0009AAC5
0009AAC5
TDI
TDO
EP4CE6E22
Tasks
Compilation
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Type ID Message
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off SEVEN_SEGMENT_
18236 Number of processors has not been specified which may cause overloading on shared machin
204019 Generated file SEVEN_SEGMENT_DISPLAY_INTERFACE.vho in folder "D:/QUARTUS_PRIME_LITE/LAB_
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings


clk
rst
counter[23..0]
counter~[23..0]
Add1
Equal0
Equal1
Equal2
Equal3
Add0
hex_value[3..0]
dig~0
dig~1
dig~4
dig[0]~not
dig~[3..2]
dig[3..0]
seg[6..0]
Mux0
Mux1
Mux2
Mux3
Mux4
Mux5
Mux6