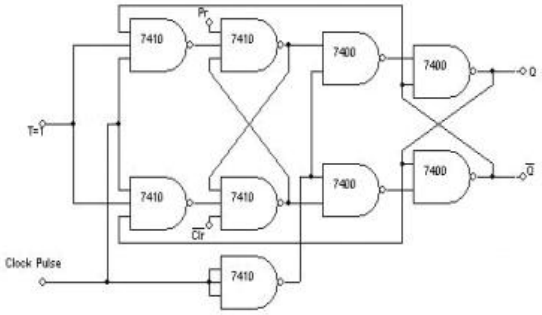
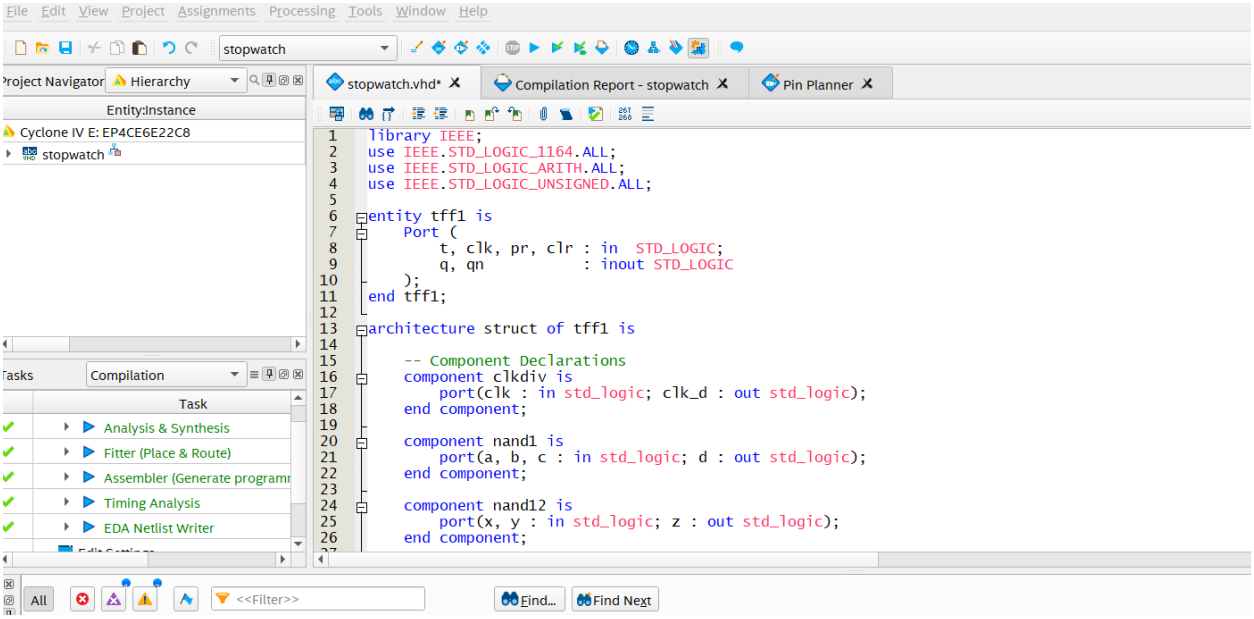
PLAZA, ELMO L. BSCpE 3-A

22. VHDL CODE FOR T FLIP-FLOP (STRUCTURAL):

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


entity tff1 is
   Port (
      t, clk, pr, clr : in  STD_LOGIC;
      q, qn           : inout STD_LOGIC
   );
end tff1;

architecture struct of tff1 is

   -- Component Declarations
   component clkdiv is
      port(clk : in std_logic; clk_d : out std_logic);
   end component;

   component nand1 is
      port(a, b, c : in std_logic; d : out std_logic);
   end component;

   component nand12 is
      port(x, y : in std_logic; z : out std_logic);
   end component;
```



```
    component nand13 is
        port(e : in std_logic; f : out std_logic);
    end component;

    -- Internal Signals
    signal s1, s2, s3, s4, s5, s6, s7, s8 : std_logic;

begin

    -- Clock divider
    u10 : clkdiv port map(clk, s7);

    -- NAND gate-based T flip-flop logic
    u1  : nand1  port map(t, qn, s7, s1);
    u2  : nand1  port map(t, s7, q, s2);
    u3  : nand1  port map(pr, s1, s4, s3);
    u4  : nand1  port map(s2, clr, s3, s4);

    u5  : nand12 port map(s3, s8, s5);
    u6  : nand12 port map(s8, s4, s6);
    u7  : nand12 port map(s5, qn, q);
    u8  : nand12 port map(s6, q, qn);

    u9  : nand13 port map(s7, s8);

end struct;
```


File Edit View Project Assignments Processing Tools Window Help
stopwatch
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22C8
stopwatch
stopwatch.vhd*
Compilation Report - stopwatch
Pin Planner
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use IEEE.STD_LOGIC_UNSIGNED.ALL;
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q, qn : inout STD_LOGIC
);
end tff1;
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-- Component Declarations
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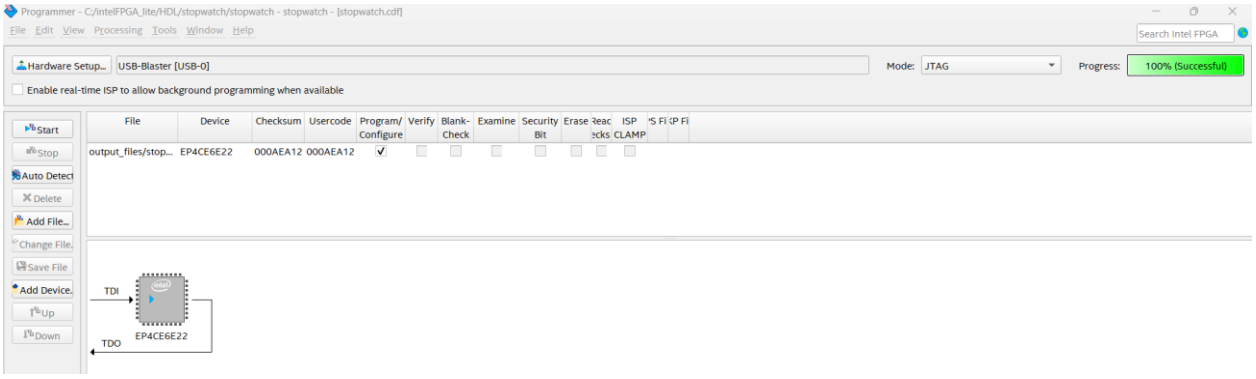
end component;
component nand1 is
port(a, b, c : in std_logic; d : out std_logic);
end component;
component nand12 is
port(x, y : in std_logic; z : out std_logic);
end component;
Tasks
Compilation
Task
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programm
Timing Analysis
EDA Netlist Writer
All
<<Filter>>
Find...
Find Next


Programmer - C:/intelFPGA_lite/HDL/stopwatch/stopwatch - stopwatch - [stopwatch.cdf]
File Edit View Processing Tools Window Help
Search Intel FPGA
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
100% (Successful)
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
Security Bit
ISP CLAMP
output_files/stop...
EP4CE6E22
000AEA12
000AEA12
TDI
TDO
EP4CE6E22