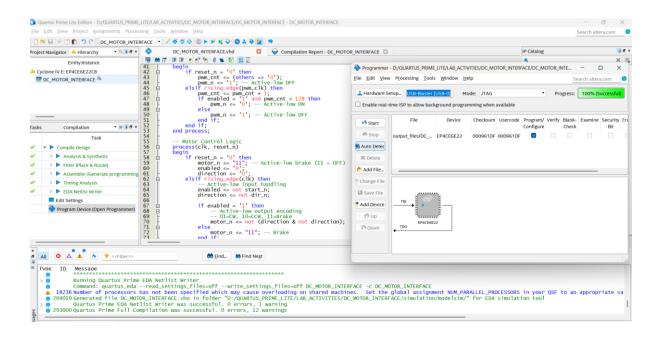
18. DC MOTOR INTERFACE

```
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.NUMERIC STD.ALL;
entity DC MOTOR INTERFACE is
Port (
  -- Active-low control inputs
  clk : in STD_LOGIC; -- PIN_23 (50MHz)
  reset n : in STD_LOGIC; -- PIN_25 (RESET button)
  start_n : in STD_LOGIC; -- PIN_88 (KEY1)
  dir n: in STD LOGIC; -- PIN 89 (KEY2)
  -- Active-low outputs
  pwm n : out STD LOGIC; -- PIN 84 (led4)
  motor n : out STD LOGIC VECTOR(1 downto 0); -- PIN 85,86 (led3,led2)
 -- Active-low status LED
  stat led n: out STD LOGIC -- PIN 87 (led1)
);
end DC MOTOR INTERFACE;
architecture Behavioral of DC MOTOR INTERFACE is
  signal pwm cnt : unsigned(7 downto 0) := (others => '0');
  signal clk div : unsigned(18 downto 0) := (others => '0');
  signal pwm_clk : STD_LOGIC := '0';
  signal enabled : STD_LOGIC := '0';
  signal direction: STD_LOGIC:= '0';
begin
  -- Clock divider (50MHz → 95Hz)
  process(clk)
  begin
    if rising_edge(clk) then
      clk div <= clk div + 1;
      pwm_clk <= clk_div(18);</pre>
    end if;
  end process;
  -- PWM Generator (active-low output)
  process(pwm_clk, reset_n)
  begin
    if reset n = '0' then
      pwm_cnt <= (others => '0');
```

```
pwm n <= '1'; -- Active-low OFF
  elsif rising edge(pwm clk) then
    pwm cnt <= pwm cnt + 1;
    if enabled = '1' and pwm_cnt < 128 then
      pwm_n <= '0'; -- Active-low ON
      pwm n <= '1'; -- Active-low OFF
    end if;
  end if;
end process;
-- Motor Control Logic
process(clk, reset n)
begin
  if reset_n = '0' then
    motor n <= "11"; -- Active-low brake (11 = OFF)
    enabled <= '0';
    direction <= '0';
  elsif rising_edge(clk) then
    -- Active-low input handling
    enabled <= not start n;
    direction <= not dir n;
    if enabled = '1' then
      -- Active-low output encoding
      -- 01=CW, 10=CCW, 11=Brake
      motor_n <= not (direction & not direction);</pre>
    else
      motor n <= "11"; -- Brake
    end if:
  end if;
end process;
-- Active-low status LED (ON when enabled)
stat led n <= not enabled;
```

end Behavioral;



Named: * Y	💨 Edit: 🗡	PIN_88									Filter
Node Name	Direction	Location	I/O Bank	VREF Group	itter Location	I/O Standard	Reserved	ırrent Streng	Slew Rate	ifferential Pai	ict Preservati
L dir_n	Input	PIN_89	5	B5_N0	PIN_89	2.5 V		8mA (default)			
motor_n[1]	Output	PIN_86	5	B5_N0	PIN_86	2.5 V		8mA (default)	2 (default)		
motor_n[0]	Output	PIN_85	5	B5_N0	PIN_85	2.5 V		8mA (default)	2 (default)		
at pwm_n	Output	PIN_84	5	B5_N0	PIN_84	2.5 V		8mA (default)	2 (default)		
- reset_n	Input	PIN_25	2	B2_N0	PIN_25	2.5 V		8mA (default)			
- start_n	Input	PIN_88	5	B5_N0	PIN_88	2.5 V		8mA (default)			
stat_led_n	Output	PIN_87	5	B5_N0	PIN_87	2.5 V		8mA (default)	2 (default)		
< <new node="">></new>											

Operation	stat_led_n	led2_n	led3_n	led4_n
Mode	(PIN_87)	(PIN_86)	(PIN_85)	(PIN_84)
Power-off	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)
Reset active	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)
Idle (start_n=1)	1 (OFF)	1 (OFF)	1 (OFF)	1 (OFF)
CW rotation	0 (ON)	1 (OFF)	0 (ON)	PWM (blinking)
CCW rotation	0 (ON)	0 (ON)	1 (OFF)	PWM (blinking)

