Module Control Card Tests

The Module Control Card tests are numbered in the 1000s.

Configuration

Test 1001

Pin Verification Fixture Tests Flag

This test passes if Test 502 determines that the Pin Verification Fixture is present. A passing result allows you to run the tests that need the Pin Verification Fixture.

If **Disable Test Restrictions** is set to **yes**, this test does not need to pass before Pin Verification Fixture tests are run.

Test 1002

Pin Verification Fixture Not Allowed Flag

This test fails if Test 502 determines that the Pin Verification fixture is present. This test is the functional complement of Test 1001.

Some tests in the diagnostics test set are nearly duplicates, one test will require the fixture, and do a slightly better job of isolating failures, while a second test does not need to use the fixture, and cannot isolate to the same level. It would waste time to run both tests; the fixture tests do a more thorough job. Test 1002 passes when the fixture is not present. This passing result is used to run those tests that should run only when the fixture is not present.

If **Disable Test Restrictions** is set to **yes**, this test does not need to pass before the non-fixture tests are run.

Test 1003

DUT Power Supply Required Flag

This test passes if DUT power supplies are present in the system config file. The passing result means that the DUT power supply tests can be run.

If **Disable Test Restrictions** is set to **yes**, this test does not need to pass before DUT power supply tests are run.

Test 1004

Debug Ports Test Flag

This test passes if debug ports are present in the system `config` file. The passing result means that the debug port tests can be run.

If **Disable Test Restrictions** is set to **yes**, this test does not need to pass before debug port tests are run.

Test 1005

Probe Tests Flag

This test passes if the probe is present in the system `config` file. The passing result means that the probe tests can be run.

If **Disable Test Restrictions** is set to **yes**, this test does not need to pass before probe tests are run.

Test 1006

DUT Power Supply Channels 5 and 6 Flag

This test reads the system `config` file to see whether DUT power supply channels 5 or 6 are being used. If they are, then the channels are tested by the DUT power supply tests.

Test 1007

Codeword Verification (Mux system only)

This test reads the card IDs on the testhead cards to determines what type of machine it is, and then reads the ROM installed on the System Card to verify that the codewords match the machine type.

Mother Card Fatal Error

Test 1020

M_FATER Stuck-Hard

This test checks the Mother Card fatal-error line, M_FATER, to see if it is being held in the error state.

If M_FATER is pulled all the time, many errors will occur on all cards tested, even though only one card may be causing this **master** error. There are twelve subtests. Empty slots always pass.

Table 3-1 Test 1020 Subtests

Subtest	Tested
Subtest 0	Module Control Card Over Voltage
Subtest 1	ASRU Card
Subtest 2	Pin Card Slot 2
Subtest 3	Pin Card Slot 3
Subtest 4	Pin Card Slot 4
Subtest 5	Pin Card Slot 5
Subtest 6	Pin Card Slot 7
Subtest 7	Pin Card Slot 8
Subtest 8	Pin Card Slot 9
Subtest 9	Pin Card Slot 10
Subtest 10	Pin Card Slot 11
Subtest 11	Module Control Card FATER, OV, SFGRD_HLT

Communication

Test 1030 and Test 1031

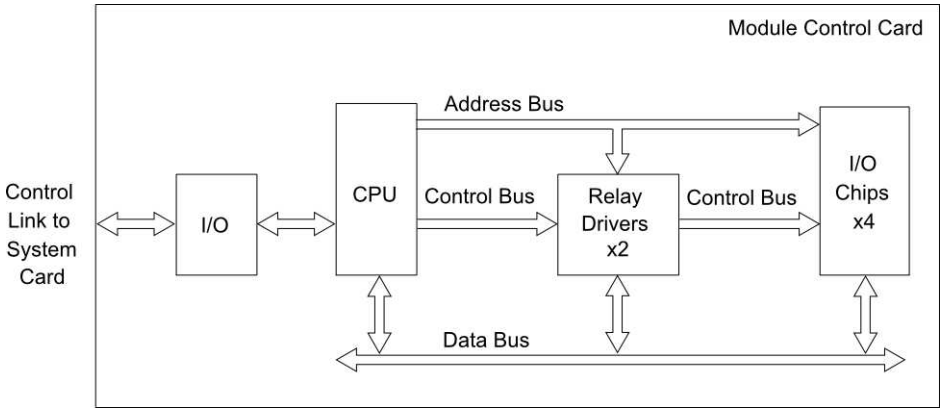
Walking ones and zeros on I/O Registers and Relay Drivers

These tests perform walking ones and walking zeros checks on the Module Control Card's I/O registers and relay driver chips. Figure shows the test path. Not all output ports can be tested (interrupts, etc.).

Table 3-2 Tests 1030 and 1031 Subtests

Subtest	Tested
Subtests 0-4	Relay Drivers
Subtests 5-19	I/O Chips

Figure 3-1 T1030



Test 1032 and Test 1033

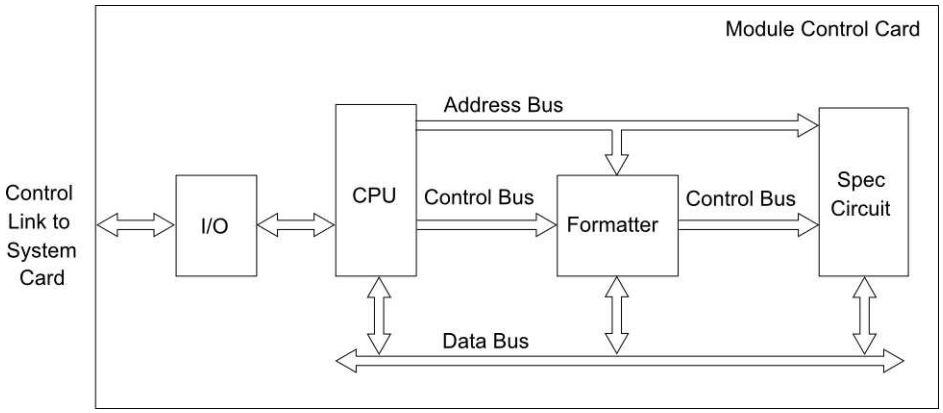
Walking ones and zeros on Format Chip and SPEC Chip

These tests perform walking ones and walking zeros checks on the Module Control Card's format chip and SPEC (system pipe and event counter) chip. Figure 3-2 shows the test path.

Table 3-3 Tests 1032 and 1033 Subtests

Subtest	Tested
Subtests 0-16	Format Chip
Subtests 17-37	System Pipe and Event Counter

Figure 3-2 Test 1032



Test 1034

Cell Address Decoding

This test writes unique data to each of several cells then reads those registers to verify cell address decoding.

Test 1035

Test Extended DRAM (Mux system only)

Requires: ControlPlus or ControlXT Card

The first 2 MB of DRAM are tested by ROM code during boot. This test checks any extended DRAM if it exists by writing test data into the memory (over any existing data) and reading it back to verify the contents. Three values are returned on failure: failing address, data stored, and expected data.

Test 1036

Walking ones and zeros CPU to Sequencer Control Register

Performs walking ones and zeros to Control Register within sequencer FPGA.

Time-Interval Counter

Test 1060

Time Interval Counter Using the AutoAdjust Routine

Requires: Test 4352

This test uses the TIC (Time Interval Counter) AutoAdjust routine to verify the functionality of the TIC. Since this procedure would change the AutoAdjust table, at the end of this test the AutoAdjust table in the testhead is restored from disk.

Test 4352 must be run before Test 1060. Test 4352 writes the AutoAdjust table to disk so it can be restored at the end of the test.

Subtest 0 through 82 test the TIC in its various modes.

DUTCLK Generator

Test 1090

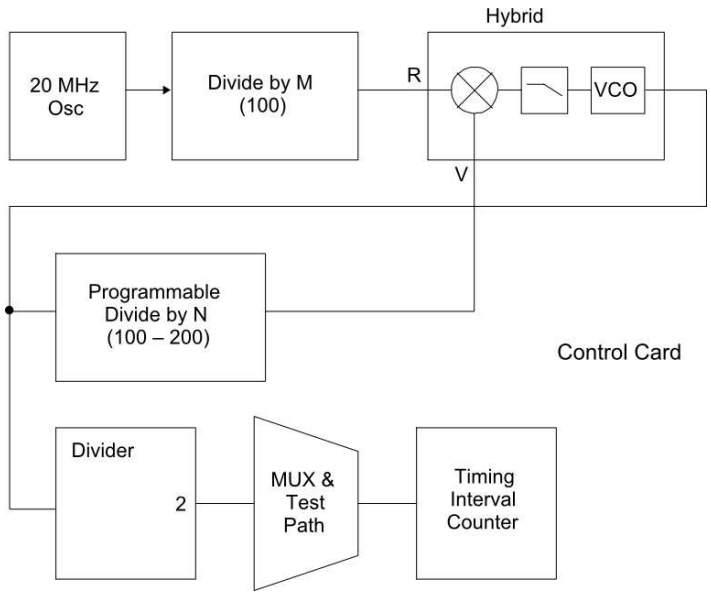
DUTCLK Generator's Divide by N, Divide by M, and Lock to Frequency

This test verifies frequency accuracy of the DUTCLK generator. The three frequencies are the maximum, the minimum and a mid-range. Frequencies chosen change each bit of the 8-bit divide-by-N divider. The output frequency divider is programmed to divide by two. Figure 3-3 on page 3-9 shows the test path.

Table 3-4 Test 1090 Subtests

Subtest	N-1 Decimal	Binary	VCO Frequency	Output Frequency
Subtest 0	99	01100011	20.0 MHz	10.0 MHz
Subtest 1	152	10011000	30.6 MHz	15.3 MHz
Subtest 2	199	11000111	40.0 MHz	20.0 MHz

Figure 3-3 T1090



Test 1091

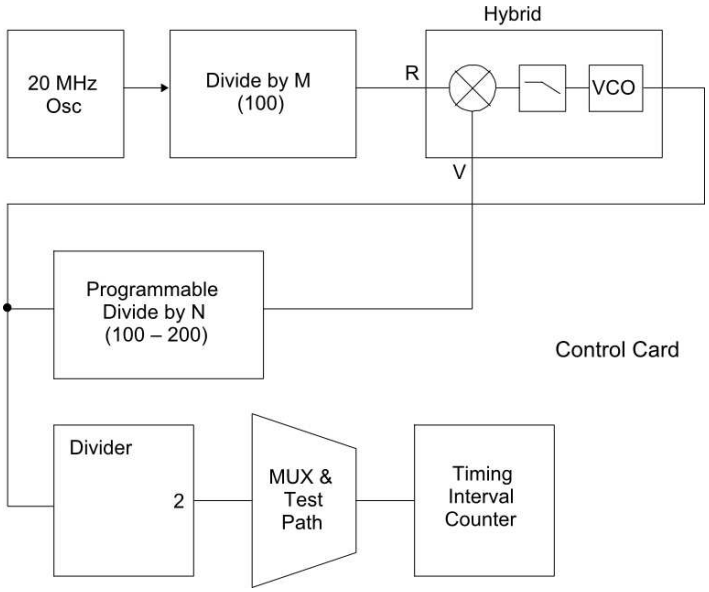
DUTCLK Generator's Output Divider

The DUTCLK VCO is set to 20 MHz and all six taps of the output frequency divider are tested. Figure 3-4 shows the test path.

Table 3-5 Test 1091 Subtests

Subtest	Divide by	Output Frequency
Subtest 0	1	20.0 MHz
Subtest 1	2	10.0 MHz
Subtest 2	4	5.0 MHz
Subtest 3	8	2.5 MHz
Subtest 4	16	1.25 MHz
Subtest 5	32	625 kHz

Figure 3-4 T1091



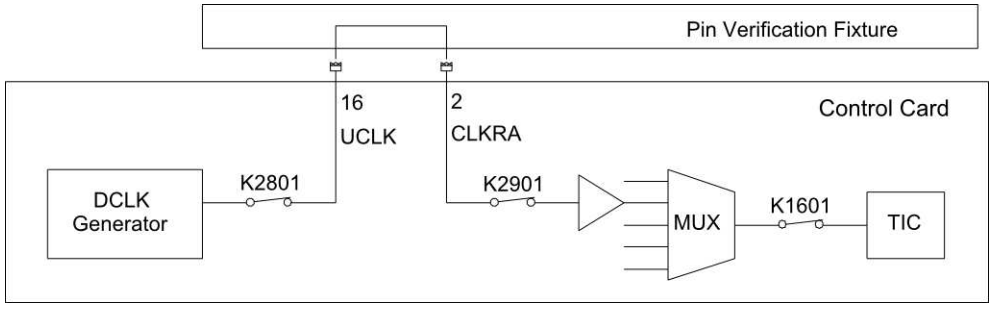
Test 1092

UCLK via the Pin Verification Fixture

Requires: Pin Verification Fixture

The DUTCLK generator is set to 10.0 MHz and sent via the UCLK MINT pins through the Pin Verification Fixture to the CLKRA input. The DCLKRA output is measured by the TIC. Figure 3-5 shows the test path.

Figure 3-5 T1092



Test 1093

ARCV and ADRV Transceivers

The DUTCLK generator drives the ADRV0 and ADRV1 lines at 10 MHz. On the ASRU Card the signals are looped back through the format chip and other hardware via the ARCV0 and ARCV1 lines. The TIC is the detector.

Table 3-6 Test 1093 Subtests

Subtest	Drive Path	TIC Channel
Subtest 0	M_ADRV0	Channel A
Subtest 1	M_ADRV0	Channel B
Subtest 2	M_ADRV1	Channel A
Subtest 3	M_ADRV1	Channel B

Test 1094

DUTCLK Output MUX

This test checks the DUTCLK ADRV[0,1] multiplexer.

Subtests 0 through 4 use the DUTCLK generator as source and the TIC as detector. These subtests check the five divider outputs from the DUTLCK generator. The DUTCLK VCO is set to 20 MHz. The path for these subtests is ADRV[0,1], ARCV[0,1], the event trigger format chip ZTCAL, the TIC A trigger MUX, and finally the TIC.

Subtests 5 through 8 select the outputs of an I/O chip (OADRV0 and OADRV1) as the MUX output. The ADRV0 and ADRV1 drive ARCV0_D and ARCV1_D which are read back via the I/O chip. Subtests 5 and 6 look at ADRV0 and ADRV1 as 0, while subtests 7 and 8 read them as a 1.

Test 1095

DUTCLK VCO Jitter

This test is done at the DUTCLK VCO's maximum and minimum frequencies. Only subtests 1 and 5 are real measurements; the other subtests are overhead.

The DUTCLK is set to 10.0 MHz with the dividers chosen so the VCO frequency is 20.0 MHz (minimum frequency). The TIC's A input is connected to a 10.0-MHz clock for reference, and the TIC's B input is connected to the DUTCLK generator's output. The standard deviation of 100 readings is used to determine jitter.

Next, the DUTCLK is set to 10.0 MHz with the dividers chosen so the VCO frequency is 40.0 MHz (maximum frequency). Standard deviation of 100 readings is again used to determine jitter.

Test 1096

DUTCLK Generator's N Divider and M Divider, and Lock to Frequency for 50 MHz

This test verifies the frequency accuracy of the DUTCLK generator. The test path is shown in Figure 3-5 on page 3-11.

TCLK Generator

Test 1120

TCLK Lock to Internal Reference

This test verifies the TCLK Generator's ability to lock to an internal reference frequency. In this test the 20.0-MHz crystal reference is used to sync the TCLK phase locked loop, and TCLK is measured by the TIC.

Test 1121

TCLK lock to DUTCLK

This test verifies the TCLK Generator's M and K dividers, and its ability to lock to DUTCLK at different frequencies. The output of the DUTCLK Generator is used as the input.

Table 3-7 Test 1121 Subtests

Subtest	m	k	Output	DUTCLK
Subtest 0	128	2	10.0 MHz	20.0 MHz
Subtest 1	64	4	10.0 MHz	20.0 MHz
Subtest 2	32	8	5.0 MHz	10.0 MHz
Subtest 3	16	16	2.5 MHz	5.0 MHz
Subtest 4	8	32	1.25 MHz	2.5 MHz
Subtest 5	4	64	625.0 kHz	1.25 MHz
Subtest 6	2	128	312.5 kHz	625 kHz
Subtest 7	2	256	156.2 kHz	625 kHz

Test 1122

TCLK Generator VCO at Maximum and Minimum Frequencies

This test checks the TCLK Generator at the maximum and minimum frequencies of the VCO. In subtest 0 the VCO is set to 41.0 MHz and divided by 4 before measurement. In subtest 1 the VCO is set to 21.5 MHz and divided by 2.

Test 1123

TCLK Out-of-Lock Detector

In subtest 0 the TCLK Generator is set to 20.0 MHz and locked to a 20-MHz clock from the DUTCLK Generator. The out-of-lock detector output, TCLKUL/, is read to verify that lock has occurred.

In subtest 1 the DUTCLK Generator output is changed to 2.0 MHz, a frequency that the TCLK Generator cannot lock to for this combination of M and K. Again TCLKUL/ is read to verify the out-of-lock condition.

For subtest 2 the DUTCLK Generator is changed to 20 MHz again, and the TCLKUL/ is read to verify lock.

Test 1124

GTCLK Divider MUX to TIC through EVENT TRIGGER

GTCLK is routed via the event trigger circuitry to the TIC for measurement. Subtests 0 through 7 test the various taps of the GTCLK divider MUX.

Table 3-8 Test 1124 Subtests

Subtest	Frequency Measured
Subtest 0	20.0 MHz
Subtest 1	10.0 MHz
Subtest 2	5.0 MHz
Subtest 3	2.5 MHz
Subtest 4	1.25 MHz
Subtest 5	625 kHz
Subtest 6	312.5 kHz
Subtest 7	156.25 kHz

Test 1125

TCLK Edge Sense Select

The TCLK Generator is synced to the DUTCLK Generator at 1.0 MHz. TCLK is connected to the TIC's B input, DUTCLK is connected to the TIC's A input as a reference signal. The TCLK Generator's timing is advanced to lead the DUTCLK. Subtest 0 measures the timing difference from TCLK to DUTCLK with rising edge selected on the TCLK Generator's input. Subtest 1 measures the timing again with the falling edge selected. Subtest 2 compares the two readings to verify the timing changed by one half the period at 1.0 MHz.

Test 1126

TCLK Timing Advance

The TCLK Generator is synced to the DUTCLK Generator at 1.0 MHz. The TCLK Generator is connected to the TIC's B input, and the DUTCLK Generator is connected to the TIC's A input. The TCLK advance is measured against DCLK.

Subtests 0 through 40 verify advances of 0 nanoseconds through 40 nanoseconds. Subtest 41 through 66 measure advances of 155 nanoseconds through 180 nanoseconds.

Test 1127

TCLK VCO Jitter

TCLK is synced to DUTCLK at 10.25 MHz with the TCLK dividers set so the TCLK VCO frequency is 41.0 MHz (the maximum). DUTCLK and TCLK timing are compared with the TIC to determine jitter. The standard deviation of 100 readings is used in the measurement.

TCLK is again synced to DUTCLK at 10.25 MHz, but this time the dividers are chosen so the TCLK VCO frequency is 20.5 MHz (the minimum). DUTCLK and TCLK timing are again compared with the TIC to determine jitter. Again, the standard deviation of 100 readings is used.

Only Subtests 1 and 5 are measurements; all other subtests are overhead.

Test 1128

TCLK Generator Symmetry

The TCLK Generator is synced to a 20-MHz clock input and sent to the TIC for measurement. Subtest 0 measures the length of the positive pulse, and subtest 1 measures the length of the negative pulse. Subtest 2 makes the comparison and evaluates the symmetry.

Test 1129

TCLK to ARCV Path

The TCLK Generator is synced to a 20.0-MHz clock and set to output 10.0 MHz onto the ADRV1 line. This drives ARCV1_D to the Event Trigger format chip. From the Event Trigger the signal is sent via ZTCAL to the TIC input A MUX through K1601 to the TIC. Subtest 0 measures the output frequency.

In this test the Mother Card drivers for ARCV[0,1]_D are disabled so the lines are local to the Module Control Card.

Test 1130

CLKRA input to TCLK via the Pin Verification Fixture

Requires: Pin Verification Fixture

The DUTCLK Generator is set to 10.0 MHz. The output is sent to the UCLK fixture interface pin, through the Pin Verification Fixture, to the CLKRA fixture interface pin. The TCLK Generator is synced to CLKRA. Subtest 0 measures TCLK with the TIC to verify it is 10.0 MHz.

Test 1131

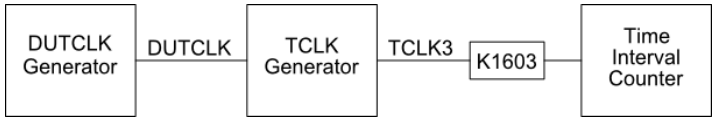
TCLK m and k Dividers by Locking to the 50-MHz DUTCLK

The M and K dividers of the TCLK generator are checked for accuracy with TCLK driven by a 50-MHz DUTCLK signal (Figure 3-6). The frequency accuracy of the TCLK generator output is verified by the TIC.

Table 3-9

Subtest	Output	DUTCLK
Subtest 0	20.0 MHz	40.0 MHz
Subtest 1	12.5 MHz	50.0 MHz thru CLKRA
Subtest 2	12.5 MHz	50.0 MHz thru CLKRB

Figure 3-6 T1131



Sequencer

- Test 1152
- Test 1153
- Test 1154
- Test 1155
- Test 1156
- Test 1157
- Test 1158
- Test 1159
- Test 1160
- Test 1161
- Test 1162
- Test 1163
- Test 1165
- Test 1175
- Test 1176
- Test 1177
- Test 1180
- Test 1182
- Test 1187
- Test 1192
- Test 1201
- Test 1202
- Test 1204
- Test 1250
- Test 1251
- Test 1252
- Test 1253
- Test 1254
- Test 1255
- Test 1256
- Test 1257
- Test 1258
- Test 1259
- Test 1260
- Test 1261
- Test 1262
- Test 1263
- Test 1264
- Test 1265
- Test 1266
- Test 1267
- Test 1268
- Test 1270
- Test 1273
- Test 1274

Test 1152

Pipe Enable and Disable

This test verifies that the buffered output of the ControlXTPA/ControlXTP Card pipe can be enabled and disabled. The pipe is a controlled sequence of registers for control data.

Test 1153

Extended Directory RAM Pointer

This test verifies that the extended directory RAM pointer of the ControlXTPA/ControlXTP Card functions properly. Subtests 0 through 7 are executed when only 8 kilobytes of directory RAM exists; subtests 8 through 15 are executed for 32 KB of RAM; and subtests 16 through 23 are executed for 128 KB of RAM.

Test 1154

Extended Sequence RAM Pointer

This test verifies that the extended sequence RAM pointer of the ControlXTPA/ControlXTP Card functions properly. Subtest 0 through 7 are executed when only 64 KB of sequencer RAM exists; subtests 8 through 15 are executed for 256 KB of RAM; and subtests 16 through 23 are executed for 1 MB of RAM.

Test 1155

Test extended piped counter

ControlPlus card (Mux systems only)

This test verifies that the extended response RAM pointer of the ControlPlus Card functions properly. Subtest 0 through 3 are executed when only 64 kilobytes of the response RAM exists; subtests 4 through 7 are executed for 256 kilobytes of RAM; and subtests 8 through 11 are executed for 1 MB of RAM.

Test 1156

Test extended directory RAM

ControlPlus card (Mux systems only)

Performs a walking 1's test on the extended directory RAM to check for proper storage.

Test 1157

Test Extended Sequence RAM

ControlPlus card (Mux systems only)

Performs a walking 1's test on the extended sequence RAM to check for proper storage.

Test 1158

Extended Status Bits

This test verifies that the SEQ_CHL and SEQ_STT4 status bits of the ControlXTPA/ControlXTP Card are working by setting them both to ones, then zeros, and then alternating. The SEQ_CHL status bit indicates to ControlXTPA/ControlXTP Card circuitry that the sequencer is in a counted homing loop (CHL). The SEQ_STT4 status bit is a general-purpose polled status bit.

Test 1159

Fail-Halt-Hold-Off Function

This test verifies that the Fail-Halt-Hold-Off function of the ControlXTPA/ControlXTP Card is working properly. This is accomplished by using a Hybrid Card to generate the fail signal by driving a binary one and expecting a binary zero. The Fail-Halt-Hold-Off function is used during the C&D process to delay (hold off) a failure halt for a given vector count.

Test 1160

Test Extended Sequence Length Counter

ControlPlus card (Mux systems only)

The sequencer executes a linear sequence with the vector counter enabled and then halts normally. The CPU reads the vector counter to verify an accurate count.

Test 1161

Loop Counter

The loop counter is tested by performing a series of functions with it. The vector counter and various status bits are then used to determine the performance of these functions.

The loop counter is used for various sequencer-related functions. It is used as the counter in counted homing loops (CHLs). An example of a homing loop is a conditional loop in programming. A counted homing loop is a homing loop that is exited if the exit condition has not occurred after a certain count.

Test 1162

Extended Response RAM and SRP (Sequence RAM Pointer) Log RAM

This test uses a Hybrid Card to load the response RAM, SRP log RAM, and status log RAM with various vector patterns. Accurate storage of these patterns is then verified by reading the stored patterns back.

Test 1163

Test Parity Error Detection Circuit (Mux system only)

ControlPlus card (Mux systems only)

This test verifies that the parity error detection circuit is working properly by checking the parity error signals via an I/O chip. The parity error detection circuit uses the parity bits of the single in-line memory modules (SIMMs) to detect data errors. The parity error signals generated by the parity error detection circuit are latched by an I/O chip.

Test 1165

Extended RAM and SRP Log RAM to 256K

This system tests the response RAM, status log RAM, and SRP RAM by loading, in order:

- 64 K of 00 pattern
- 64 K of 01 pattern
- 64 K of 10 pattern
- 64 K of 11 pattern

Test 1175

Extended Piped Counter

This test verifies that the extended response RAM pointer of the ControlXTPA/ControlXTP Card functions properly. Subtest 0 through 3 are executed when only 64 kilobytes of the response RAM exists; subtests 4 through 7 are executed for 256 kilobytes of RAM; and subtests 8 through 11 are executed for 2 MB of RAM.

Test 1176

Extended Directory RAM

This test performs a walking ones test on the extended directory RAM to check for proper storage.

Test 1177

Extended Sequence RAM

This test performs a walking ones test on the extended sequence RAM to check for proper storage.

Test 1180

Extended Sequence Length Counter

The sequencer executes a linear sequence with the vector counter enabled and then halts normally. The CPU reads the vector counter to verify an accurate count.

Test 1182

Extended Response RAM and SRP (Sequence RAM Pointer) Log RAM

This test uses the Pin Card to load the response RAM, SRP log RAM, and status log RAM with various vector patterns. Accurate storage of these patterns is then verified by reading the stored patterns back.

Test 1187

Extended Sequence RAM

This test performs a walking 1's test on the extended sequence RAM to check for proper storage.

Test 1192

Extended Response RAM and SRP (Sequence RAM Pointer) Log RAM

This test uses the Pin Card to load the response RAM, SRP log RAM, and status log RAM with various vector patterns. Accurate storage of these patterns is then verified by reading the stored patterns back.

Test 1201

ID Code of Sequencer FPGA

Pass/Fail test that verifies correct FPGA for sequencer.

Test 1202

Done Bit of Sequencer FPGA

Pass/Fail test that verifies programming completed successfully for sequencer.

Test 1204

5-pin Port Verification

Pass/Fail test that verifies 5-pin port functionality.

Test 1250

Directory RAM Pointer and Sequence RAM Pointer

This test checks the directory RAM pointer, sequence RAM pointer, vector counter, and piped counter. (The vector counter and piped counter are in the custom system pipe and event counter chip or SPEC.)

Subtest 0 loads the directory RAM pointer with zeros, then reads it to verify it contains those zeros. ones are loaded and read in subtest 1. The directory RAM itself is addressed in subtest 2. Addressing the RAM causes the directory RAM counter to increment, and, since is all ones, it folds back to all zeros. Reading the counter again verifies it contains zeros.

A similar procedure is used to test the other pointer and counters in the remaining subtests. Subtests 3 through 5 test the sequence RAM pointer. The SPEC chip's vector counter is tested in subtests 6 through 8, and SPEC's piped counter is the target of subtests 9 through 11.

Test 1251

Sequencer RAMs

This test checks the SCLK Timing RAM, the FCLK Timing RAM, the Directory RAM, and the Sequencer RAM.

Test 1252

Instructions and Log RAM

This test sets up and executes a sequencer program that uses all sequencer instructions except the conditional branch.

After the program is set up and run, subtest 0 reads the sequencer status. Subtest 1 reads the vector counter in the SPEC chip. Subtests 2 through 17 read the sequence RAM pointer log RAM. Subtests 18 through 33 read the status log RAM.

Test 1253

CPU / Sequencer Handshake, Max SCLK Frequency, and Status Register

This test verifies sequencer operation. Subtests 0, 2 and 3 read from the status register. Subtest 1 makes a measurement of SCLK at maximum frequency, but note that the returned value is one half the SCLK frequency. Subtest reads the vector counter.

Test 1254

32K Linear Sequence

In this test a 32K long sequence of vectors is driven. In the single subtest, subtest 0, the Sequencer's vector counter returns the number of vectors that where handled.

Test 1255

Buffers from Vector Address Bus to Timing RAM

This test verifies the sequencer timing circuitry by making frequency measurements of the resultant signal. There are two subtests, 0 and 1.

Test 1256

Safeguard Halt

This test verifies the Safeguard halt feature. Subtests are numbered 0 through 3.

Test 1257

Vector Count Halt

This test verifies halting on vector count. Subtest 0 reads the status register to prove halt occurred. Subtest 1 reads the vector counter to show where the halt took place. Subtest 2 reads the halt comparator. Subtests 3 through 10 read results logged in the response RAM.

Test 1258

Halt Global Fail

This test verifies sequencer halt on global fail. Subtest 0 reads the status register to prove the sequencer has halted on a failure. Subtest 1 reads the vector counter to show where the halt took place.

Test 1259

FCLK

Requires: Pin Verification Fixture

This test verifies FCLK. There are three subtests, 0 through 2, that represent FCLK0 through FCLK2.

Test 1260

Global Fail Readback

This test verifies the readback of the global fail bit. Subtest 0 and 1 read the bit expecting 1 in the first case and 0 in the second.

Test 1261

Sync Comparator to Timing Interval Counter

This test verifies the sync comparator input to the TIC's channels A and B and sequencer arming of TIC. Subtest 0 and 1 are timing measurements done with the TIC.

Test 1262

Sync Comparator Timing Interval Counter

This test verifies sync comparator arming on the TIC. Subtest 0 is a timing measurement made with the TIC.

Test 1263

SRP and Status Log RAMs

In this test the sequencer is run to load the RAMs, and then the RAMs are read to verify their contents.

Test 1264

Response RAM

In this test the sequencer is run to load the Response RAM, and then the RAM is read to verify its contents.

Test 1265

Halt on Fatal Error

Requires: Pin Card

This test verifies the Module Control Card's ability to detect a fatal error (FATER) and halt in response.

The test is done at 10 MHz. The first Pin Card found in the module is connected so that all its receivers are hooked to the ASRU Card source. Receiver high is set to +3.5 volts, and the ASRU source is programmed to -10.0 volts. A 50-ohm load is placed on this circuit to keep the source from supplying the full voltage at first. With the 50-ohm load in place, no overvoltage will occur. Removal of this 50-ohm load later will cause the source to go to -10.0 volts. This will create an overvoltage condition and a fatal error.

The test starts a sequencer program. In subtest 0, the status register is read to prove that there are no errors.

The 50-ohm load is taken out. With an overvoltage condition created, the sequencer should now halt. In subtest 1, reading the status register proves that the sequencer halted on the fatal error.

Test 1266

CPU/Sequencer handshake, Max SCLK Frequency, and Status Register for 317x Systems

This test is identical to Test 1253 except for the maximum frequency tested: 6-MP/s Module Control Cards.

This test verifies sequencer operation. Subtests 0, 2, and 3 read from the status register. Subtest 1 makes a measurement of SCLK at maximum frequency, but note that the returned value is one-half the SCLK frequency.

Test 1267

Halt on Vector Count

This is a 20-MP/s version of test 1257.

Test 1268

Halt on Mother Card Fail

This is a 20-MP/s version of test 1258.

Test 1270

Global Fail Line to I/O Readback

This test forces a global fail signal by asserting a local fail, which is then clocked into the high-speed link pipe and read from the global halt line.

Test 1273

SRP (Sequence RAM Pointer) Log RAM and Status Log RAM

This test is a 20-MP/s version of test 1263. The sequencer loads the two types of RAM with alternating ones and zeros, and then verifies accurate storage. The test is then executed again with the bit patterns reversed.

Test 1274

Response RAM

This is a 20-MP/s version of test 1264. The response RAM is loaded with alternating ones and zeros patterns, and then verifies accurate storage.

High-Speed Link

Test 1280

CPU Branching Through the High-Speed Link

This test checks the ability of the CPU to branch via the high-speed link. There are eight subtests: even subtests evaluate the sequencer status register, and odd subtests evaluate the vector counter.

Test 1281

Sequencer Start and Stop Through the High-Speed Link

This test verifies the ability of the sequencer to be started and stopped through the high-speed link in both directions. Subtests 0 through 2 verify the safeguard halt capability in one direction. Subtest 0 reads the vector counter before the sequencer is started. Subtest 1 reads the status register to verify that safeguard halt occurred. Subtest 2 reads the vector counter after the halt. Subtests 3 through 5 are the same as subtests 0 through 3, except that they test the link in the opposite direction.

Test 1282

Sequencer Branching Through the High-Speed Link

This test verifies the ability of the sequencer to branch via the high-speed link. Subtest 0 reads the status register to verify that branch on fail occurred. Subtest 1 reads the vector count after the halt. Subtests 2 and 3 are the same as subtests 0 and 1, except that they test the link in the opposite direction.

Test 1283

HPSYNC Lines

This test verifies the operation of the HPSYNC lines. The ten subtests are numbered 0 through 9.

Test 1284

HCAL Path

This test verifies the HCAL path. Subtests 0 and 1 are frequency measurements done with the Time Interval Counter.

NOTE **If there is a stuck open relay in the HCAL path it will cause test 1284 to fail for all Module Control Cards other than the card with the faulty relay.**

Test 1285

CAL Path for 2-Module Systems

This test is identical to Test 1284 except for test frequency.

It creates a loop through the other modules and pipes a frequency through them. Then it measures the frequency with the Time Interval Counter (TIC). This first checks the con_xl to TIC path, then the TIC calibration.

Test 1292

Sequencer Branching Through the High-Speed Link

This test is a 20-MP/s version of test 1282.

Test 1295

Prepare for Multi-Module Semaphore Tests

This test sets up the Semaphore (high-speed link) tests: depending on the number of modules present, it will run test 1296, 1297, 1298 or 1299.

Test 1296

One-Module Semaphore Test

This test checks the high-speed link Semaphore hardware in a one-module testhead.

Test 1297

Two-Module Semaphore Test

This test checks the high-speed link Semaphore hardware in a two-module testhead.

Test 1298

Three-Module Semaphore Test

This test checks the high-speed link Semaphore hardware in a three-module testhead.

Test 1299

Four-Module Semaphore Test

This test checks the high-speed link Semaphore hardware in a four-module testhead.

Event Trigger

Test 1310

Event Capture Window

Requires: Pin Verification Fixture

This test verifies the event trigger's capture window. The four subtests, subtests 0 through 3 test the circuit at two delays, -30 nanoseconds and +100 nanoseconds. Even numbered subtests should fail to catch the event, and odd numbered tests should catch the event.

Test 1311

Event Trigger Relays and Trigger Conditions

Requires: Pin Verification Fixture

This test verifies the event trigger input relays and trigger conditions. There are 10 subtest. Event trigger channels ET1A through ET3B are tested in subtests 0 through 5, and combinations of these lines are tested together in subtests 6 through 9. The disconnect relays associated with each of these channels are K1801 (ET1A) through K1806 (ET3B), respectively.

Test 1312

Event Trigger Pipe Delay

This test verifies the event trigger pipe delays. Measurements are made with the TIC, and subtests 0 through 7 verify eight different pipeline delays.

Test 1313

ztcal Relay K1807

This test verifies the functionality of relay K1807, ztcal input to the event trigger.

Miscellaneous High-Speed Link

Test 1340

TCLK Lock to Other Modules

This test verifies the high-speed link's inputs to the TCLK.

Test 1341

High-Speed Link Cables Connection

This test verifies the high-speed link cable are connected in the proper order.

Test 1342

Multi-Module Lock to TCLK

In this test all sequencers are started together, then measurements are made on the timing of Hybrid Card drivers in all modules to insure that all sequencers started on the same TCLK edge.

Debug Signal

Test 1370

Verify Debug Signal MUX

Requires: Pin Verification Fixture

This test verifies the Debug MUX circuitry. MDB[0,2] are connected through the Pin Verification Fixture.

Table 3-10

Subtest	Debug Pin	Source
Subtest 0	MDB0	SYNC_CMP
Subtest 1	MDB0	SCLK
Subtest 2	MDB0	SYNC_SR
Subtest 3	MDB1	SCLK
Subtest 4	MDB1	GTCLK
Subtest 5	MDB1	TCLK
Subtest 6	MDB1	ARCV0
Subtest 7	MDB1	ZTCAL
Subtest 8	MDB1	ET_STRIG
Subtest 9	MDB2	ARCV0
Subtest 10	MDB2	ARCV1
Subtest 11	MDB2	ET_STRIG

Test 1371

Verify Debug Paths Through the High-Speed Link

Requires: Pin Verification Fixture and two modules

This test generates signals on one module and measures them on another.

Test 1372

Debug Ports

Requires: Pin Verification Fixture, test cable, and manual intervention.

This test checks the debug ports at the side of the testhead.

Test 1373

Verify Debug Signal Selection MUX for 317x Systems

Requires: Pin Verification Fixture

This test is a 317x system version of Test 1370. They are identical except for test frequency.

This test verifies the Debug MUX circuitry. MDB[0,2] are connected through the Pin Verification Fixture.

Table 3-11

Subtest	Debug Pin	Source
Subtest 0	MDB0	SYNC_CMP
Subtest 1	MDB0	SCLK
Subtest 2	MDB0	SYNC_SR
Subtest 3	MDB1	SCLK
Subtest 4	MDB1	GTCLK
Subtest 5	MDB1	TCLK
Subtest 6	MDB1	ARCV0
Subtest 7	MDB1	ZTCAL
Subtest 8	MDB1	ET_STRIG
Subtest 9	MDB2	ARCV0
Subtest 10	MDB2	ARCV1
Subtest 11	MDB2	ET_STRIG

Test 1380

Debug Signal MUX

Requires: Pin Verification Fixture

This test verifies the Debug MUX circuitry. MDB[0,2] are connected through the Pin Verification Fixture.

Table 3-12 Test 1380 Subtests

Subtest	Debug Pin	Source
Subtest 0	MDB0	SYNC_CMP
Subtest 1	MDB0	SCLK
Subtest 2	MDB0	SYNC_SR
Subtest 3	MDB1	SCLK
Subtest 4	MDB1	GTCLK
Subtest 5	MDB1	TCLK
Subtest 6	MDB1	ARCV0
Subtest 7	MDB1	ZTCAL
Subtest 8	MDB1	ET_STRIG
Subtest 9	MDB2	ARCV0
Subtest 10	MDB2	ARCV1
Subtest 11	MDB2	ET_STRIG

Test 1381

Debug Paths Through High-Speed Link

Requires: Pin Verification Fixture and two modules

This test generates signals on one module and measures them on another. This is the same as Test 1371, but for the ControlXT Card only.

GP Relay

Test 1400

GP Relays, Autofile, and Fixture Enable

Requires: Pin Verification Fixture

This test verifies the GP relays, the Autofile pins, and Fixture Enable 1. There are 33 subtests numbered from 0 through 32. Fixture Enable 0 is hardwired to ground in the Pin Verification Fixture, as it is in other fixtures. Fixture Enable 1 can be grounded with a GP relay via connections in the Pin Verification Fixture. The Autofile pins can also be grounded, some via GP relays, others through switched ground pins. The Safety Disable pin can be grounded with a switched ground.

Table 3-13 Test 1400

Pin Tested	Autofile 0	Autofile 1	Autofile 2	Autofile 3
Pin Number	66	67	68	69
Grounded By	General-Purpose 1	General-Purpose 2	General-Purpose 3	General-Purpose 4
Pin Numbers	48, 49 and 18	50, 51, and 20	52, 53, and 22	54, 55, and 39
Pin Tested	Autofile 4	Autofile 5	Autofile 6	Autofile 7
Pin Number	70	71	72	73
Grounded By	General-Purpose 5	General-Purpose 6	General-Purpose 7	General-Purpose 8
Pin Numbers	56, 57 and 41	58, 59, and 44	60, 61, and 46	62, 63, and 78
Pin Tested	Autofile 8	Autofile 9	Autofile 10	Autofile 11
Pin Number	74	75	76	77
Grounded By	Clk Rcvr Sw Gnd	Event Trg1 Sw Gnd	Event Trg2 Sw Gnd	Event Trg3 Sw Gnd
Pin Number	1	5	8	11
Pin Tested	FX_EN1/	SAF_DIS		
Pin Number	40	43		
Grounded By	General-Purpose 2	User Clock Gnd		
Pin Number	50, 51 and 20	15		

Subtest 0 reads the Autofile (also known as fixture id) with no Autofile pins grounded. This should return the number 0, the normal Autofile number of the Pin Verification Fixture.[1] In the Autofile, Fixture Enable and Safety Disable scheme, no connection is a 0 and grounded is a 1.

Subtest 1 reads Fixture Enable 0, Subtest 2 reads Fixture Enable 1, and Subtest 3 reads the Safety Disable. Only Fixture Enable 0 should return a 1; it is hardwired to ground. Safety Disable and Fixture Enable 1 should return 0.

In subtests 4 through 6, General-Purpose Relay 1 is closed. With General-Purpose Relay 1 closed, Subtest 4 reads the Autofile again. Autofile 0 is connected to ground through GP1 and Pin Verification Fixture traces. The Autofile number will change; it should return 1 now. This tests Autofile 0, the least significant Autofile bit. Subtest 5 reads Fixture Enable 0 which is hardwired to ground and should remain 0. Subtest 6 reads Fixture Enable 1. It is not grounded via GP1, so should remain 0. General-Purpose 1 is then opened.

Subtests 7 through 9 repeat the procedure with General-Purpose 2 closed. In Subtest 7 Autofile should be 2. This is Autofile 1. For subtest 8 Fixture Enable 0 will remain 1. Subtest 9 checks Fixture Enable 1 which is also grounded via GP2, and should now become 1. GP2 is opened.

Subtests 10 through 12 repeat this scheme with General-Purpose 3 closed, and so on. Subtests 13 through 27 finish this testing with all the other General-Purpose Relays. Only the Autofile numbers should change. In each subtest the next higher order Autofile bit is verified.

NOTE

If you set Disable Test Restrictions = Yes in the DGN Config screen, then run test 502 from Test Number Entry before test 1400.

If you don't, you will get false failures of subtests 22 and 25.

Subtests 28 through 31 continue testing the Autofile pins, this time with various switched ground pins used to ground the Autofile bits instead of General-Purpose Relays. In subtest 28, Clk Receiver Sw Gnd is used to check Autofile 8. Subtest 29 uses Event Trig 1 Sw Gnd to check Autofile 9, subtest 30 checks Autofile 10 with Event Trig 2 Sw Gnd, and subtest 31 verifies Autofile 11 with Event Trig 3 Sw Gnd.

Subtest 32 verifies Safety Disable by grounding it with User Clock Ground. Also tested by usage are the various ground pins that are used to create the grounding of Autofile, Fixture Enable, and Safety Disable pins.

1. In this case, if the Autofile number was not 0 when the a normal run of diagnostics started, this test would not be allowed to run. You could, however, force it to run from Test Number Entry.

Test 1401

Fixture Enable 0

Requires: No fixture present

This test verifies fixture enable is 0 with no fixture in place. This test is run when the Pin Verification Fixture is released, and verifies that Fixture Enable 0 is not grounded.

Test 1400 tests the other state of Fixture Enable 0.

Data Transfer

Test 1501

Data Transfer

This test verifies data transfer from the controller to System Card and the Module Control Cards, as well as DMA data transfers on board the System Card and Module Control Cards. It is capable of finding data transfer faults that will not prevent testhead boot.

In this test, data is sent to segments of RAM, then moved using DMA to other segments. The direction of transfer is then reversed. System Card is tested first, then the Module Control Card. After testing, the original contents of RAM and DMA registers gets restored.

Subtests 0 through 67 involve the System Card, and subtests 68 through 135 involve the Module Control Cards.

Special Tests

Test 1511

Verify the Pull-Up Resistor Value

Requires: Hybrid or HybridPlus Pin Card

This is a special-purpose test that is not structured in any testing set. There are a number of early-production Module Control Cards in systems that have a too-high valued pull-up resistor pack on certain lines. These cards will pass diagnostics but cause failures during high-speed testing. This test takes a CRC (cyclic redundancy check) at 12.5 MHz, and will catch any cards with this problem.

Run this test from **Test Number Entry** only to verify that none of the bad cards are in the system.

Test 1521

Read / Write of Format Chip Registers

This test was written because a defective format chip was found to have a register over-writing problem. To test for this problem a unique read/write pattern is used. Failure of any subtest indicates a faulty format chip.