ASRU Card Tests

The ASRU Card tests are numbered in the 2000s.

NOTE

Open Relay Tests – These tests verify that relays can be opened. If the MOA goes into compliance due to a shorted relay, the system will return the failure message:

-4.400000 L+1 ohms

This message does not represent a negative resistance, but a measurement error. Interpret this message as a shorted path.

Communications

Test 2030

ASRU Card Reset

This test toggles the motherboard-reset-bit in the MAC (control card) reset register. The M_RST/ line is asserted to reset the ASRU Card; then subtests 0 through 24 read the various registers to verify that they were reset.

Test 2031

Address Decoding

This test writes a different integer to each of the tested cells. Subtests 0 through 28 check the contents of the registers to verify that the data sent match the register contents.

Test 2032

Walk ones Through Registers

Test 2032 walks ones through the ASRU Card cells. Subtests 0 through 28 each test a different cell.

Test 2033

Walk Zeros Through Registers

Test 2033 walks zeros through the ASRU Card cells. Subtests 0 through 28 each test a different cell.

Test 2034

Walk Ones Through RAM

Subtest 0 performs a walking ones test on the vector RAM. Subtest 1 tests the source RAM, and subtest 2 performs a walking ones test on the state capture RAM in the format chip.

Test 2035

ASRU Clock Frequency Using ARCV

This test routes the ASRU Card clock via the format chip circuitry over both the ARCV0 and ARCV1 lines to the Module Control Card and then measures its frequency on the TIC (time interval counter). Subtest 0 measures the signal via ARCV0 for TIC channel A. Subtest 1 measures the ARCV1 signal for TIC channel B.

Test 2036

Buffered ARCV Lines

This test checks the buffered ARCV lines. A signal is put onto one of the ARCV lines and the buffered version of it is routed to the Time Interval Counter (TIC) via the other line. Then the path is swapped. To get a clock from ADRV to the ARCV lines, the probe receiver is used.

The four subtests measure the TIC Channel-A frequency. Subtests 0 and 1 use the GTL0 line to route signals from one ARCV line to the other, whereas subtests 2 and 3 use the GTL1 line.

Test 2037

RAM Program Mode Override

This test writes four binary numbers to RAM in override and non-override mode; the four subtests read and verify the RAM contents.

Test 2038

Format Chip DD0 and DD1 from ADRV and Flip-Flop

This test verifies the format chip on the ASRU Card. The format chip allows drive data to be generated via the ADRV lines and from an internal flip-flop.

Of the 12 subtests, 0 through 5 verify DD0 (FSRCT). Subtest 0 uses the ADRV0 line to set DD0 high. Subtest 1 uses ADRV0 to set it low. Subtests 2 and 3 use ADRV1 to set DD0 high and low. Subtests 4 and 5 set DD0 high and low via the flip-flop. Subtests 6 through repeat the procedure for DD1 (GDCLR).

Test 2039

Format Chip SRCTS from ADRV and Flip-Flop

This test verifies the format chip's SRCTS (source output state enable control) output on the ASRU Card. The format chip allows three-state pulser data to be generated via ADRV and by an internal flip-flop. In this test only the TSP0 output is checked; that is, the format chip output line is used as SRCTS to three-state the source.

Subtests 0 and 1 use ADRV0 to set TSP0 high and then low. Subtests 2 and 3 use ADRV1 to set TSP0 high and low. Subtests 4 and 5 use the internal flip-flop to set TSP0 high and low.

Test 2040

Format Chip FDETT from ADRV and Flip-Flop

This test verifies the Format chip FDETT (detector trigger control in SCAT) output. The test double-triggers the TSP1 and checks the ASRU status register bit 6 (Detector Over-Trig bit). Subtests 0, 1 and 2 use ADRV0, ADRV1, and the internal flip-flop as the data source respectively.

Test 2041

Format Chip Receiver Data

This test verifies the ASRU Card's format chip receiver data handling. It routes the sequencer drive (SEQ_DRV0) signal through PACCAL and Probe to the GTx1 lines and also routes through PACCAL to the GTx0 lines to act as the Format chip receiver inputs. If there is a problem with the receivers, the sequencer should halt early on failure and give a low vector count.

Subtest 0 reads the status register to prove a halt-on-fail condition occurred, and subtest 1 reads the vector counter.

Test 2042

Source and Detector Trigger from the Sequencer

This test verifies source and detector triggering from the sequencer.

Test 2043

Detector Output without AIMIN

This test checks the ADC output without the AIMIN interrupt line by applying +10.0 volts and -10.0 volts to the detector, delaying the integration time, and then reading the output.

Format Chip

Test 2044

CRC on Format Chip

This test checks the format chip's CRC circuit.

Table 4-1 Test 2044 Subtests

Subtest	Function
0, 1	Read CRC register before sequencer start
2	Read status register
3	Read vector counter
4, 5	Read failure log
6, 7	Read CRC register

Test 2045

Data Logging to State Capture RAM

The ASRU Card uses one of the format chips developed for the Hybrid Pin Card. This test checks the state capture RAM.

Table 4-2 Test 2045 Subtests

Subtest	Function
0	Read hold register before sequencer start
1	Read state capture RAM pointer before sequencer start

Table 4-2 Test 2045 Subtests

Subtest	Function
2	Read sequencer status
3	Read vector counter
4	Read hold register
5	Read state capture RAM pointer
6-10	Read state capture RAM contents

Test 2046

Driver Delay Lines

The ASRU Card uses one of the format chips developed for the Hybrid Pin Card. This test checks the driver delay lines.

Table 4-3 Test 2046 Subtests

Subtest	Function
0-7	Channel 0 delay A
8-15	Channel 0 delay B
16-2	Channel 1 delay A
24-31	Channel 1 delay B

Test 2047

Receiver Delay Lines

The ASRU Card uses one of the format chips developed for the Hybrid Pin Card. This test checks the receiver delay lines.

Table 4-4 Test 2047 Subtests

Subtest	Function
0-7	Channel 0 delay A
8-15	Channel 0 delay B
16-23	Channel 1 delay A
24-31	Channel 1 delay B

Test 2048

Read / Write of Format Chip Registers

This test is used to check the register over-writing problem in the Format Chip. First, a unique bit pattern is written for each of the 16 registers and read back. Then, another unique bit pattern is used again to overwrite the registers and read back again. A failure of any of the 32 subtests indicates a faulty format chip.

Test 2051

Format Chip Receiver Data

This test is a fast-mode version of test 2041. The sequencer ADRV outputs are routed through PACCAL to the probe and the GTH0/GTL0 MUX, which acts as a receiver. If the receiver fails, an early halt occurs, giving a low vector count and a failure. If the format chip FAIL line fails to cause a halt, a large vector count occurs, which in turn yields an incorrect status.

NOTE When the pattern rate of the system is greater than 12 MP/s, piping circuitry is activated which puts the system in what is called fast-mode. All systems that operate at 20 MP/s run in fast-mode.

Test 2054

CRC on Format Chip

This test is a fast-mode version of test 2044.

Test 2055

Data Logging to State Capture RAM

This test is a fast-mode version of test 2045.

Test 2056

FAIL Pipe Enable / Disable

This test verifies that the pipe enable/disable for the format chip FAIL line is functional on the ASRU Card.

Test 2057

ARCV0 and ARCV1 Pipe Enable / Disable

This test verifies that the pipe enable/disable for the format chip ARCV0 and ARCV1 lines is functional on the ASRU Card.

Test 2058

Fail and ARCV0 and ARCV1 Pipe Enable / Disable

This test verifies that pipe enable/disable for the format chip FAIL, ARCV0, and ARCV1 lines is functional on the ASRU Card.

Test 2059

EEPROM Writeable Line

This test verifies operation of the EEPROM write disable on ASRU Card. The EEPROM's write enable is disabled and Cell 0 is read. This value in binary is reversed and then the new value is written to the EEPROM's cell 0. Once again Cell 0 is read and that value is compared to the original value. If the values are the same, then the write disable is functioning properly.

Detector

Test 2060

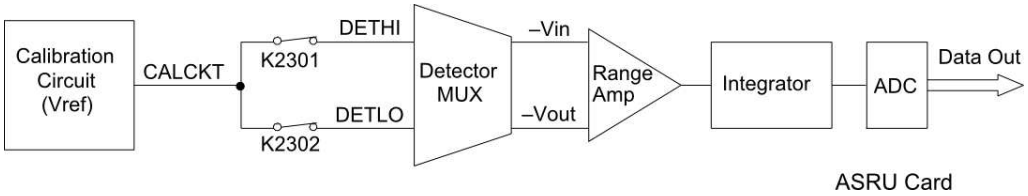
DC Detector Voltage Accuracy

The output of the calibration circuit (CALCKT) is used to test the detector on nine ranges, with half- and full-scale inputs, using long and short integration times. These are single-ended measurements; that is, one input is referenced to ground. The reference voltage output (VREF) is selected as the output on the calibration circuit.

Subtests 0 through 8 represent half-scale measurements with positive voltages applied to the positive detector input (DETHI) at short integration times. Subtests 9 through 17 are half-scale measurements with negative voltages applied to the negative input (DETLO) at short integration times.

Subtests 18 through 26 test full-scale accuracy with positive voltages applied to the negative detector input at long integration times. Subtests 27 through 35 test full-scale with negative voltages applied to the positive detector input and long integration times. Figure 4-1 shows the measurement path.

Figure 4-1 T2060



Test 2061

DC Detector Common-Mode Rejection

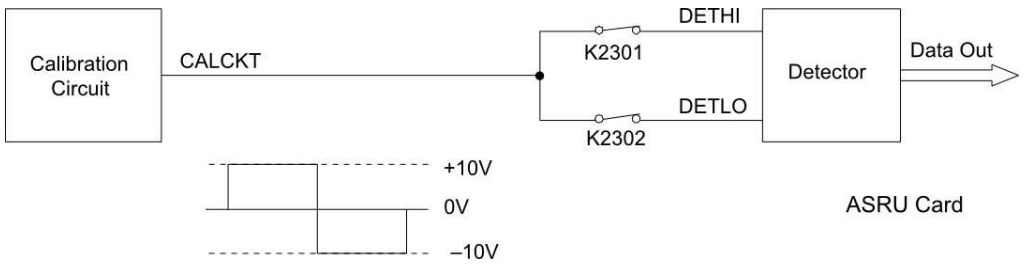
With the positive and negative detector inputs shorted, readings are taken with +10.0 and -10.0 volts of common-mode voltage applied (Figure 4-2).

The first measurements are done with short integration times. The DETHI and DETLO inputs are connected together; then, for each of nine ranges, +10.0 volts are applied to the inputs and a short-integration reading is taken. -10.0 volts are then applied and another short-integration time reading is taken. The difference between the readings is a measure of common-mode rejection (CMR).

Long integration time CMR is checked next. For each of the nine ranges, +10.0 volts are applied and a long-integration time reading is taken. -10.0 volts are applied and another long-integration time reading is taken.

The data are processed and evaluated. Subtests 0 to 8 report on all ranges using the short integration time, and subtests 9 through 17 represent the readings with long integration times.

Figure 4-2 T2061



Test 2062

DC Detector Noise

DETHI and DETLO are both grounded, and then 10 readings are taken on each range with a long integration time. Subtests 0 through 8 check each range.

Test 2063

DC Detector Overrange

The detector is tested with both negative and positive inputs, on the 5 volt range. By putting in a voltage that is very close to the trip point, the accuracy of the range amplifier can be checked. Subtest 0 uses -5.3625 volts on the 5 volt range. Subtest 0 reads the ASRU Card status register to verify no over-range condition exists. Subtest 1 applies -5.6325 volts and reads the status register to verify an over-range condition occurred. Subtests 2 and 3 repeat the procedure with +5.3625 volts and +5.6325 volts applied.

Test 2064

DC Detector Integrator Overrange, Overtrigger, and Missed Result

This test checks several detector functions.

Subtest 0 verifies the detector integrator will not flag an overrange condition too quickly with a negative input. Subtest 1 verifies a negative input can cause overrange. Subtests 2 and 3 repeat the procedure for a positive input. Subtest 4 clears the overrange condition.

Subtest 5 verifies that triggering the integrator a second time, while it is completing a reading, will cause an overtrigger condition. Subtest 6 proves that this causes the result-missed bit to be set. Subtest 7 clears the condition and verifies the reset occurred.

Test 2065

DC Detector Attenuation

This test verifies the attenuator circuit (16:1) at detector ranging input. It also checks the VR+10 and VR-10 inputs to the calibration circuit output multiplexer. Subtest 0 provides attenuated positive voltage to the detector positive input. Subtest 1 provides attenuated negative voltage to the detector negative input.

Test 2066

DC Detector Input bias current

This test places a 1-megohm resistor across the detector input and measures the bias current.

Test 2067

Digitizer Accuracy

This test verifies digitizer accuracy at six input voltages. Subtests 0 through 5 test the digitizer at +2.5, +5.0, +10.0, -2.5, -5.0, and -10.0 volts.

Source

Test 2090

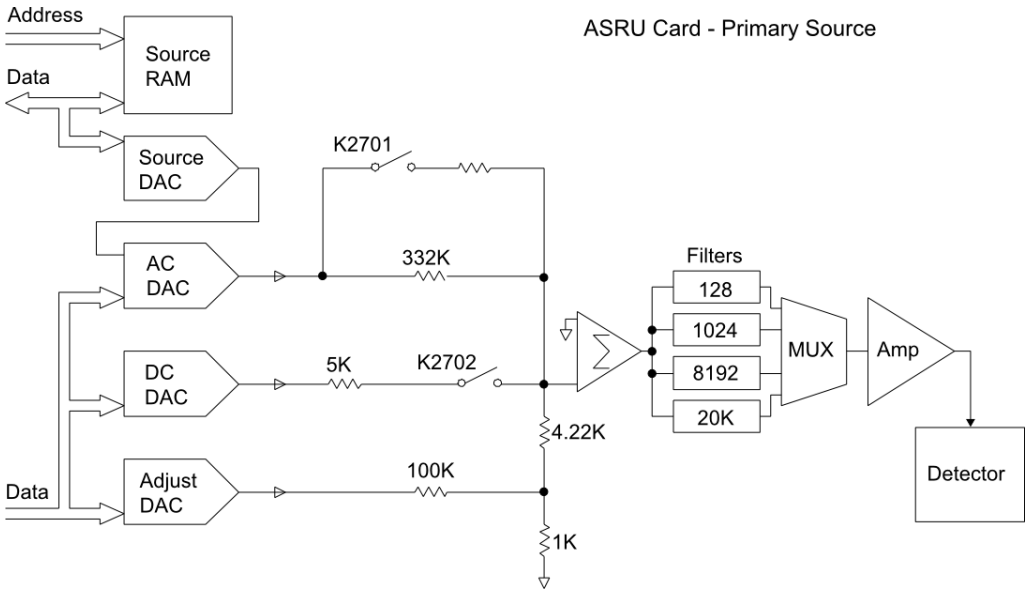
Primary DC Source

This test is a general check of the primary source at DC.

Subtests 0 through 7 test the DC DAC maximum and minimum DC output through four low-pass filters. All subsequent subtests use the 20-kHz filter.

Subtest 8 verifies that the DC DAC's output can be disconnected from the summing amplifier (by opening K2702). Subtests 9 and 10 test the maximum and minimum DC output using only the Adjust DAC. Subtest 11 measures the primary source output with the AC DAC programmed to about zero volts. Subtests 12 through 15 test maximum and minimum DC output using the AC DAC instead of the DC DAC (AC mode but with a DC waveform). Subtests 12 and 13 check the maximum and minimum output on the low range (with K2701 open). Subtests 14 and 15 verify the minimum and maximum output on the high range. Figure 4-3 shows the measurement path.

Figure 4-3 T2090



Test 2091

Primary DC Source Accuracy

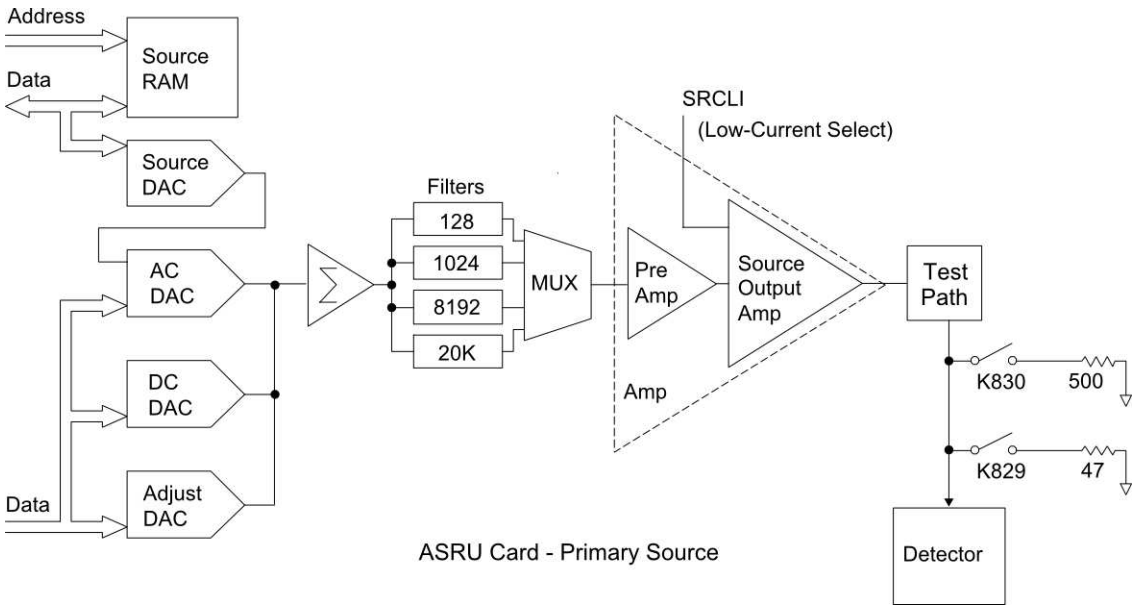
This test checks DC accuracy tests in high- and low-current modes, unloaded and loaded.

Subtests 0 through 6 test DC accuracy in high-current mode with no load at seven output voltages. Subtests 7 through 13 test DC accuracy in low-current mode with no load at the same seven voltages.

Subtests 14 and 15 use a 47-ohm resistor as a load (through K829), and run in the high-current mode. Subtest 14 uses -7.05 volts, and subtest 15 uses +7.05 volts. These voltages produce +150 or -150 milliamps into the supplied load.

Subtests 16 and 17 use a 500-ohm load resistor as a load (through K830), and run in the low-current mode. Subtest 16 runs at +10.0 volts and subtest 17 at -10.0 volts; the current delivered is +20 or -20 milliamps. Figure 4-4 shows the measurement path.

Figure 4-4 T2091



Test 2092

Primary DC Source Current Limit, Status, and Three-State

This test verifies the current limit circuitry, current limit status bit, and three-state current leakage of the primary source at DC.

High-current mode is tested first. Subtest 0 clears and reads the ASRU Card status register to verify that the current limit bit is cleared. Subtest 1 measures the current that is delivered into a 10-ohm load with 3.0 volts programmed. Subtest 2 reads the status register to prove the current limit bit was set.

Subtest 3 clears and reads the status register to verify the current-limit bit is cleared. Subtest 4 measures the current delivered into the 10-ohm load with -3.0 volts programmed. Subtest 5 reads the status register to prove that the current limit was set.

Now low-current mode is tested. Subtest 6 clears and reads the status register to verify that the current limit bit has been set. Subtests 7 and 8 check the positive and negative low current limit. Subtests 9 and 10 measure the three-state current leakage.

Test 2093

Fast Transition

This test verifies that the source will not go into current compliance with no load and fast output transitions.

AC Source and Detector

Test 2100

Primary AC Source, SCAT Chip, and Detector

This is a functional test of the primary source in AC mode, the SCAT (source control and timing) chip, and the detector.

The AC level accuracy is tested at three voltages and three frequencies. Subtests 0 through 2 are performed at 128 hertz with levels of 0.1 volts, 3.0 volts, and 7.0 volts rms. Subtests 3 through 5 run at 1024 hertz at the same levels. Subtests 6 through 8 run at 8192 hertz, again at 0.1 volts, 3.0 volts, and 7.0 volts. Subtest 9 runs at 8192 hertz with the 20-kilohertz filter.

Test 2101

Primary AC Source and Detector Quadrature Rejection

This test verifies the timing relationship between the primary source and detector, by measuring the imaginary component of a real waveform. Both positive and negative imaginary components are measured and subtracted to get rid of the DC component. The difference is halved to get the average quadrature value. Then, the ratio of the residual imaginary component to the amplitude of AC voltage is calculated in decibels.

Subtests 0 through 8 test nine ranges of the detector at 128 hertz. Subtests 9 through 17 repeat the test at the same nine ranges but at 1024 hertz. Subtests 18 through 26 run at 8192 hertz.

Test 2102

Primary AC Source and Detector DC Rejection

This test takes two AC readings 180 degrees out-of-phase, and subtracts them. The DC component should drop out and dividing the difference by two allows checking of DC rejection.

Subtests 0, 1, and 2 run at 128 hertz, 1024 hertz, and 8192 hertz, respectively.

MOA

Test 2120

MOA Compliance Voltage

This test verifies the MOA's voltage compliance function at 1.0 volt, 5.0 volts, and 10.0 volts. Both positive and negative inputs are checked.

Subtests 0 through 5 use a 1.0-volt compliance limit. With no stimulus to the MOA, subtest 0 clears the status register and reads the voltage compliance bit to verify it is not set. When the MOA is overdriven with a negative voltage, subtest 1 reads the compliance bit to prove that a voltage limit occurred. Subtest 2 reads the compliance voltage at the output of the MOA. Subtests 3 through 5 repeat for the positive voltage. Subtests 6 through 17 repeat the procedure using 5.0 and 10.0 volts.

Test 2121

MOA Current Limit and Status Register

This test verifies the MOA current limit function. Checks are performed at high and low current limits with positive and negative inputs.

Subtest 0 clears and reads the status register to prove the current limit bit is not set. Subtest 1 measures the current with a positive input at a level that should cause current limiting in the high-current mode. Subtest 2 reads the current limit bit to verify that it is set. Subtest 3 again clears and reads the status register to prove the current limit bit is reset. Subtest 4 measures the negative current that should cause current limiting in high-current mode, and subtest 5 reads the status register to show the current limit bit is set.

When low-current mode is set, subtest 6 clears and reads the status register to show the current limit bit is not set. Subtest 7 measures the output current with a positive input that should cause a current limit in the low-current mode. Subtest 8 measures the output current with a negative input.

Test 2122

MOA Offset Voltage

This test grounds both MOA inputs and sets the MOA gain to 1000. Subtest 0 measures the output voltage of the MOA. This voltage is 1000 V_{os}.

Test 2123

MOA Bias Current

This test configures the MOA so that any bias current will pass through the 1-megohm feedback resistor. Subtest 0 calculates the bias current by dividing the MOA output by one million.

Test 2124

MOA Noise

With the MOA inputs grounded, this test takes multiple MOA output readings at gains of 100 and 1000. The difference between the minimum and maximum reading is the MOA noise. Subtest 0 calculates the noise for a MOA gain of 100, and subtest 1 calculates the noise for a gain of 1000.

Test 2125

MOA Gain and Phase

The MOA is setup as an inverting amplifier driven by the source. Phase synchronous measurements are taken for real and imaginary components (for gain and phase) at three frequencies.

Subtests 0 through 5 calculate the gain and phase for 128 hertz, 1024 hertz, and 8192 hertz at narrow band. Subtests 6 through 11 repeat the calculations for wide band.

Auxiliary Source

Test 2250

Auxiliary Source Minimum and Maximum Output

This test programs the auxiliary source to maximum (positive) and minimum (negative) outputs. The detector reads these output voltages to ensure an acceptable programming range. Subtest 0 measures the minimum output; subtest 1 measures the maximum output.

Test 2251

Auxiliary Source Accuracy

The detector measures the auxiliary source voltage accuracy. Subtest 0 runs at +1.0 volts, subtest 1 at +4.0 volts, subtest 2 at +10.0 volts, subtest 3 at -1.0 volts, subtest 4 at -4.0 volts, and subtest 5 at -10.0 volts.

Test 2252

Auxiliary Source Current Limit, Three-State, and AUXDRV

This test checks the auxiliary source's current limit function, three-state leakage current, and preamp output (AUXDRV).

Subtest 0 clears and then reads the ASRU Card's status register to ensure that the current limit is cleared. The auxiliary source is set to high-current mode and then programmed to deliver 300 milliamps into 10 ohms. Subtest 1 reads the current delivered, and subtest 2 reads the status register to verify the current limit bit is set. Subtest 3 monitors the AUXDRV signal to verify it has railed.

Subtest 4 clears and then reads the status register to prove it can be cleared. A negative drive is applied, and subtest 5 measures AUXDRV again to verify that it went to the negative rail. Subtest 6 reads the status register to verify the current limit bit was set. Subtest 7 measures the current delivered. Subtest 8 clears and reads the status register to show current limiting can be cleared.

The test sets the low-current mode and the auxiliary source to deliver 40 milliamps into 100 ohms. Subtest 9 measures the current delivered. Subtest 10 repeats this with negative drive.

In subtests 11 and 12, the auxiliary source is three-stated and the leakage current is measured with +10.0 volts and -10.0 volts selected.

Probe

Test 2280

Probe AC Path and Propagation Delay

This test verifies the probe circuitry. Subtests 0, 2, and 3 check the GTH path, and subtests 1, 4, and 5 check the GTL path. Subtests 0 and 1 measure the frequency through each path; subtests 2 through 5 measure the propagation delay.

Test 2281

Probe Trip Point Accuracy, Threshold Noise, and Hysteresis

This test verifies the probe trip voltage accuracy, threshold noise and hysteresis. The source is Sets up to single step with triggers from the sequencer. The source output is routed to the probe tip and the GTH/GTL probe outputs are logged to the state capture ram. The sequencer causes the source to output a ramp of a small AC voltage on top of a large DC offset equal to the trip point. Then the state capture ram is examined to determine when the trip is occurred. Subtests 0 through 31 measure probe trip positive and negative levels, subtests 32 through 39 calculates threshold noise and subtests 40 through 43 calculate hysteresis.

Test 2283

Probe Relays and Resistor

This test verifies the probe relays and probe tip resistor (20k ohms) are working. Subtest 0 tests the probe tip resistor with K2202 closed. Subtest 1 verifies the K2202 can be opened. Subtest 2 again verifies the probe tip resistor and K2202. Subtest 3 verifies that K2201 can be opened. Subtest 4 verifies the probe tip resistor and K2202 again. Subtest 5 verifies that the probe tip relay K1 can be opened.

Test 2284

Probe Tip Through Fixture

Requires: Pin Verification Fixture and manual intervention

The operator holds the probe tip to one of the **lo** contacts on the fixture as prompted and then presses <return>. Subtest 0 verifies that the voltage drops to 0.0 volts. Test 2284 also checks the CALIB2 fixture interface pin.

MUX

Test 2310

Interconnect MUX Relays K852 and K853

This test checks interconnect MUX relays using DC level measurement. It verifies that the K852 and K853 relays both close and open. Subtest 0 checks that both relays close. Subtests 1 and 2 verify that K852 and K853 open.

Test 2311

Interconnect MUX Relays K854 and K855

This test verifies that K854 and K855 both close and open. Subtest 0 assures both relays close. Subtests 1 and 2 verify that K854 and K855 open.

Test 2312

SUBMUX Relays K748 and K761

Requires: Pin Verification Fixture

This test verifies that K748 and K761 both close and open by connecting the source through a resistor to ground with these relays and taking a voltage measurement to check the paths. Subtest 0 closes both relays; subtest 1 opens K748, and subtest 2 opens K761.

Test 2313

SUBMUX Relays K747 and K759

Requires: Pin Verification Fixture

This test verifies that K747 and K759 both close and open. Subtest 0 closes both relays. Subtests 1 and 2 verify that K747 and K759 open.

Test 2314

SUBMUX Relays K747 and K760

Requires: Pin Verification Fixture

This test verifies that K747 and K760 both close and open. Subtest 0 closes both relays. Subtests 1 and 2 verify that K747 and K760 open.

Test 2315

Relays K748 and K774 for ASRU-C

Requires: Pin Verification Fixture

This test is identical to Test 2312, except that K774 replaces K761.

This test verifies that K748 and K774 both close and open by connecting the ASRU source through a resistor to ground with these relays and taking a simple voltage measurement with the ASRU Detect module to check the paths.

Table 4-5 Test 2315 Subtests

Subtest	K748	K774
0	Closed	Closed
1	Open	Closed
2	Closed	Open

Test 2316

Relays K747 and K770 for ASRU-C

Requires: Pin Verification Fixture

This test verifies that the X7 bus relay K747 and B-bus relay K770 (Sout) can be closed and opened.

Table 4-6 Test 2316 Subtests

Subtest	K747	K770
0	Closed	Closed
1	Open	Closed
2	Closed	Open

Test 2317

Relays K747 and K771 for ASRU-C

Requires: Pin Verification Fixture

This test verifies that the X7 bus relay K747 and I-bus relay K771 (Iout) can be closed and opened. The test method is similar to that used in test 2312.

Table 4-7 Test 2317 Subtests

Subtest	K747	K771
0	Closed	Closed
1	Open	Closed
2	Closed	Open

Test 2318

Relays K747 and K772 for ASRU-C

Requires: Pin Verification Fixture

This test verifies that the X7 bus relay K747 and A-bus relay K772 (Aout) can be closed and opened.

Table 4-8 Test 2318 Subtests

Subtest	K747	K772
0	Closed	Closed
1	Open	Closed
2	Closed	Open

Test 2319

Relays K747 and K773 for ASRU-C

Requires: Pin Verification Fixture

This test verifies that the X7 bus relay K747 and B-bus relay K773 (Bout) can be closed and opened.

Table 4-9 Test 2319 Subtests

Subtest	K747	K773
0	Closed	Closed
1	Open	Closed
2	Closed	Open

Test 2320

X1-X8 Fixture Interface Pins with Probe

Requires: Manual intervention

This test checks the Fixture Interface Pins and relays for X1 thru X8 using the hand-held probe. This is needed for a TestJet subsystem which won't have any DUT power supplies and may not have a pin verification fixture. Otherwise X1-X6 are only checked during the DUT power supply tests.

Table 4-10 Test 2320 Subtests

Subtest	MUX Chanel Tested
0	X1
1	X2
2	X3
3	X4
4	X5
5	X6
6	X7
7	X8

DUT Power Supply

Test 2334

Check relays and fuses for High Current PS Channel 3

NOTE **This test is only for testing channel 3 with high-current power supply configuration.**

This test checks the additional relays and fuses added for DUT power supply channel 3 to support high current power supply up to 12 A. The components under this test are K1622, F1006, F1007, F1010 and F1011.

The DC 5 V from the DUT power supply is measured with the ASRU-N detector through different paths as listed below. In each pair of subtests, the first subtest checks whether one pair of switches in a relay can be closed and the fuse in the path is in working condition. The subsequent subtest opens the relay and takes the measurement again to make sure that the relay is not stuck.

- Subtests 0-1: K1607 through F1006
- Subtests 2-3: K1622 through F1010
- Subtests 4-5: K1607 through F1007
- Subtests 6-7: K1622 through F1011

Test 2335

Check relays and fuses for High Current PS Channel 4

NOTE **This test is only for testing channel 4 with high-current power supply configuration.**

This test checks the additional relays and fuses added for DUT power supply channel 4 to support high current power supply up to 12 A. The components under this test are K1623, F1008, F1009, F1012 and F1013.

The DC 5 V from the DUT power supply is measured with the ASRU-N detector through different paths as listed below. In each pair of subtests, the first subtest checks whether one pair of switches in a relay can be closed and the fuse in the path

is in working condition. The subsequent subtest opens the relay and takes the measurement again to make sure that the relay is not stuck.

- Subtests 0-1: K1610 through F1008
- Subtests 2-3: K1623 through F1012
- Subtests 4-5: K1610 through F1009
- Subtests 6-7: K1623 through F1013

Test 2340

DUT Power Supplies Ground Fault

Requires: Pin Verification Fixture and DUT power supplies

This test must pass before the other DUT power supply tests can run.

Each of the four outputs[1] on the DUT power supply are set to 10.0 volts with the current limit set to the minimum. Each DUT supply is measured while first one, then the other power lead is grounded. If any lead is shorted to ground, grounding the other lead will cause a current limit. If no leads are shorted to ground, no current limit will occur.

Subtest 0 measures the DUT power supply output 1 on the detector with the low lead grounded. Subtest 1 measures output 1 again, this time with the high lead grounded. Subtests 2 and 3 check DUT power supply output 2. Subtests 4 through 7 test DUT supply outputs 3 and 4.

1. Most Keysight systems have 6624A DUT power supplies. These have four separate 40-watt outputs. Some systems have 6621A DUT power supplies; these supplies have two 80-watt outputs. All the hardware in the path, except the power supplies themselves, is identical. This includes four sets of relays and four output cables. To handle the extra current, two sets of relays and two cables are used with each supply. For this reason the two-output 6621As appear to be four-output supplies.

Test 2341

DUT Power Supply Cables

Requires: Pin Verification Fixture and DUT power supplies

This test checks the DUT power supply outputs by delivering 2.0 volts into the supply leads, measurement path, and a 10-ohm resistor on the ASRU Card. Voltage drop measurements allow the calculation of current and lead resistances. Subtests 0 through 5 test DUT power supply output 1. Subtests 6 through 23 test the other three DUT supply outputs.

If test 2341 fails, check:

- MINT pins on the ASRU Card
- Connections on the rear of the DUT supply (tighten screws, solder crimped lugs)
- Plug connections on the rear of the DUT supply
- DUT supply relays on the ASRU Card.

Test 2342

DUT Power Supply Voltage Accuracy

Requires: Pin Verification Fixture and DUT power supplies

The outputs of the DUT power supplies are tested loaded and unloaded.

DUT power supply outputs 1 and 2 are tied together, as are the outputs of 3 and 4. One supply is tested while the other is used as its load. (The ASRU Card's relays will not handle the current needed to test these supplies.)

Subtest 0 tests power supply output 1 with no load; then subtest 1 tests supply output 1 using output 2 as a load. Subtests 2 and 3 test power supply output 2; subtest 3 uses output 1 to load output 2. Subtests 4 through 7 repeat the procedure for outputs 3 and 4.

Test 2343

Proper DUT Power Supply Connection to ASRU-C Card

Requires: Pin Verification Fixture and any of the following power supplies: 6621A, 6624A, 6634A, 6642A.

This test is only tests channels 5 and 6. It verifies that the power supplies are connected as specified in the system configuration All the data for channels 5 and 6 is found in the power supplies data array in the dgn config module.

First the test queries channels 5 and 6 to see if the proper power supply type is connected. Once that is verified, the power supply is programmed to output 5 volts on the proper channel and a voltage measurement taken in the ASRU-C Card to verify it is connected properly.

Table 4-11 Test 2343 Subtests

Subtests	Channel Tested
0-4	Channel 5
5-9	Channel 6

Test 2344

Additional Relays and Fuses for High Current PS Channels (ASRU-N Only)

NOTE This test is for the ASRU Revision N Card and requires either the E4033C PVF (for 2- or 4-module system) or E3771C PVF (for 1-module system).

This test checks the additional relays and fuses added for DUT power supply channel 3 and channel 4 to support high current power supply up to 12 A. The components under this test are K1622, K1623, F1006, F1007, F1008, F1009, F1010, F1011, F1012 and F1012.

The DC 5 V from the DUT power supply is measured with the detector through different paths as listed in Table 4-12. In each pair of subtests, the first subtest checks whether one pair of switches in a relay can be closed and the fuse in the path is in working condition. The next subtest opens the relay and takes the measurement again to make sure that the relay is not stuck.

Table 4-12 Test 2344 Subtests

Subtest	Target Component
Subtests 0-1	K1607 through F1006
Subtests 2-3	K1622 through F1010
Subtests 4-5	K1607 through F1007
Subtests 6-7	K1622 through F1011
Subtests 8-9	K1610 through F1008
Subtests 10-11	K1623 through F1012
Subtests 12-13	K1610 through F1009
Subtests 14-15	K1622 through F1013

Other Source and MOA

Test 2345

Source Output Resistors and MOA Feedback Resistors

This test verifies MOA source and feedback resistors.

Table 4-13 Test 2345 Subtests

Subtest	Tested Resistors
0	R801 and R812
1	R803, R804, and R822
2	R805 and R823
3	R805 and R824
4	R805 and R825
5	R806 and R808

Test 2346

Source Transformer

This test verifies the transformer that is used for SLIC testing and op-amp testing. Subtest 0 checks the transformer's 1:1 winding, and subtest 1 checks the 50:1 winding.

AutoAdjust Reference

Test 2347

AutoAdjust Reference Circuit Temperature

This test calculates the temperature circuit of the AutoAdjust reference circuit by measuring the circuit's output voltage. Subtest 0 converts the output to Celsius temperature.

Test 2348

AutoAdjust Reference Circuit Module Power Supplies

In this test, the detector uses the AutoAdjust reference circuit to measure the module power supplies' outputs. Each subtest tests a power supply.

Table 4-14 Test 2348 Subtests

Subtest	Power Supply	Expected Level
0	-10V pulser	-10.0 volts
1	+12V pulser	+12.0 volts
2	-10V	-10.0 volts
3	-20V	-20.0 volts
4	+20V	+20.0 volts
5	+12V	+12.0 volts
6	+5V	+5.0 volts

Test 2349

AutoAdjust Reference Voltages

This test measures (with the detector) the +10.0 volt and -10.0 volt references. Subtest 0 measures the +10.0 volt reference. Subtest 1 measures the -10.0 volt reference.

SCAT Clock

Test 2350

SCAT Clock Select

This test verifies the SCAT (Source Control and Timing) chip's clock select line. The detector makes two voltage measurements, one for each subtest. Subtest 0 uses the crystal as the clock, and subtest 1 uses the ADRV1 line. Since the ASRU Card's clock frequency is approximately twice that of ADRV1's, subtest 0's voltage measurement should be about half of subtest 1's measurement.

Test 2351

Trapped-charge relays and resistor

This test checks the trapped-charge bleed-off hardware. K826 connects the source; K816 connects I to G; K812 connects I the detector; K752 connects G to XG. Subtest 0 makes a measurement with the trapped charge relay K799 open. Subtest 1 makes a measurement with K799 closed. Subtest 2 closes K845 (10 ohms) and K755 (24.5 ohms). Subtest 3 opens K755 and closes K756 (5 ohms).

Test 2352

Trapped Charge Relays and Resistors

This test is identical to Test 2351 except it adds a test for the new 150-ohm trapped charge resistor. It verifies the operation of the trapped-charge bleed-off hardware.

Functional Port

Test 2500

Manual Intervention Prompt

Requires: Manual intervention

This test prompts the operator for functional port intervention.

Relays

Test 2702

DETHI Relay

This test verifies relays in the DETHI input path.

Table 4-15 Test 2702 Subtests

Subtest	Target relays and mode
0	K2302 and K2306 closed
1	K2302 opened
2	K2306 opened
3	K2310 and K2316 closed
4	K2310 opened
5	K2316 opened
6	K2304 closed
7	K2304 opened

Test 2703

DETLO Relay

This test verifies the relays in the DETLO input path.

Table 4-16 Test 2703 Subtests

Subtest	Target relays and mode
0	K2301 and K2305 closed
1	K2301 opened
2	K2305 opened
3	K2309 and K2315 closed
4	K2309 opened
5	K2315 opened
6	K2303 closed
7	K2303 opened

Test 2705

MOA Bandwidth Relay

This test checks the MOA bandwidth relays using AC voltage measurements. The subtests and their expected results are given below.

Table 4-17 Test 2705 Subtests

Subtest	K2601	K2604	Result
1	Closed	Open	10 Vrms
2	Open	Closed	1 Vrms

Test 2706

MOA Feedback Relay

This test verifies relay K2605, the MOA feedback relay. Subtest 0 checks the relay closed, and subtest 1 checks it open.

Test 2710

Interconnect MUX Relays

This test verifies interconnect MUX relays.

Table 4-18 Test 2710 Subtests

Subtest	Target relays and mode
0	K806 and K808 closed
1	K806 opened
2	K808 opened
3	K826 and K828 closed
4	K826 opened
5	K828 opened
6	K818 and K820 closed
7	K818 opened
8	K820 opened
9	K822 and K823 closed
10	K822 opened

Table 4-18 Test 2710 Subtests

Subtest	Target relays and mode
11	K823 opened
12	K813 and K837 closed
13	K813 opened
14	K837 opened

Test 2711

Interconnect MUX Relays

This test verifies additional interconnect MUX relays. The test order is (K801+K802), (K811+K812), (K824+K851), (K815+K843), (K819+K857), (K814), (K842), (K821+K822), (K827+K828), (K838), (K807+K808), and then (K804+K803).

Test 2712

Interconnect MUX Relays

This test verifies additional interconnect MUX relays.

Table 4-19 Test 2712 Subtests

Subtest	Target relay and mode
0	K856 closed
1	K856 opened
2	K816 closed
3	K816 opened
4	K844 closed
5	K844 opened

Test 2713

Interconnect MUX Relays

This test verifies additional interconnect MUX relays.

Table 4-20 Test 2713 Subtests

Subtest	Target relay and mode
0	K817 closed
1	K817 opened
2	K809 closed
3	K809 opened
4	K810 closed
5	K810 opened

Test 2714

Interconnect MUX Relays (ASRU-N Only)

This test verifies interconnect MUX relays in the ASRU Revision N Card. It is same as Test 2711 except that it adapts to the removal of K801, K802, K803 and K804 in the ASRU-N.

The test order is (K811+K812), (K824+K851), (K815+K843), (K819+K857), (K814), (K842), (K821+K822), (K827+K828), (K838), and then (K807+K808).

Test 2715 to Test 2719

SUBMUX Relays Closed Tests (ASRU-N Only)

Test 2715 to Test 2719 are same as Test 2720 to Test 2728 except that the test source voltage is adapted for the ASRU Revision N Card.

Test 2720

SUBMUX S-bus Relays Closed

This test verifies the closure of the SUBMUX relays that connect the S-bus to the analog buses X1 through X8.

Table 4-21 Test 2720 Subtests

Subtest	Target relay
0	K733 S-bus to X1
1	K734 S-bus to X2
2	K735 S-bus to X3
3	K736 S-bus to X4
4	K737 S-bus to X5
5	K738 S-bus to X6
6	K739 S-bus to X7
7	K740 S-bus to X8

Test 2722

SUBMUX I-Bus Relays Closed

This test verifies the closure of the SUBMUX relays that connect the I-bus to the analog buses X1 through X8.

Table 4-22 Test 2722 Subtests

Subtest	Target relay
0	K725 I-bus to X1
1	K726 I-bus to X2
2	K727 I-bus to X3
3	K728 I-bus to X4
4	K729 I-bus to X5
5	K730 I-bus to X6
6	K731 I-bus to X7
7	K732 I-bus to X8

Test 2724

SUBMUX L-Bus Relays Closed

This test verifies the closure of the SUBMUX relays that connect the L-bus to the analog buses X1 through X8.

Table 4-23 Test 2724 Subtests

Subtest	Target relay
0	K717 L-bus to X1
1	K718 L-bus to X2
2	K719 L-bus to X3
3	K720 L-bus to X4
4	K721 L-bus to X5
5	K722 L-bus to X6
6	K723 L-bus to X7
7	K724 L-bus to X8

Test 2726

SUBMUX A-bus Relays Closed

This test verifies the closure of the SUBMUX relays that connect the A-bus to the analog buses X1 through X8.

Table 4-24 Test 2726 Subtests

Subtest	Target relay
0	K709 A-bus to X1
1	K710 A-bus to X2
2	K711 A-bus to X3
3	K712 A-bus to X4
4	K713 A-bus to X5
5	K714 A-bus to X6
6	K715 A-bus to X7
7	K716 A-bus to X8

Test 2728

SUBMUX B-Bus Relays Closed

This test verifies the closure of the SUBMUX relays that connect the B-bus to the analog buses X1 through X8.

Table 4-25 Test 2728 Subtests

Subtest	Target relay
0	K701 B-bus to X1
1	K702 B-bus to X2
2	K703 B-bus to X3
3	K704 B-bus to X4
4	K705 B-bus to X5
5	K706 B-bus to X6
6	K707 B-bus to X7
7	K708 B-bus to X8

Test 2730

SUBMUX S-Bus Relays Opened

This test verifies that the SUBMUX relays that connect the S-bus to analog buses X1 through X8 can be opened.

Table 4-26 Test 2730 Subtests

Subtest	Target relay
0	K733 S-bus to X1
1	K734 S-bus to X2
2	K735 S-bus to X3
3	K736 S-bus to X4
4	K737 S-bus to X5
5	K738 S-bus to X6
6	K739 S-bus to X7
7	K740 S-bus to X8

Test 2732

SUBMUX I-Bus Relays Opened

This test verifies that the SUBMUX relays that connect the I-bus to analog buses X1 through X8 can be opened.

Table 4-27 Test 2732 Subtests

Subtest	Target relay
0	K725 I-bus to X1
1	K726 I-bus to X2
2	K727 I-bus to X3
3	K728 I-bus to X4
4	K729 I-bus to X5
5	K730 I-bus to X6
6	K731 I-bus to X7
7	K732 I-bus to X8

Test 2734

SUBMUX L-Bus Relays Opened

This test verifies that the SUBMUX relays that connect the L-bus to analog buses X1 through X8 can be opened.

Table 4-28 Test 2734 Subtests

Subtest	Target relay
0	K717 L-bus to X1
1	K718 L-bus to X2
2	K719 L-bus to X3
3	K720 L-bus to X4
4	K721 L-bus to X5
5	K722 L-bus to X6
6	K723 L-bus to X7
7	K724 L-bus to X8

Test 2736

SUBMUX A-Bus Relays Opened

This test verifies that the SUBMUX relays that connect the A-bus to analog buses X1 through X8 can be opened.

Table 4-29 Test 2736 Subtests

Subtest	Target relay
0	K709 A-bus to X1
1	K710 A-bus to X2
2	K711 A-bus to X3
3	K712 A-bus to X4
4	K713 A-bus to X5
5	K714 A-bus to X6
6	K715 A-bus to X7
7	K716 A-bus to X8

Test 2738

SUBMUX B-Bus Relays Opened

This test verifies that the SUBMUX relays that connect the B-bus to analog buses X1 through X8 can be opened.

Table 4-30 Test 2738 Subtests

Subtest	Target relay
0	K701 B-bus to X1
1	K702 B-bus to X2
2	K703 B-bus to X3
3	K704 B-bus to X4
4	K705 B-bus to X5
5	K706 B-bus to X6
6	K707 B-bus to X7
7	K708 B-bus to X8

Test 2741

SUBMUX Relays (K752, K762, and K764) and Functional Ports

Requires: Manual intervention

This test verifies the K752, K762, and K764 relays. Subtest 0 checks that all three relays close. Subtests 1, 2, and 3 verify that K752, K762, and K764 can open. Since the path requires a cable to be hooked to the functional ports, manual intervention is needed.

Test 2742

SUBMUX Relays (K751 and K754) and Functional Ports

Requires: Manual intervention

This test verifies the K751 and K754 relays. Subtests 0 and 1 check K751 closed and open, and subtests 2 and 3 check K754 closed and open. Since the path requires a cable to be hooked to the ports, manual intervention is needed.

Test 2743

SUBMUX relays (K757, K763, K758, and K765) and Functional Ports

Requires: Manual intervention

This test verifies two relay pairs K757 with K763 and K758 with K765. Since a cable must be connected to the functional ports, manual intervention is needed.

Table 4-31 Test 2743 Subtests

Subtest	Function
0	trigger out drive high to trigger in receiver
1	trigger out drive low to trigger in receiver
2	test K763 or K757 closed
3	test K763 or K757 closed
4	test K765 or K758 closed
5	test K765 or K758 closed
6	test K763 or K757 open
7	test K763 or K757 open
8	test K765 or K758 open
9	test K765 or K758 open

Test 2744

SUBMUX Miscellaneous Relays

This test verifies relays K749 and K753. Subtest 0 checks the closure of both relays; however, it cannot isolate a single relay failure. Subtest 1 checks that K749 can open, and subtest 2 checks that K753 can open.

Test 2745

Continuity of Functional Port Cables and Relays

Requires: Manual intervention

This test verifies the functional port cables and relays. Test 2745 prompts the operator to connect a BNC-female to BNC-female connector (a BNC tee works also) across the cable ends and then to press Return.

Test 2748

Interconnect MUX Relay and Debug Capacitor

This test verifies the K805 relay and the C801 debug capacitor. Subtest 0 checks that K805 opens; subtest 1 checks that K805 closes.

ASRU-N

NOTE The following tests are applicable only to the ASRU Revision N Card.

Test 2800

Check 5V Fixture Power Supply Accuracy (ASRU-N Only)

This test checks the accuracy of the 5 V fixture power supply on the ASRU Revision N Card.

Test 2801

Check 12V Fixture Power Supply Accuracy (ASRU-N Only)

This test checks the accuracy of the 12 V fixture power supply on the ASRU Revision N Card.

Test 2804

Check 70V compliance voltage and K912 relay (ASRU-N Only)

This test checks the accuracy of the 70 V compliance voltage in the zener diode measurement circuit. It confirms the status of supply to the zener amplifier, zener enable signal, zener voltage setting from auxiliary source, and zener amplifier circuits.

Test 2814

Test Interconnect MUX Relays (ASRU-N Only)

This test verifies interconnect MUX relays using level measurement.

Table 4-32 Test 2814 Subtests

Subtest	Target Relay	Mode
0	K922	closed
1	K922	opened
2	K919	closed
3	K919	opened
4	K923 and K925	closed
5	K923	opened
6	K925	opened
7	K916 and K917	closed
8	K916	opened
9	K917	opened
10	K926	closed
11	K926	opened
12	K915, 913	closed
13	K915	opened
14	K913	opened
15	K918	closed
16	K918	opened
17	K920	closed
18	K920	opened

Test 2818

Verify DMC Source Amplifier with ASRU Detector (ASRU-N Only)

This test checks the Digitized Measurement Circuit (DMC) source amplifier with the ASRU detector. It also tests the relays (K901, K903 and K924) on the DMC MOA source output line and DFT_SBUS.

Test 2820

Measure CALBUS for Each DMC PA Setting

This test measures DMC Calbus using the ASRU detector for each DMC Precision Attenuator (PA) setting.

Test 2822

Measure CALBUS with Each DMC Detector on All Ranges

This test uses the ASRU source to drive DMC Calbus which is then connected to the input of each of the four detectors (A, B, I and O) and measures DC voltages with each detector on all ranges.

Test 2824

Measures A, B and I Buses of DMC with Each DMC Detector

This test connects the ASRU source to the DFT_ABUS, DFT_BBUS and DFT_IBUS of DMC and uses the DMC A, B, and I detectors to measure the DC voltages. It also tests the relays K906 and K909 on DFT_ABUS, K908 and K910 on DFT_BBUS and K907 on DFT_IBUS.

Test 2828

Resistor Measurement with New DMC

This test checks resistor measurement with the ASRU-N's Digitized Measurement Circuit (DMC). The existing golden resistor (10k ohms) and feedback resistors (10 ohms, 100 ohms, 1K ohms, 10K ohms, 100K ohms and 1M ohms) are measured using the DMC.

Test 2830

Testing Power Monitoring Circuit (PMC)

This test checks the functionality of the three PMC channels in the ASRU Revision N Card.