HybridPlus and AnalogPlus Pin Card Tests

This chapter describes HybridPlus and AnalogPlus Pin Card Tests for i3070 Mux systems.
The HybridPlus and AnalogPlus Pin Card tests are numbered in the 3000s.
The Hybrid32 Pin Card tests are numbered in the 13000s.

NOTE

Page B is shown in all Confirmation and Diagnostic subtest tables for double-density cards.

Many of the relay test descriptions include tables that list the relays involved in each subtest. In the tables the relays being tested are in **bold** type.

To isolate relay failures on any Hybrid Card:

1. Run **Pin Card Relay Tests** from the System Diagnostics screen.
2. Run Diagnostics on a single failing Hybrid Card from the Module/Slot screen.
3. Run **Diagnose Relays** (F5) from the Test Execution screen.

KEYSIGHT TECHNOLOGIES

NOTE

Open Relay Tests verify that relays can be opened. If the MOA goes into compliance due to a shorted relay, the system will return the failure message:

```
-4.400000 L+1 ohms
```

This message does not represent a negative resistance, but a measurement error. Interpret this message as a shorted path.

NOTE

Confirmation tests are intended to quickly verify system functionality to the module/slot assembly level. To isolate individual field-replaceable relays, use the Diagnose Relays process in the *Module/Slot Troubleshooting Flowchart*.

Confirmation

Test 3011

Confirm Format Chips and Registers

This test checks the registers of the format chips on the HybridPlus Pin Card and then walks 1's and 0's through all the registers and memory.

Table 5-1

Subtest	Function
Page A	**Page A**
0a-193a	Reset format chip and check registers
194a-273a	Walk 1's through format chip registers
274a-353a	Walk 0's through format chip registers
354a-358a	Walk 1's through RAM
Page B	**Page B**
0b-193b	Reset format chip and check registers
194b-273b	Walk 1's through format chip registers
274b-353b	Walk 0's through format chip registers
354b-358b	Walk 1's through RAM

Test 3012

Confirm Double-Density Format Chips and Registers

Requires: Double-density pin card

This test is the double-density Series II card version of Test 3011 (E4000-66540 card).

This test checks the registers of the format chips on the double-density HybridPlus Pin Card and then walks 1's and 0's through all the registers and memory.

Test 3013

Confirm Double-Density Format Chips and Registers

Requires: Double-density pin card

This test is the double-density Series 3 card version of Test 3011 (E4000-66550 card).

This test checks the registers of the format chips on the double-density HybridPlus Pin Card and then walks 1's and 0's through all the registers and memory.

Test 3021

Confirm Relays can be Closed

This confirmation test verifies the closure of fixture interface (MINT) pin relays, KDCG, KDCL, KDC, X-bus, and XGL-bus relays.

Table 5-2

Subtest	Function
Page A	
0a-8a	Close K10A through K18A, K1A through K9A, KDC1, KX1, and KGLA
9a-17a	Close K10B through K18B, K1B through K9B, KDC2, KX2, and KGLB
18a-26a	Close K10C through K18C, K1C through K9C, KDC3, KX3, and KGLC
27a-35a	Close K10D through K18D, K1D through K9D, KDC4, KX4, and KGLD
36a-44a	Close K10E through K18E, K1E through K9E, KDC5, KX5, and KGLE
45a-53a	Close K10F through K18F, K1F through K9F, KDC6, KX6, and KGLF
54a-62a	Close K10G through K18G, K1G through K9G, KDC7, KX7, and KGLG

Table 5-2

Subtest	Function
Page B	
0b-8b	Close K10A through K18A, K1A through K9A, KDC1, KX1, and KGLA
9b-17b	Close K10B through K18B, K1B through K9B, KDC2, KX2, and KGLB
18b-26b	Close K10C through K18C, K1C through K9C, KDC3, KX3, and KGLC
27b-35b	Close K10D through K18D, K1D through K9D, KDC4, KX4, and KGLD
36b-44b	Close K10E through K18E, K1E through K9E, KDC5, KX5, and KGLE
45b-53b	Close K10F through K18F, K1F through K9F, KDC6, KX6, and KGLF
54b-62b	Close K10G through K18G, K1G through K9G, KDC7, KX7, and KGLG
63b-71b	Close K10H through K18H, K1H through K9H, KDC8, KX8, and KGLH
63b-71b	Close K10H through K18H, K1H through K9H, KDC8, KX8, and KGLH

Test 3022

Confirm Driver and Receiver Relays

This confirmation test verifies that the Pin Card driver and receiver channel relays (KR<a> and KD<a>) both close and open.

Table 5-3

Subtest	Function
Page A	
0a-15a	Measure pull-up receiver/driver level of KRA through KRH and KDA through KDH for closure check
16a-31a	Measure ground receiver/driver level of KRA through KRH and KDA through KDH for open check
Page B	
0b-15b	Measure pull-up receiver/driver level of KRA through KRH and KDA through KDH for closure check
16b-31b	Measure ground receiver/driver level of KRA through KRH and KDA through KDH for open check

Test 3023

Confirm Fixture Interface (MINT) Pins

Requires: Pin Verification Fixture

Test 3023 confirms that the Pin Card fixture interface (MINT) pins have good continuity.

Table 5-4

Subtest	Function
Page A	
0a	Measure path resistance for pins 1, 4, 25, 28, 49, 52, 73, 74
1a	Measure path resistance for pins 3, 6, 27, 30, 51, 54, 75, 76
2a	Measure path resistance for pins 5, 8, 29, 32, 53, 56, 77, 78
3a	Measure path resistance for pins 7, 10, 31, 34, 55, 58, 61, 62
4a	Measure path resistance for pins 9, 12, 33, 36, 57, 42, 63, 64
5a	Measure path resistance for pins 11, 14, 35, 38, 41, 44, 65, 66
6a	Measure path resistance for pins 13, 16, 37, 22, 43, 46, 67, 68
7a	Measure path resistance for pins 15, 18, 21, 24, 45, 48, 69, 70
8a	Measure path resistance for pins 17, 2, 23, 26, 47, 50, 71, 72
Page B	
0b	Measure path resistance for pins 1, 4, 25, 28, 49, 52, 73, 74
1b	Measure path resistance for pins 3, 6, 27, 30, 51, 54, 75, 76
2b	Measure path resistance for pins 5, 8, 29, 32, 53, 56, 77, 78
3b	Measure path resistance for pins 7, 10, 31, 34, 55, 58, 61, 62
4b	Measure path resistance for pins 9, 12, 33, 36, 57, 42, 63, 64
5b	Measure path resistance for pins 11, 14, 35, 38, 41, 44, 65, 66
6b	Measure path resistance for pins 13, 16, 37, 22, 43, 46, 67, 68
7b	Measure path resistance for pins 15, 18, 21, 24, 45, 48, 69, 70
8b	Measure path resistance for pins 17, 2, 23, 26, 47, 50, 71, 72

Test 3024

Confirm Relays Opened

This confirmation test verifies that the Pin Card relays can be opened.

Table 5-5

Subtest	Function
Page A	
0a-7a	Check receiver pin relays opened
8a-15a	Check driver pin relays opened
16a	Check X-bus relays opened
17a	Check X-bus disconnect relays opened
18a	Check XGL-bus relays opened
19a	Check XL-bus disconnect and XG-bus disconnect relays opened
Page B	
0b-7b	Check receiver pin relays opened
8b-15b	Check driver pin relays opened
16b	Check X-bus relays opened
17b	Check X-bus disconnect relays opened
18b	Check XGL-bus relays opened
19b	Check XL-bus disconnect and XG-bus disconnect relays opened

Test 3025

Confirm Ground Relays

Requires: Pin Verification Fixture

This confirmation test verifies that the ground relays can both open and close.

Table 5-6

Subtest	Function
Page A	
0a-5a	Check KGD1 through KGD6 closed
6a-11a	Check KGD1 through KGD6 opened
Page B	
0b-5b	Check KGD1 through KGD6 closed
6b-11b	Check KGD1 through KGD6 opened

Test 3031

Confirm Driver Levels

This confirmation test sets the drivers low to -2.0 volts and then measures the output to verify that the Pin Card driver levels are within tolerance.

Test 3032

Confirm Receiver Levels

This confirmation test verifies the accuracy of the Pin Card receiver levels. Subtests 0 through 7 correspond to receiver level calculations for channels A through H.

Test 3033

Confirm Driver and Receiver Timing

This confirmation test verifies that the Pin Card driver and receiver timing is accurate. Subtests 0 through 31 check driver timing, and subtests 32 through 47 check receiver timing.

Table 5-7

Subtest	Function
Page A	
0a-31a	Check driver timing
32a-39a	Check receiver timing
40a-47a	Check receiver timing using a different delay time
Page B	
0b-31b	Check driver timing
32b-39b	Check receiver timing
40b-47b	Check receiver timing using a different delay time

Test 3034

Confirm Driver and Receiver at Speed

This confirmation test verifies that the Pin Card drivers and receivers operate at 6.25 MHz.

Table 5-8

Subtest	Function
Page A	
0a, 2a, 4a, 6a 8a, 10a, 12a, 14a	Check sequencer status
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure driver frequency of DCHA through DCHH
Page B	
0b, 2b, 4b, 6b 8b, 10b, 12b, 14b	Check sequencer status
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure driver frequency of DCHA through DCHH

Test 3035

Confirm Driver and Receiver Data Capture

This confirmation test verifies that the Pin Card driver and receiver data handling is working.

Table 5-9

Subtest	Function
Page A	
0a	Check sequencer status with enable pull-down
1a-8a	Check fail log data with enable pull-down
9a	Check sequencer status with enable pull-up
10a-1a7	Check fail log data with enable pull-up
18a	Check sequencer status with NOP
19a-26a	Check fail log data with NOP
27a-34a	Check hold register and state capture RAM pointer before sequencer run
35a-42a	▪ Check hold register and state capture RAM pointer after sequencer run 43-554 ▪ Check state capture RAM content for all channels
555a-556a	Check sequencer and card status, drive 1 and 0 both pass
557a-564a	Check fail log flag, 1 and 0 both pass
565a-566a	Check sequencer and card status, drive 1 fail
567a-574a	Check fail log flag, 1 fail
575-576	Check sequencer and card status, drive 0 fail
577a-584a	Check fail log flag, 0 fail
Page B	
0b	Check sequencer status with enable pull-down
1b-8b	Check fail log data with enable pull-down
9b	Check sequencer status with enable pull-up
10b-1b7	Check fail log data with enable pull-up
18b	Check sequencer status with NOP
19b-26b	Check fail log data with NOP
27b-34b	Check hold register and state capture RAM pointer before sequencer run

Table 5-9

Subtest	Function
35b-42b	▪ Check hold register and state capture RAM pointer after sequencer run 43-554 ▪ Check state capture RAM content for all channels
555b-556b	Check sequencer and card status, drive 1 and 0 both pass
557b-564b	Check fail log flag, 1 and 0 both pass
565b-566b	Check sequencer and card status, drive 1 fail
567b-574b	Check fail log flag, 1 fail
575-576	Check sequencer and card status, drive 0 fail
577b-584b	Check fail log flag, 0 fail

Card Communication

Test 3110

Check for Reset and Initialization for Pin Card

- Toggles the bit in the MAC (control card) reset register for motherboard reset.
- Reset Format chip by writing 0 and then 31 to FC reset registers (Channel 0 through 7).
- Check Format chip's registers reset status.

1	Check Vector Period Select Register	(subtest 0 - 3)
2	Check Driver Output Control Register (Channel 0/1)	(subtest 4 - 11)
3	Check Receiver Control Register (Channel 0/1)	(subtest 12 - 19)
4	Check Fail Log Register (Channel 0/1)	(subtest 20 - 27)
5	Check CRC Register (Low/High)	(subtest 28 - 35)
6	Check Response Storage Hold register	(subtest 36 - 39)
7	Check Response Storage Pointer	(subtest 40 - 43)
8	Check Driver/Receiver Delay Line Clock Select	(subtest 44 - 51)
9	Check Asymmetry Control Register	(subtest 52 - 55)
10	Check Reset Register	(subtest 56 - 59)
11	Check Over power and over current bits	(subtest 60)
12	Read PIN card status register	(subtest 61)

- Initialize PIN card (Set Driver/Receiver reference levels to the TTL level, driver current limit and driver slew rate).

1	Check that all relays are opened	(subtest 62 - 73)
2	Check registers' reset status	
	– Driver/Receiver Delay Line Clock Select Register	(subtest 74 - 81)
	– Vector Period Select Register/Driver	(subtest 82 - 85)
	– Output Control Register (Channel 0/1)	(subtest 86 - 93)
	– Receiver Control Register (Channel 0/1)	(subtest 94 - 101)
3	Read VGER RAM contents to check TTL levels set	
	– For Receiver channels 0 to 7 (for High/Low)	(subtest 102 - 117)
	– For Driver channels 0 to 7 (for High/Low)	(subtest 118 - 133)
4	Read VGER RAM contents to check drivers' current limit 500 mA (channels 0 to 7)	(subtest 134 - 141)
5	Read VGER RAM contents to check drivers' slew rate 175 V/usec (channels 0 to 7)	(subtest142 - 149)
6	Check Fail log register	(subtest 150 - 157)
7	Check Driver delay setup (150 ns - 170 ns)	(subtest 158 - 173)
8	Check Receiver delay setup (150 ns - 170 ns)	(subtest 174 - 189)
9	Check asymmetry register	(subtest190 - 193)

Test 3111

Reset and Initialize Double-Density HybridPlus Pin Card

Requires: Series II double-density pin card

This test is the same as Test 3110, but for the Series II double-density card.

Test 3112

Reset and Initialize Double-Density HybridPlus Pin Card

Requires: Series 3 double-density pin card

This test is the same as Test 3110, but for the Series 3 double-density card.

Test 3140 and Test 3150

Walk 1's and 0's Through Registers

Subtests 0a through 79a walk 1's and 0's through the various cells of side A of the Pin Card. Subtests 0b through 79b walk 1's and 0's through the various cells of side B of the Pin Card.

Test 3160

Walk 1's Through RAM

This test walks 1's through the Pin Card RAM.

Table 5-10

Subtest	Function
Page A	
0a-2a	Walk 1's through Pin Card RAM, banks A through C
3a	Walk 1's through voltage generator RAM
4a	Walk 1's through state capture RAM
Page B	
0b-2b	Walk 1's through Pin Card RAM, banks A through C
3b	Walk 1's through voltage generator RAM
4b	Walk 1's through state capture RAM

Test 3161

Check Vector Addresses 14 and 15 on the Double-Density Pin Card

Requires: Double-density pin card

This tests the vector address bits 14 and 15.

Test 3170

Verify Read/Write of Format Chip Registers

This test was written because a defective format chip was found to have a register over-writing problem. To test for this problem a unique read/write pattern is used. Failure of any subtest indicates a faulty format chip is present.

Test 3180

AnalogPlus Pin Card Registers

This test verifies the card ID register and relay drivers for the AnalogPlus Pin Card.

Closed Relay

Test 3210

Test Sets of Reciever to X-bus, X-bus Disconnect, and Driver to XGL-Bus Relays can be Closed

This test verifies sets of KDC, KX, and KGL relays can be closed. A test failure is caused when either relay in a set being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

NOTE This test does not isolate individual relays. Other relay diagnostic tests isolate these individual relays.

Figure 5-1 shows the measurement path.

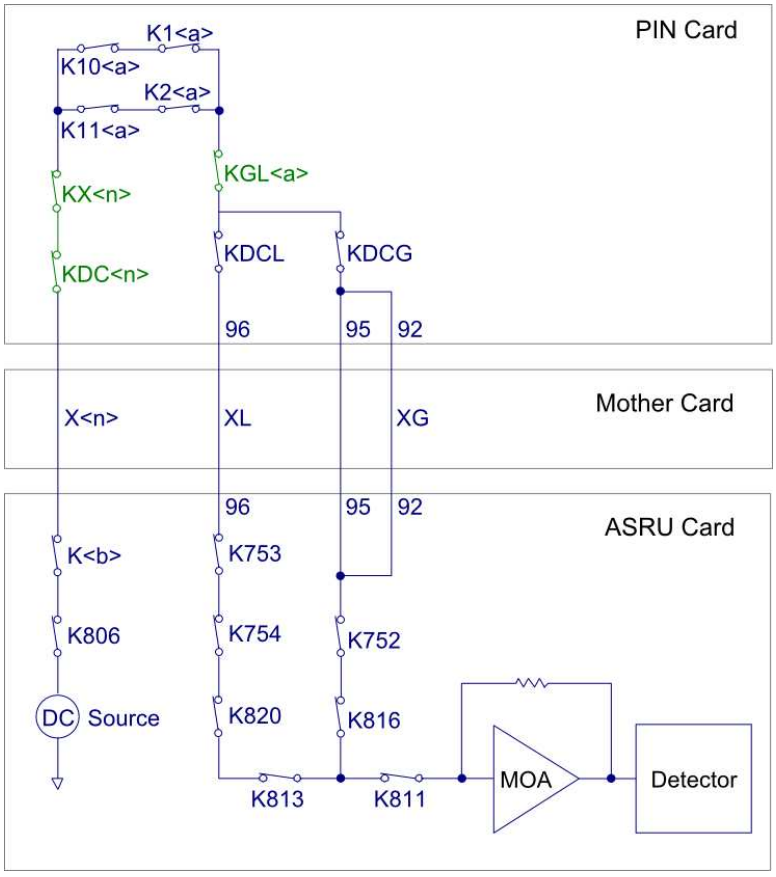
Table 5-11

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	KGL<a>
Page A									
0a	K733	X1	**KDC1**	**KX1**	K1A	K2A	K10A	K11A	**KGLA**
1a	K734	X2	**KDC2**	**KX2**	K1B	K2B	K10B	K11B	**KGLB**
2a	K735	X3	**KDC3**	**KX3**	K1C	K2C	K10C	K11C	**KGLC**
3a	K736	X4	**KDC4**	**KX4**	K1D	K2D	K10D	K11D	**KGLD**
4a	K737	X5	**KDC5**	**KX5**	K1E	K2E	K10E	K11E	**KGLE**
5a	K738	X6	**KDC6**	**KX6**	K1F	K2F	K10F	K11F	**KGLF**
6a	K739	X7	**KDC7**	**KX7**	K1G	K2G	K10G	K11G	**KGLG**
7a	K740	X8	**KDC8**	**KX8**	K1H	K2H	K10H	K11H	**KGLH**

Table 5-11

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	KGL<a>
Page B									
0b	K733	X1	**KDC1**	**KX1**	K1A	K2A	K10A	K11A	**KGLA**
1b	K734	X2	**KDC2**	**KX2**	K1B	K2B	K10B	K11B	**KGLB**
2b	K735	X3	**KDC3**	**KX3**	K1C	K2C	K10C	K11C	**KGLC**
3b	K736	X4	**KDC4**	**KX4**	K1D	K2D	K10D	K11D	**KGLD**
4b	K737	X5	**KDC5**	**KX5**	K1E	K2E	K10E	K11E	**KGLE**
5b	K738	X6	**KDC6**	**KX6**	K1F	K2F	K10F	K11F	**KGLF**
6b	K739	X7	**KDC7**	**KX7**	K1G	K2G	K10G	K11G	**KGLG**
7b	K740	X8	**KDC8**	**KX8**	K1H	K2H	K10H	K11H	**KGLH**

Figure 5-1 T3210



Test 3230

Test Relays KDCG and KDCL Closed

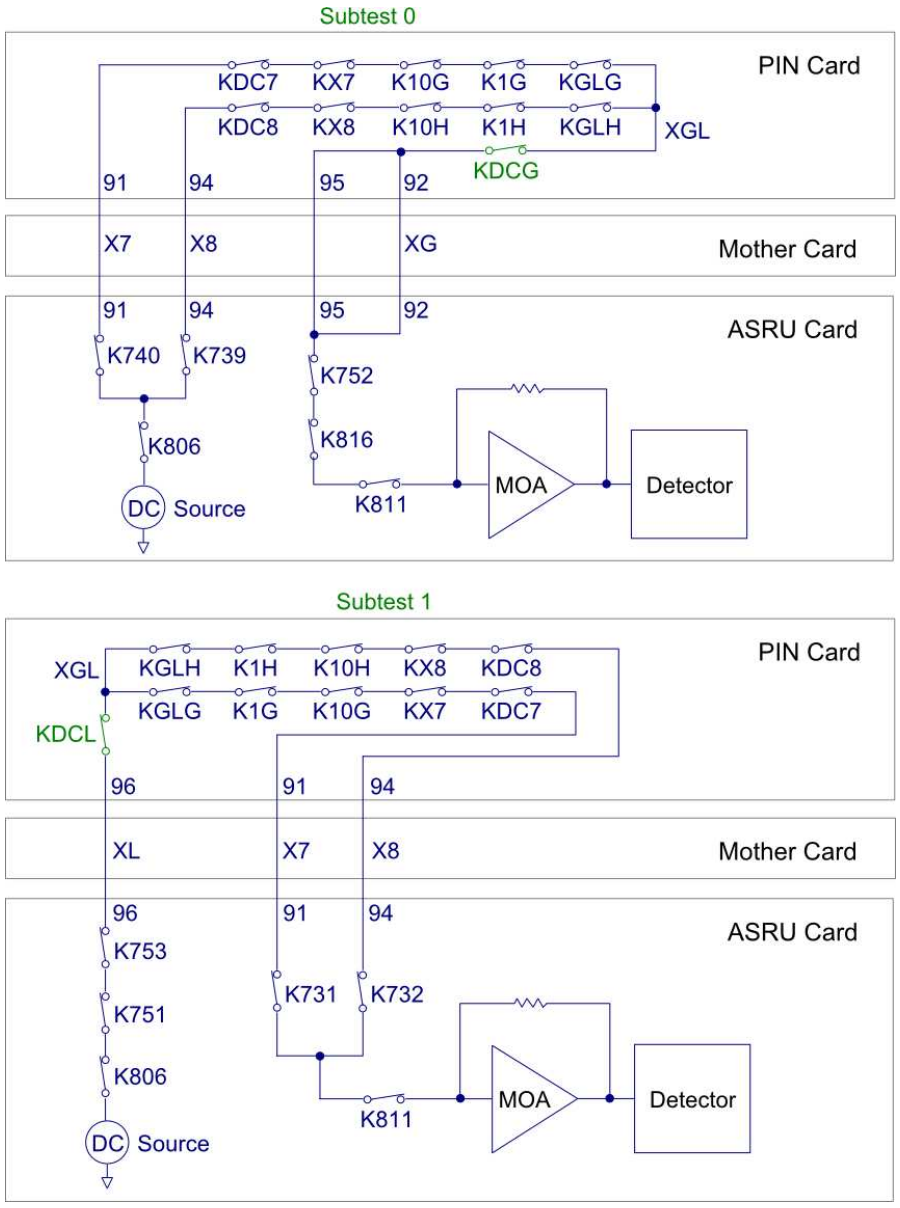
This test verifies KDCG and KDCL relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

Figure 5-2 shows the measurement paths.

Table 5-12

Subtest	KDC<n>	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
Page A											
0a	**KDCG**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
1a	**KDCL**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
Page B											
0b	**KDCG**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
1b	**KDCL**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH

Figure 5-2 T3230



Test 3240

Test Pairs of Driver and Receiver to Fixture Interface (MINT) Pin (MUX) Relays can be Closed

This test verifies pairs of fixture interface pin relays can be closed. A test failure is caused when either relay in the pair being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

Test 3240 requires the proper operation of KDC, KX, and KGL relays.

Since test 3240 cannot isolate single relay failures, we recommend running tests 3974 and 3975 which require the Pin Verification Fixture.

Figure 5-3 shows the measurement path.

Table 5-13

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K<r>	K<d>	KGL<a>
Page A							
0a	K733	X1	KDC1	KX1	**K10A**	**K1A**	KGLA
1a	K733	X1	KDC1	KX1	**K11A**	**K2A**	KGLA
2a	K733	X1	KDC1	KX1	**K12A**	**K3A**	KGLA
3a	K733	X1	KDC1	KX1	**K13A**	**K4A**	KGLA
4a	K733	X1	KDC1	KX1	**K14A**	**K5A**	KGLA
5a	K733	X1	KDC1	KX1	**K15A**	**K6A**	KGLA
6a	K733	X1	KDC1	KX1	**K16A**	**K7A**	KGLA
7a	K733	X1	KDC1	KX1	**K17A**	**K8A**	KGLA
8a	K733	X1	KDC1	KX1	**K18A**	**K9A**	KGLA
9a	K734	X2	KDC2	KX2	**K10B**	**K1B**	KGLB
10a	K734	X2	KDC2	KX2	**K11B**	**K2B**	KGLB
11a	K734	X2	KDC2	KX2	**K12B**	**K3B**	KGLB
12a	K734	X2	KDC2	KX2	**K13B**	**K4B**	KGLB
13a	K734	X2	KDC2	KX2	**K14B**	**K5B**	KGLB
14a	K734	X2	KDC2	KX2	**K15B**	**K6B**	KGLB
15a	K734	X2	KDC2	KX2	**K16B**	**K7B**	KGLB
16a	K734	X2	KDC2	KX2	**K17B**	**K8B**	KGLB
17a	K734	X2	KDC2	KX2	**K18B**	**K9B**	KGLB
18a	K735	X3	KDC3	KX3	**K10C**	**K1C**	KGLC
19a	K735	X3	KDC3	KX3	**K11C**	**K2C**	KGLC
20a	K735	X3	KDC3	KX3	**K12C**	**K3C**	KGLC
21a	K735	X3	KDC3	KX3	**K13C**	**K4C**	KGLC
22a	K735	X3	KDC3	KX3	**K14C**	**K5C**	KGLC
23a	K735	X3	KDC3	KX3	**K15C**	**K6C**	KGLC
24a	K735	X3	KDC3	KX3	**K16C**	**K7C**	KGLC
25a	K735	X3	KDC3	KX3	**K17C**	**K8C**	KGLC

Table 5-13

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K<r>	K<d>	KGL<a>
26a	K735	X3	KDC3	KX3	**K18C**	**K9C**	KGLC
27a	K736	X4	KDC4	KX4	**K10D**	**K1D**	KGLD
28a	K736	X4	KDC4	KX4	**K11D**	**K2D**	KGLD
29a	K736	X4	KDC4	KX4	**K12D**	**K3D**	KGLD
30a	K736	X4	KDC4	KX4	**K13D**	**K4D**	KGLD
31a	K736	X4	KDC4	KX4	**K14D**	**K5D**	KGLD
32a	K736	X4	KDC4	KX4	**K15D**	**K6D**	KGLD
33a	K736	X4	KDC4	KX4	**K16D**	**K7D**	KGLD
34a	K736	X4	KDC4	KX4	**K17D**	**K8D**	KGLD
35a	K736	X4	KDC4	KX4	**K18D**	**K9D**	KGLD
36a	K737	X5	KDC5	KX5	**K10E**	**K1E**	KGLE
37a	K737	X5	KDC5	KX5	**K11E**	**K2E**	KGLE
38a	K737	X5	KDC5	KX5	**K12E**	**K3E**	KGLE
39a	K737	X5	KDC5	KX5	**K13E**	**K4E**	KGLE
40a	K737	X5	KDC5	KX5	**K14E**	**K5E**	KGLE
41a	K737	X5	KDC5	KX5	**K15E**	**K6E**	KGLE
42a	K737	X5	KDC5	KX5	**K16E**	**K7E**	KGLE
43a	K737	X5	KDC5	KX5	**K17E**	**K8E**	KGLE
44a	K737	X5	KDC5	KX5	**K18E**	**K9E**	KGLE
45a	K738	X6	KDC6	KX6	**K10F**	**K1F**	KGLF
46a	K738	X6	KDC6	KX6	**K11F**	**K2F**	KGLF
47a	K738	X6	KDC6	KX6	**K12F**	**K3F**	KGLF
48a	K738	X6	KDC6	KX6	**K13F**	**K4F**	KGLF
49a	K738	X6	KDC6	KX6	**K14F**	**K5F**	KGLF
50a	K738	X6	KDC6	KX6	**K15F**	**K6F**	KGLF
51a	K738	X6	KDC6	KX6	**K16F**	**K7F**	KGLF
52a	K738	X6	KDC6	KX6	**K17F**	**K8F**	KGLF
53a	K738	X6	KDC6	KX6	**K18F**	**K9F**	KGLF
54a	K739	X7	KDC7	KX7	**K10G**	**K1G**	KGLG
55a	K739	X7	KDC7	KX7	**K11G**	**K2G**	KGLG

Table 5-13

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K<r>	K<d>	KGL<a>
56a	K739	X7	KDC7	KX7	**K12G**	**K3G**	KGLG
57a	K739	X7	KDC7	KX7	**K13G**	**K4G**	KGLG
58a	K739	X7	KDC7	KX7	**K14G**	**K5G**	KGLG
59a	K739	X7	KDC7	KX7	**K15G**	**K6G**	KGLG
60a	K739	X7	KDC7	KX7	**K16G**	**K7G**	KGLG
61a	K739	X7	KDC7	KX7	**K17G**	**K8G**	KGLG
62a	K739	X7	KDC7	KX7	**K18G**	**K9G**	KGLG
63a	K740	X8	KDC8	KX8	**K10H**	**K1H**	KGLH
64a	K740	X8	KDC8	KX8	**K11H**	**K2H**	KGLH
65a	K740	X8	KDC8	KX8	**K12H**	**K3H**	KGLH
66a	K740	X8	KDC8	KX8	**K13H**	**K4H**	KGLH
67a	K740	X8	KDC8	KX8	**K14H**	**K5H**	KGLH
68a	K740	X8	KDC8	KX8	**K15H**	**K6H**	KGLH
69a	K740	X8	KDC8	KX8	**K16H**	**K7H**	KGLH
70a	K740	X8	KDC8	KX8	**K17H**	**K8H**	KGLH
71a	K740	X8	KDC8	KX8	**K18H**	**K9H**	KGLH
Page B							
0b	K733	X1	KDC1	KX1	**K10A**	**K1A**	KGLA
1b	K733	X1	KDC1	KX1	**K11A**	**K2A**	KGLA
2b	K733	X1	KDC1	KX1	**K12A**	**K3A**	KGLA
3b	K733	X1	KDC1	KX1	**K13A**	**K4A**	KGLA
4b	K733	X1	KDC1	KX1	**K14A**	**K5A**	KGLA
5b	K733	X1	KDC1	KX1	**K15A**	**K6A**	KGLA
6b	K733	X1	KDC1	KX1	**K16A**	**K7A**	KGLA
7b	K733	X1	KDC1	KX1	**K17A**	**K8A**	KGLA
8b	K733	X1	KDC1	KX1	**K18A**	**K9A**	KGLA
9b	K734	X2	KDC2	KX2	**K10B**	**K1B**	KGLB
10b	K734	X2	KDC2	KX2	**K11B**	**K2B**	KGLB
11b	K734	X2	KDC2	KX2	**K12B**	**K3B**	KGLB
12b	K734	X2	KDC2	KX2	**K13B**	**K4B**	KGLB

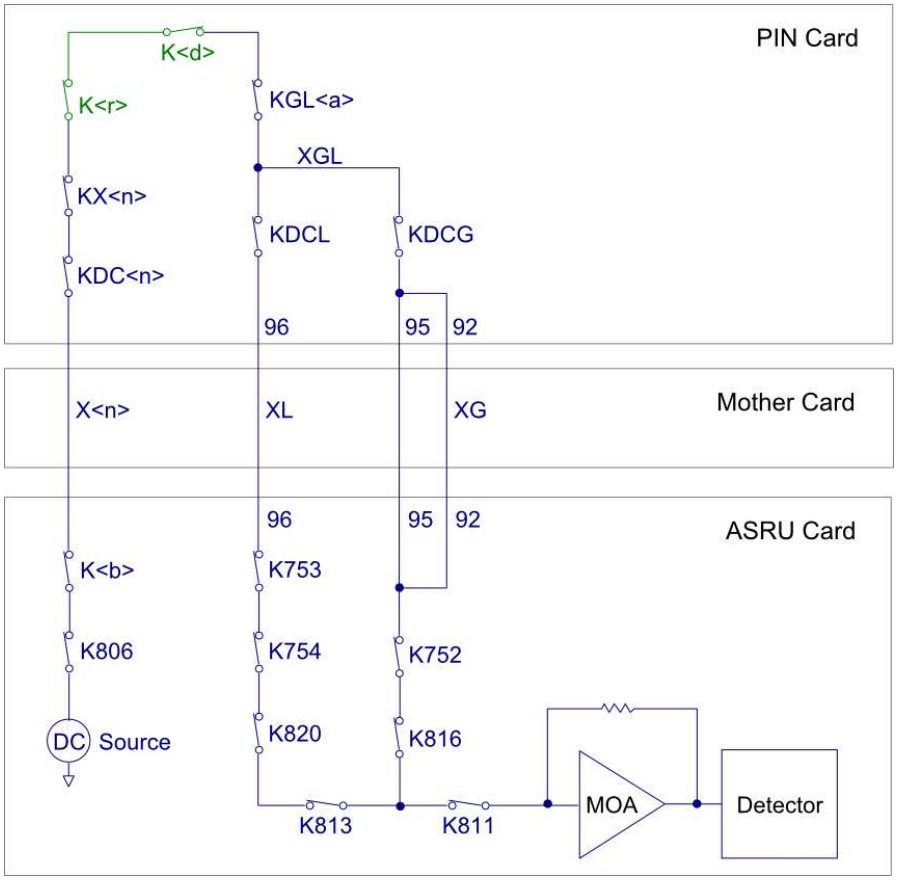
Table 5-13

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K<r>	K<d>	KGL<a>
13b	K734	X2	KDC2	KX2	**K14B**	**K5B**	KGLB
14b	K734	X2	KDC2	KX2	**K15B**	**K6B**	KGLB
15b	K734	X2	KDC2	KX2	**K16B**	**K7B**	KGLB
16b	K734	X2	KDC2	KX2	**K17B**	**K8B**	KGLB
17b	K734	X2	KDC2	KX2	**K18B**	**K9B**	KGLB
18b	K735	X3	KDC3	KX3	**K10C**	**K1C**	KGLC
19b	K735	X3	KDC3	KX3	**K11C**	**K2C**	KGLC
20b	K735	X3	KDC3	KX3	**K12C**	**K3C**	KGLC
21b	K735	X3	KDC3	KX3	**K13C**	**K4C**	KGLC
22b	K735	X3	KDC3	KX3	**K14C**	**K5C**	KGLC
23b	K735	X3	KDC3	KX3	**K15C**	**K6C**	KGLC
24b	K735	X3	KDC3	KX3	**K16C**	**K7C**	KGLC
25b	K735	X3	KDC3	KX3	**K17C**	**K8C**	KGLC
26b	K735	X3	KDC3	KX3	**K18C**	**K9C**	KGLC
27b	K736	X4	KDC4	KX4	**K10D**	**K1D**	KGLD
28b	K736	X4	KDC4	KX4	**K11D**	**K2D**	KGLD
29b	K736	X4	KDC4	KX4	**K12D**	**K3D**	KGLD
30b	K736	X4	KDC4	KX4	**K13D**	**K4D**	KGLD
31b	K736	X4	KDC4	KX4	**K14D**	**K5D**	KGLD
32b	K736	X4	KDC4	KX4	**K15D**	**K6D**	KGLD
33b	K736	X4	KDC4	KX4	**K16D**	**K7D**	KGLD
34b	K736	X4	KDC4	KX4	**K17D**	**K8D**	KGLD
35b	K736	X4	KDC4	KX4	**K18D**	**K9D**	KGLD
36b	K737	X5	KDC5	KX5	**K10E**	**K1E**	KGLE
37b	K737	X5	KDC5	KX5	**K11E**	**K2E**	KGLE
38b	K737	X5	KDC5	KX5	**K12E**	**K3E**	KGLE
39b	K737	X5	KDC5	KX5	**K13E**	**K4E**	KGLE
40b	K737	X5	KDC5	KX5	**K14E**	**K5E**	KGLE
41b	K737	X5	KDC5	KX5	**K15E**	**K6E**	KGLE
42b	K737	X5	KDC5	KX5	**K16E**	**K7E**	KGLE

Table 5-13

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K<r>	K<d>	KGL<a>
43b	K737	X5	KDC5	KX5	**K17E**	**K8E**	KGLE
44b	K737	X5	KDC5	KX5	**K18E**	**K9E**	KGLE
45b	K738	X6	KDC6	KX6	**K10F**	**K1F**	KGLF
46b	K738	X6	KDC6	KX6	**K11F**	**K2F**	KGLF
47b	K738	X6	KDC6	KX6	**K12F**	**K3F**	KGLF
48b	K738	X6	KDC6	KX6	**K13F**	**K4F**	KGLF
49b	K738	X6	KDC6	KX6	**K14F**	**K5F**	KGLF
50b	K738	X6	KDC6	KX6	**K15F**	**K6F**	KGLF
51b	K738	X6	KDC6	KX6	**K16F**	**K7F**	KGLF
52b	K738	X6	KDC6	KX6	**K17F**	**K8F**	KGLF
53b	K738	X6	KDC6	KX6	**K18F**	**K9F**	KGLF
54b	K739	X7	KDC7	KX7	**K10G**	**K1G**	KGLG
55b	K739	X7	KDC7	KX7	**K11G**	**K2G**	KGLG
56b	K739	X7	KDC7	KX7	**K12G**	**K3G**	KGLG
57b	K739	X7	KDC7	KX7	**K13G**	**K4G**	KGLG
58b	K739	X7	KDC7	KX7	**K14G**	**K5G**	KGLG
59b	K739	X7	KDC7	KX7	**K15G**	**K6G**	KGLG
60b	K739	X7	KDC7	KX7	**K16G**	**K7G**	KGLG
61b	K739	X7	KDC7	KX7	**K17G**	**K8G**	KGLG
62b	K739	X7	KDC7	KX7	**K18G**	**K9G**	KGLG
63b	K740	X8	KDC8	KX8	**K10H**	**K1H**	KGLH
64b	K740	X8	KDC8	KX8	**K11H**	**K2H**	KGLH
65b	K740	X8	KDC8	KX8	**K12H**	**K3H**	KGLH
66b	K740	X8	KDC8	KX8	**K13H**	**K4H**	KGLH
67b	K740	X8	KDC8	KX8	**K14H**	**K5H**	KGLH
68b	K740	X8	KDC8	KX8	**K15H**	**K6H**	KGLH
69b	K740	X8	KDC8	KX8	**K16H**	**K7H**	KGLH
70b	K740	X8	KDC8	KX8	**K17H**	**K8H**	KGLH
71b	K740	X8	KDC8	KX8	**K18H**	**K9H**	KGLH

Figure 5-3 T3240



Test 3260

Test Receiver Channel Relays can be Closed

This test verifies the KRA through KRH relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

Test 3260 sets the receiver references (RHI and RLO) to +2.0 and -2.0 volts, enables the receiver's pull-up, closes the relay, and then measures the receiver's input level. A 10 kohm path to ground ensures the test will fail if the path is open; it eliminates the possibility of a drift value.

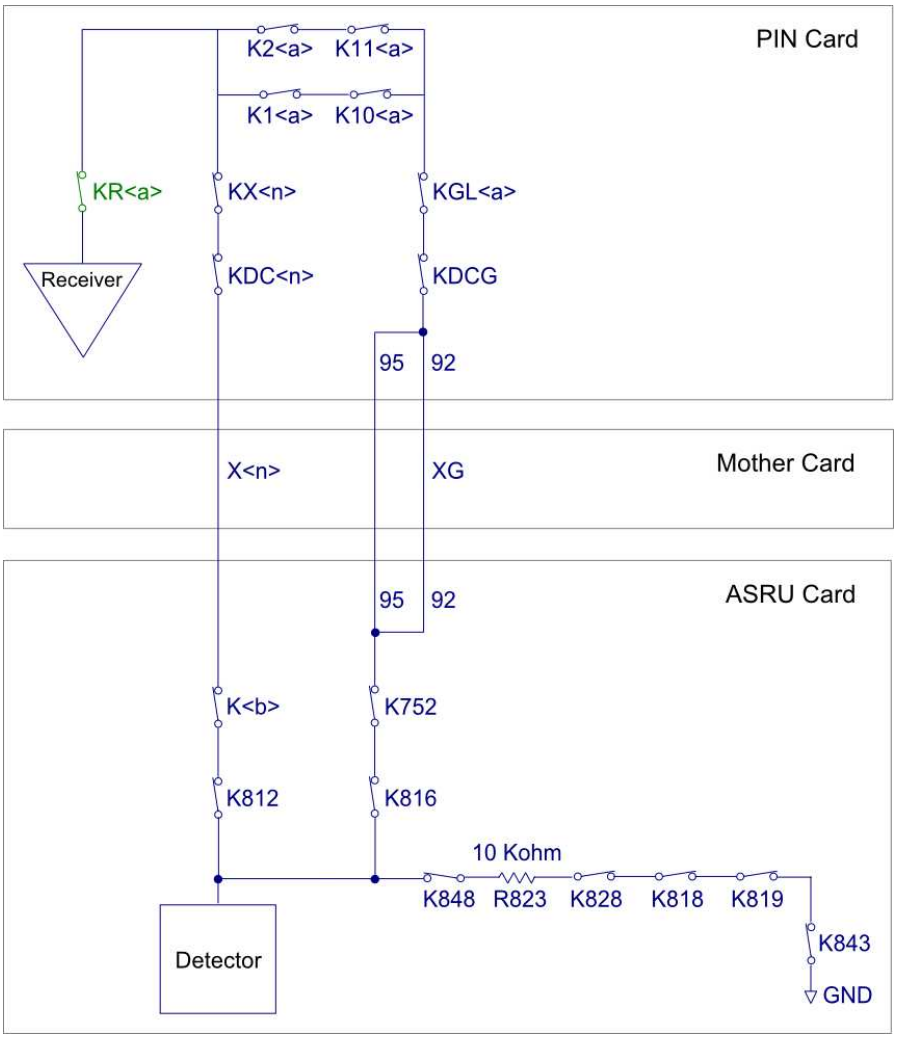
Test 3260 requires the proper operation of X-bus, X-bus disconnect, and XGL-bus relays.

Figure 5-4 shows the measurement path.

Table 5-14

Subtest	KR<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-4 T3260



Test 3270

Test Driver Channel Relays can be Closed

This test verifies the driver channel relays K<x>P0 through K<x>P7 can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

Test 3270 sets the driver high (+3.5 volts), closes the driver channel relay, and then measures the driver output level. A 10-kohm path to ground ensures that the test will fail if the path is open; it eliminates the possibility of a drift value.

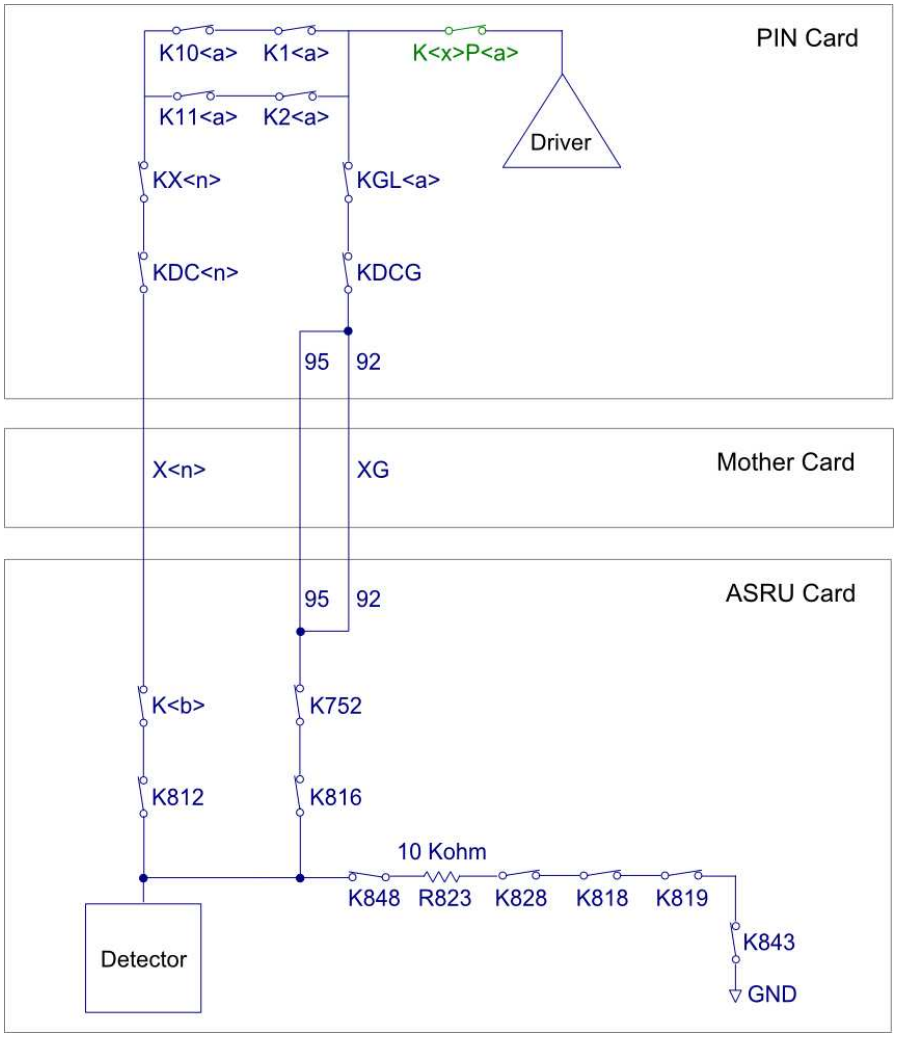
Test 3270 requires the proper operation of X-bus, X-bus disconnect, XGL-bus, and fixture interface (MINT) pin relays.

Figure 5-5 shows the measurement path.

Table 5-15

Subtest	K<x>P<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KAP0**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KAP1**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KAP2**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KAP3**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KAP4**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KAP5**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KAP6**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KAP7**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KBP0**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KBP1**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KBP2**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KBP3**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KBP4**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KBP5**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KBP6**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KBP7**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-5 T3270



Test 3272

Test Receiver to Driver Sense Connect Relays can be Closed

This test verifies the double-density card K<x>C relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

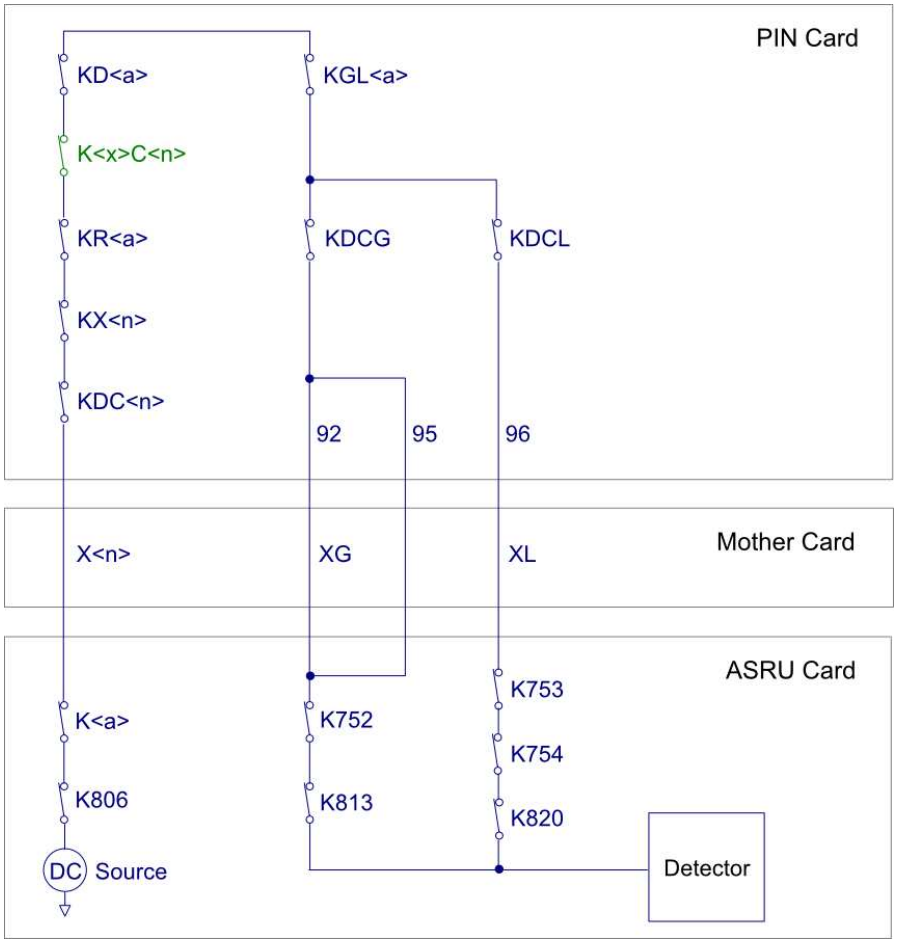
This test can be executed with or without the Pin Verification Fixture. It requires proper operation of: ASRU, Disconnect relays, X Bus relays, Driver relays, and Receiver relays

Figure 5-6 shows the measurement path.

Table 5-16

Subtest	K<n>	KDC<n>	KX<n>	KR<n>	K<x>C<n>	KD<n>	KGL<n>
Page A							
0a	K733	KDC1	KX1	KRA	**KAC0**	KDA	KGLA
1a	K734	KDC2	KX2	KRB	**KAC1**	KDB	KGLB
2a	K735	KDC3	KX3	KRC	**KAC2**	KDC	KGLC
3a	K746	KDC4	KX4	KRD	**KAC3**	KDD	KGLD
4a	K737	KDC5	KX5	KRE	**KAC4**	KDE	KGLE
5a	K738	KDC6	KX6	KRF	**KAC5**	KDF	KGLF
6a	K739	KDC7	KX7	KRG	**KAC6**	KDG	KGLG
7a	K740	KDC8	KX8	KRH	**KAC7**	KDH	KGLH
Page B							
0b	K733	KDC1	KX1	KRA	**KBC0**	KDA	KGLA
1b	K734	KDC2	KX2	KRB	**KBC1**	KDB	KGLB
2b	K735	KDC3	KX3	KRC	**KBC2**	KDC	KGLC
3b	K746	KDC4	KX4	KRD	**KBC3**	KDD	KGLD
4b	K737	KDC5	KX5	KRE	**KBC4**	KDE	KGLE
5b	K738	KDC6	KX6	KRF	**KBC5**	KDF	KGLF
6b	K739	KDC7	KX7	KRG	**KBC6**	KDG	KGLG
7b	K740	KDC8	KX8	KRH	**KBC7**	KDH	KGLH

Figure 5-6 T3272



Test 3274

Test Driver to XL-Bus Connect Relays can be Closed

This test verifies the K<x>X relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

This test can be executed with or without the Pin Verification Fixture. Each X-bus pin is connected to the ASRU's S-bus, and the XL-bus pin is connected to the I-bus. A resistance measurement is then performed.

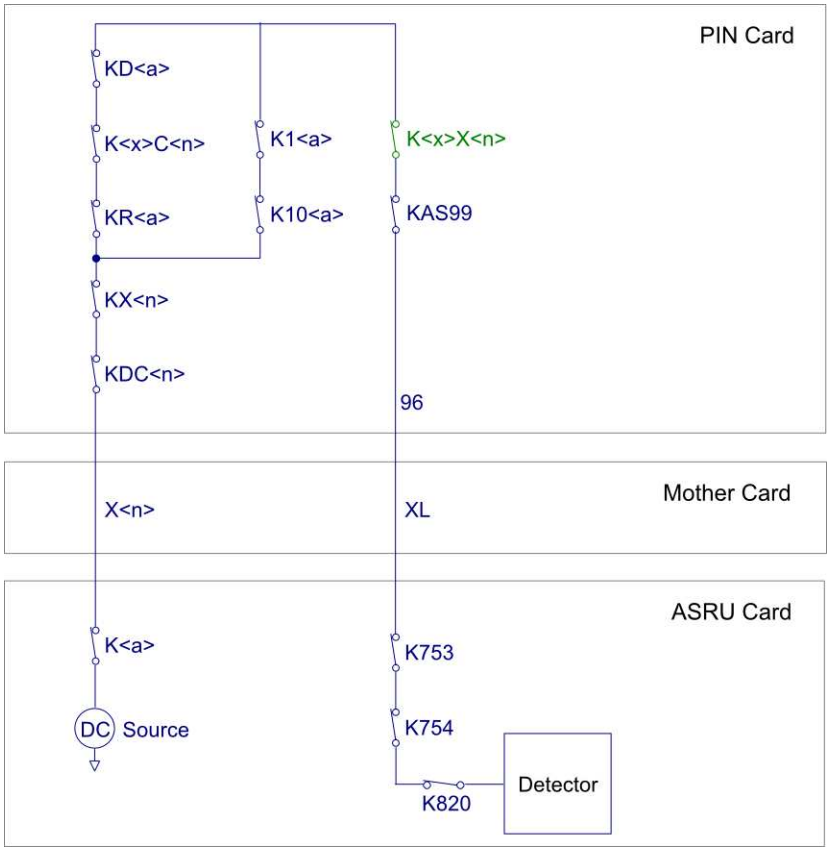
Requires proper operation of: ASRU, disconnect relays, X Bus relays, Receiver relays, Driver-to-Receiver relays, Driver relays, K999.

Figure 5-7 shows the measurement path.

Table 5-17

Subtest	K<x>X<n>	K<a>	KDC<n>	KX<n>	KR<a>	K<x>C<n>	KD<a>	K1<a>	K10<a>
Page A									
0a	**KAX09**	K733	KDC1	KX1	KRA	KAC0	KDA	K1A	K10A
1a	**KAX19**	K734	KDC2	KX2	KRB	KAC1	KDB	K1B	K10B
2a	**KAX29**	K735	KDC3	KX3	KRC	KAC2	KDC	K1C	K10C
3a	**KAX39**	K736	KDC4	KX4	KRD	KAC3	KDD	K1D	K10D
4a	**KAX49**	K737	KDC5	KX5	KRE	KAC4	KDE	K1E	K10E
5a	**KAX59**	K738	KDC6	KX6	KRF	KAC5	KDF	K1F	K10F
6a	**KAX69**	K739	KDC7	KX7	KRG	KAC6	KDG	K1G	K10G
7a	**KAX79**	K740	KDC8	KX8	KRH	KAC7	KDH	K1H	K10H
Page B									
0b	**KBX09**	K733	KDC1	KX1	KRA	KBC0	KDA	K1A	K10A
1b	**KBX19**	K734	KDC2	KX2	KRB	KBC1	KDB	K1B	K10B
2b	**KBX29**	K735	KDC3	KX3	KRC	KBC2	KDC	K1C	K10C
3b	**KBX39**	K736	KDC4	KX4	KRD	KBC3	KDD	K1D	K10D
4b	**KBX49**	K737	KDC5	KX5	KRE	KBC4	KDE	K1E	K10E
5b	**KBX59**	K738	KDC6	KX6	KRF	KBC5	KDF	K1F	K10F
6b	**KBX69**	K739	KDC7	KX7	KRG	KBC6	KDG	K1G	K10G
7b	**KBX79**	K740	KDC8	KX8	KRH	KBC7	KDH	K1H	K10H

Figure 5-7 T3274



Test 3276

Test X-Bus Disconnect Relays can be Closed

This test verifies the KDC<n> relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

This test can be executed with or without the Pin Verification Fixture.A pair of disconnect relays are closed creating a path in and out of the Pin card. One X-bus pin is connected to the ASRU source via the S-bus, another X-bus pin is connected to the ASRU detector via the L-bus, and a resistance measurement performed.

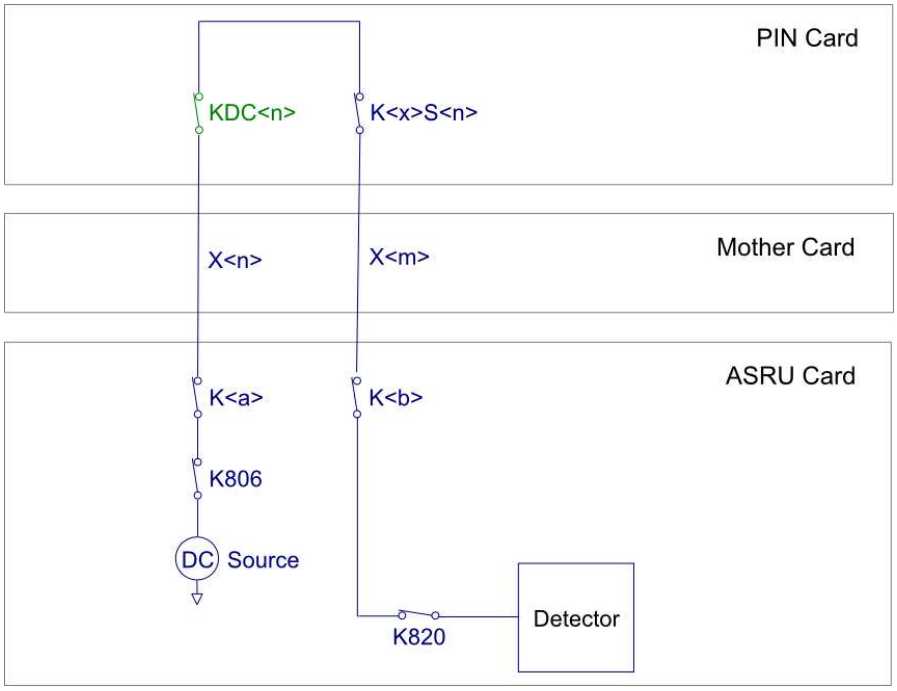
This test requires the proper operation of the ASRU and the other set of Pin disconnect relays.

Figure 5-8 shows the measurement path.

Table 5-18

Subtest	KDC<n>	K<x>S<n>	K<a>	K<b>
Page A				
0a	**KDC1**	KAS31	K733	K719
1a	**KDC2**	KAS42	K734	K720
2a	**KDC3**	KAS53	K735	K721
3a	**KDC4**	KAS64	K736	K722
4a	**KDC5**	KAS75	K737	K723
5a	**KDC6**	KAS86	K738	K724
6a	**KDC7**	KAS17	K739	K717
7a	**KDC8**	KAS28	K740	K718
Page B				
0b	**KDC1**	KBS31	K733	K719
1b	**KDC2**	KBS42	K734	K720
2b	**KDC3**	KBS53	K735	K721
3b	**KDC4**	KBS64	K736	K722
4b	**KDC5**	KBS75	K737	K723
5b	**KDC6**	KBS86	K738	K724
6b	**KDC7**	KBS17	K739	K717
7b	**KDC8**	KBS28	K740	K718

Figure 5-8 T3276



Test 3278

Test Ground-Bounce Relays can be Closed

Requires: Double-density pin cards

This test verifies the KBV<n> relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

This test can be executed with or without the Pin Verification Fixture. It requires the proper operation of: ASRU, Disconnect relays, X Bus relays, and Channel MUX relays. A redundant test path is created up to the KBV<n> relays, and the detector measures for 0 volts across the closed relay. The return path is via chassis ground.

Figure 5-9 shows the measurement path.

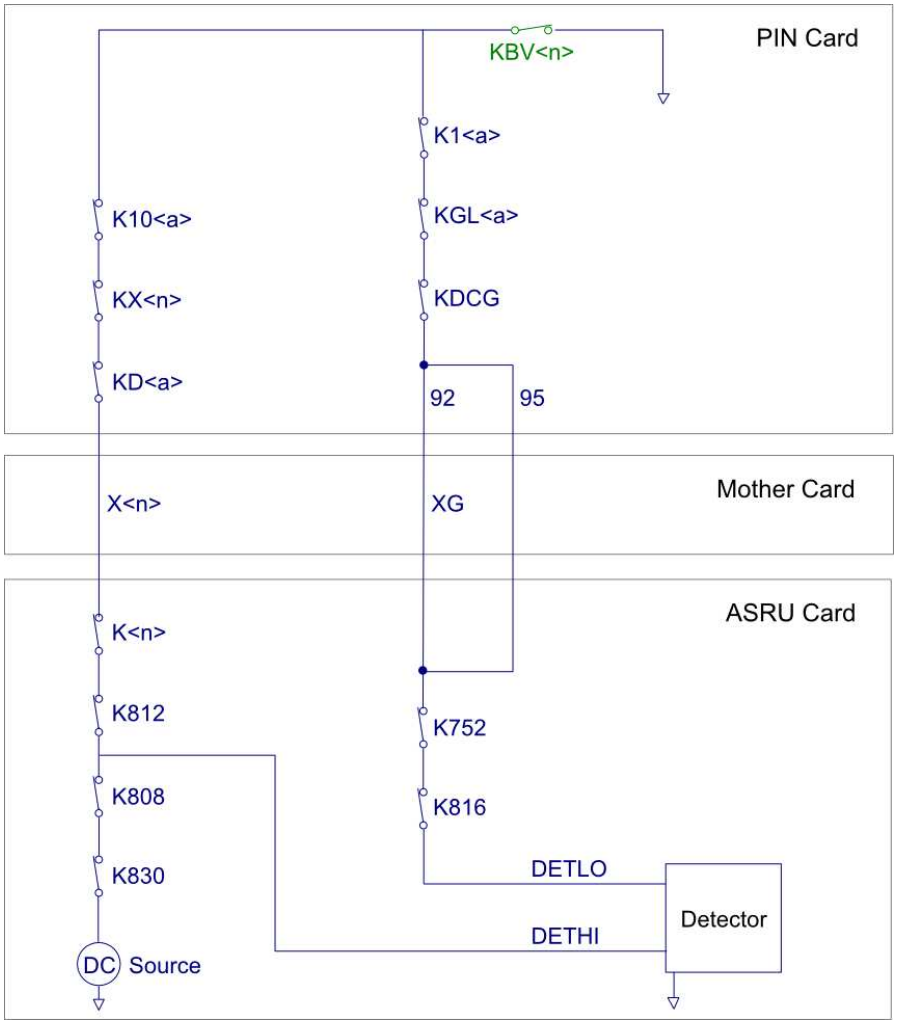
Table 5-19

Subtest	KBV<n>	K1<n>	K10<n>	KX<n>	KGL<n>	KD<n>	K<n>
Page B							
0	**KBV11**	K1B	K10B	KX2	KGLB	KDC2	K726
1	**KBV12**	K2B	K11B	KX2	KGLB	KDC2	K726
2	**KBV13**	K3B	K12B	KX2	KGLB	KDC2	K726
3	**KBV14**	K4B	K13B	KX2	KGLB	KDC2	K726
4	**KBV15**	K5B	K14B	KX2	KGLB	KDC2	K726
5	**KBV16**	K6B	K15B	KX2	KGLB	KDC2	K726
6	**KBV17**	K7B	K16B	KX2	KGLB	KDC2	K726
7	**KBV18**	K8B	K17B	KX2	KGLB	KDC2	K726
8	**KBV19**	K9B	K18B	KX2	KGLB	KDC2	K726
9	**KBV31**	K1D	K10D	KX4	KGLD	KDC4	K728
10	**KBV32**	K2D	K11D	KX4	KGLD	KDC4	K728
11	**KBV33**	K3D	K12D	KX4	KGLD	KDC4	K728
12	**KBV34**	K4D	K13D	KX4	KGLD	KDC4	K728
13	**KBV35**	K5D	K14D	KX4	KGLD	KDC4	K728
14	**KBV36**	K6D	K15D	KX4	KGLD	KDC4	L728
15	**KBV37**	K7D	K16D	KX4	KGLD	KDC4	K728
16	**KBV38**	K8D	K17D	KX4	KGLD	KDC4	K728
17	**KBV39**	K9D	K18D	KX4	KGLD	KDC4	K728

Table 5-19

Subtest	KBV<n>	K1<n>	K10<n>	KX<n>	KGL<n>	KD<n>	K<n>
18	**KBV41**	K1E	K10E	KX5	KGLE	KDC5	K729
19	**KBV42**	K2E	K11E	KX5	KGLE	KDC5	K729
20	**KBV43**	K3E	K12E	KX5	KGLE	KDC5	K729
21	**KBV44**	K4E	K13E	KX5	KGLE	KDC5	K729
22	**KBV45**	K5E	K14E	KX5	KGLE	KDC5	K729
23	**KBV46**	K6E	K15E	KX5	KGLE	KDC5	K729
24	**KBV47**	K7E	K16E	KX5	KGLE	KDC5	K729
25	**KBV48**	K8E	K17E	KX5	KGLE	KDC5	K729
26	**KBV49**	K9E	K18E	KX5	KGLE	KDC5	K729
27	**KBV61**	K1G	K10G	KX7	KGLG	KDC7	K731
28	**KBV62**	K2G	K11G	KX7	KGLG	KDC7	K731
29	**KBV63**	K3G	K12G	KX7	KGLG	KDC7	K731
30	**KBV64**	K4G	K13G	KX7	KGLG	KDC7	K731
31	**KBV65**	K5G	K14G	KX7	KGLG	KDC7	K731
32	**KBV66**	K6G	K15G	KX7	KGLG	KDC7	K731
33	**KBV67**	K7G	K16G	KX7	KGLG	KDC7	K731
34	**KBV68**	K8G	K17G	KX7	KGLG	KDC7	K731
35	**KBV69**	K9G	K18G	KX7	KGLG	KDC7	K731

Figure 5-9 T3278



Test 3280

Test Receiver Channel Relays can be Closed (AnalogPlus Pin Card ONLY)

This test verifies relays KRA through KRH can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

Test 3280 uses the ASRU source and detector to determine if a relay is stuck open. A 10-kohm path to ground ensures the test will fail if the path is open; it eliminates the possibility of a drift value.

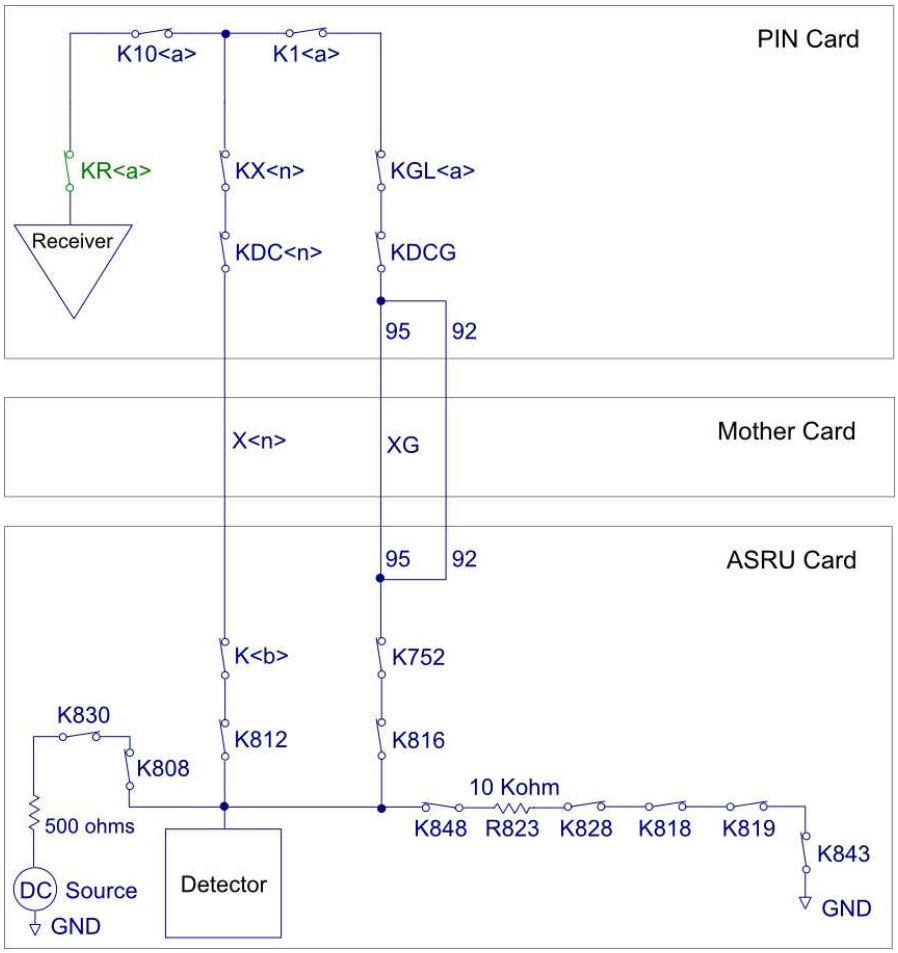
Test 3280 requires the proper operation of X-bus, X-bus disconnect, and XGL-bus relays.

Figure 5-10 shows the measurement path.

Table 5-20

Subtest	KR<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-10 T3280



Test 3285

Test Driver Channel Relays can be Closed (AnalogPlus Pin Card ONLY)

This test verifies relays KDA through KDH can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

Test 3285 uses the ASRU source and detector to determine if a relay is stuck open. A 10-kohm path to ground ensures that the test will fail if the path is open; it eliminates the possibility of a drift value.

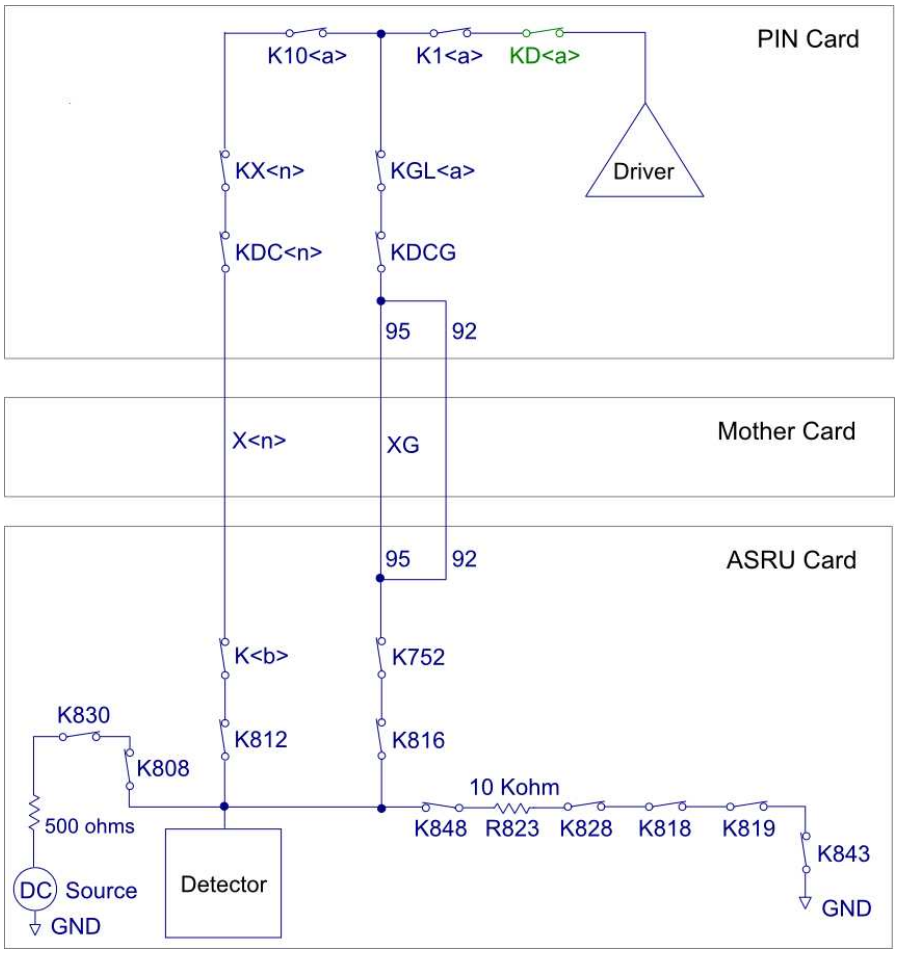
Test 3285 requires the proper operation of X-bus, X-bus disconnect, XGL-bus, and fixture interface (MINT) pin relays.

Figure 5-11 shows the measurement path.

Table 5-21

Subtest	KD<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KDA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KDB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KDC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KDD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KDE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KDF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KDG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KDH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KDA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KDB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KDC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KDD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KDE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KDF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KDG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KDH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-11 T3285



Open Relay

Test 3310

Test Receiver to X-bus Connect Relays can be Opened

This test verifies KX1 through KX8 can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3310 is dependent on functioning XGL-bus, X-bus disconnect, and fixture interface (MINT) pin relays. Figure 5-12 shows the measurement path.

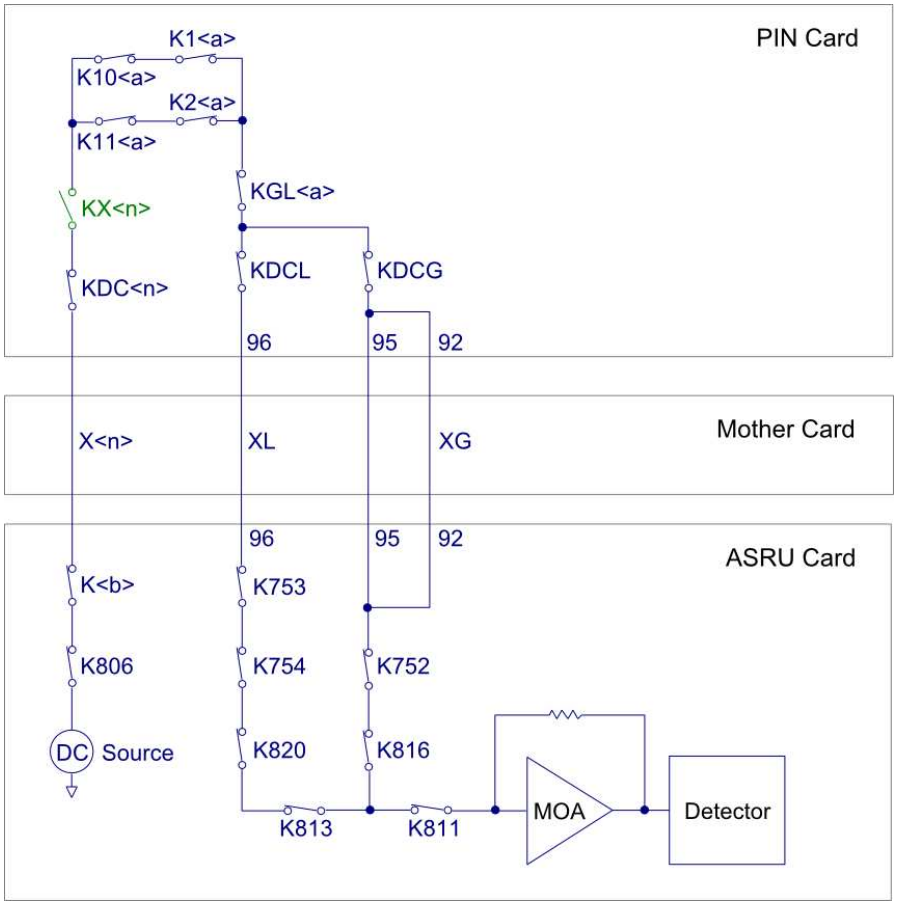
Table 5-22

Subtest	KX<n>	X<n>	KDC<n>	K<b>	K1<a>	K2<a>	K10<a>	K11<a>	KGL<a>
Page A									
0a	**KX1**	X1	KDC1	K733	K1A	K2A	K10A	K11A	KGLA
1a	**KX2**	X2	KDC2	K734	K1B	K2B	K10B	K11B	KGLB
2a	**KX3**	X3	KDC3	K735	K1C	K2C	K10C	K11C	KGLC
3a	**KX4**	X4	KDC4	K736	K1D	K2D	K10D	K11D	KGLD
4a	**KX5**	X5	KDC5	K737	K1E	K2E	K10E	K11E	KGLE
5a	**KX6**	X6	KDC6	K738	K1F	K2F	K10F	K11F	KGLF
6a	**KX7**	X7	KDC7	K739	K1G	K2G	K10G	K11G	KGLG
7a	**KX8**	X8	KDC8	K740	K1H	K2H	K10H	K11H	KGLH

Table 5-22

Subtest	KX<n>	X<n>	KDC<n>	K<b>	K1<a>	K2<a>	K10<a>	K11<a>	KGL<a>
Page B									
0b	**KX1**	X1	KDC1	K733	K1A	K2A	K10A	K11A	KGLA
1b	**KX2**	X2	KDC2	K734	K1B	K2B	K10B	K11B	KGLB
2b	**KX3**	X3	KDC3	K735	K1C	K2C	K10C	K11C	KGLC
3b	**KX4**	X4	KDC4	K736	K1D	K2D	K10D	K11D	KGLD
4b	**KX5**	X5	KDC5	K737	K1E	K2E	K10E	K11E	KGLE
5b	**KX6**	X6	KDC6	K738	K1F	K2F	K10F	K11F	KGLF
6b	**KX7**	X7	KDC7	K739	K1G	K2G	K10G	K11G	KGLG
7b	**KX8**	X8	KDC8	K740	K1H	K2H	K10H	K11H	KGLH

Figure 5-12 T3310



Test 3320

Test X-Bus Disconnect Relays can be Opened

This test verifies that KDC1 through KDC8 can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

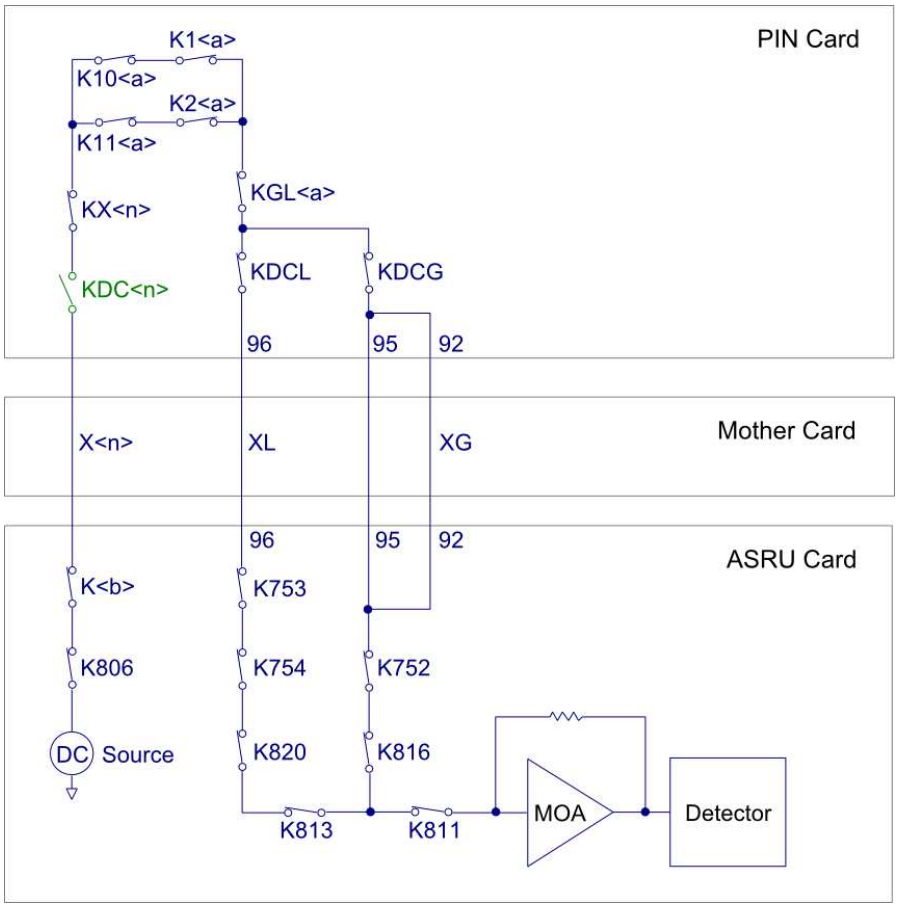
Test 3320 is dependent on functioning XGL-bus, X-bus, and fixture interface (MINT) pin relays.

Figure 5-13 shows the measurement path.

Table 5-23

Subtest	KDC<n>	X<n>	K<b>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	KGL<a>
Page A									
0a	**KDC1**	X1	K733	KX1	K1A	K2A	K10A	K11A	KGLA
1a	**KDC2**	X2	K734	KX2	K1B	K2B	K10B	K11B	KGLB
2a	**KDC3**	X3	K735	KX3	K1C	K2C	K10C	K11C	KGLC
3a	**KDC4**	X4	K736	KX4	K1D	K2D	K10D	K11D	KGLD
4a	**KDC5**	X5	K737	KX5	K1E	K2E	K10E	K11E	KGLE
5a	**KDC6**	X6	K738	KX6	K1F	K2F	K10F	K11F	KGLF
6a	**KDC7**	X7	K739	KX7	K1G	K2G	K10G	K11G	KGLG
7a	**KDC8**	X8	K740	KX8	K1H	K2H	K10H	K11H	KGLH
Page B									
0b	**KDC1**	X1	K733	KX1	K1A	K2A	K10A	K11A	KGLA
1b	**KDC2**	X2	K734	KX2	K1B	K2B	K10B	K11B	KGLB
2b	**KDC3**	X3	K735	KX3	K1C	K2C	K10C	K11C	KGLC
3b	**KDC4**	X4	K736	KX4	K1D	K2D	K10D	K11D	KGLD
4b	**KDC5**	X5	K737	KX5	K1E	K2E	K10E	K11E	KGLE
5b	**KDC6**	X6	K738	KX6	K1F	K2F	K10F	K11F	KGLF
6b	**KDC7**	X7	K739	KX7	K1G	K2G	K10G	K11G	KGLG
7b	**KDC8**	X8	K740	KX8	K1H	K2H	K10H	K11H	KGLH

Figure 5-13 T3320



Test 3330

Test Driver to XGL-bus Connect Relays can be Opened

This test verifies that KGLA through KGLH can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

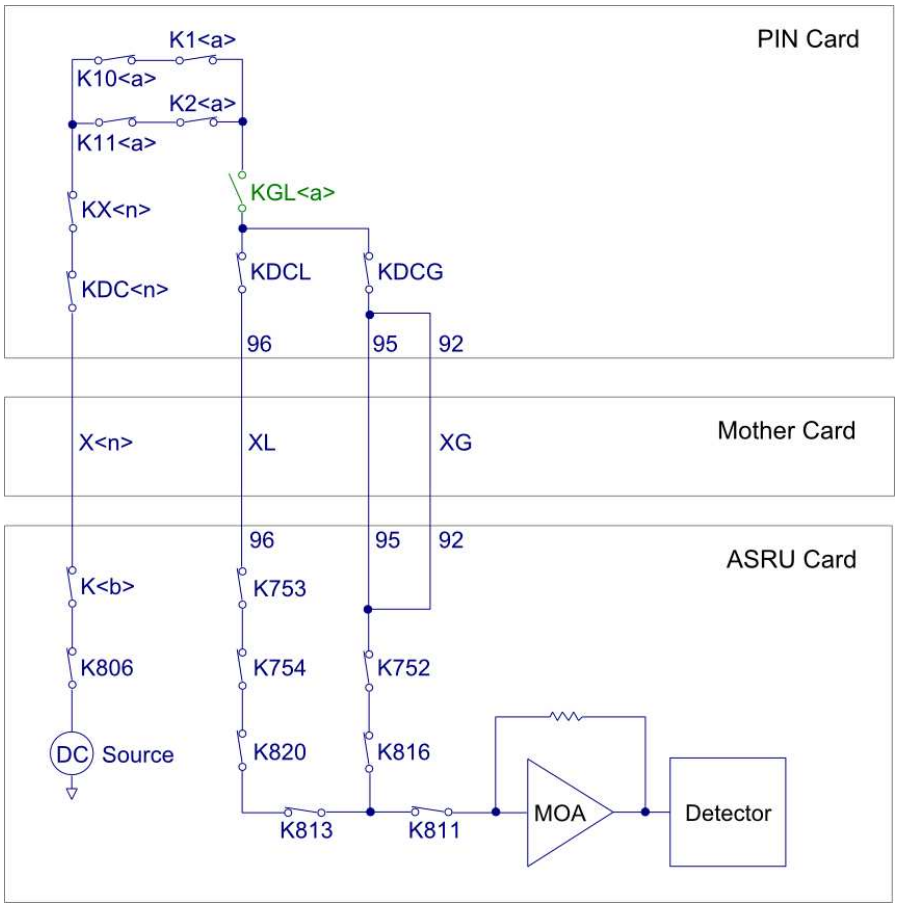
Test 3330 is dependent on functioning X-bus disconnect, X-bus, and fixture interface (MINT) pin relays.

Figure 5-14 shows the measurement path.

Table 5-24

Subtest	KGL<a>	X<n>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	K<b>
Page A									
0a	**KGLA**	X1	KDC1	KX1	K1A	K2A	K10A	K11A	K733
1a	**KGLB**	X2	KDC2	KX2	K1B	K2B	K10B	K11B	K734
2a	**KGLC**	X3	KDC3	KX3	K1C	K2C	K10C	K11C	K735
3a	**KGLD**	X4	KDC4	KX4	K1D	K2D	K10D	K11D	K736
4a	**KGLE**	X5	KDC5	KX5	K1E	K2E	K10E	K11E	K737
5a	**KGLF**	X6	KDC6	KX6	K1F	K2F	K10F	K11F	K738
6a	**KGLG**	X7	KDC7	KX7	K1G	K2G	K10G	K11G	K739
7a	**KGLH**	X8	KDC8	KX8	K1H	K2H	K10H	K11H	K740
Page B									
0b	**KGLA**	X1	KDC1	KX1	K1A	K2A	K10A	K11A	K733
1b	**KGLB**	X2	KDC2	KX2	K1B	K2B	K10B	K11B	K734
2b	**KGLC**	X3	KDC3	KX3	K1C	K2C	K10C	K11C	K735
3b	**KGLD**	X4	KDC4	KX4	K1D	K2D	K10D	K11D	K736
4b	**KGLE**	X5	KDC5	KX5	K1E	K2E	K10E	K11E	K737
5b	**KGLF**	X6	KDC6	KX6	K1F	K2F	K10F	K11F	K738
6b	**KGLG**	X7	KDC7	KX7	K1G	K2G	K10G	K11G	K739
7b	**KGLH**	X8	KDC8	KX8	K1H	K2H	K10H	K11H	K740

Figure 5-14 T3330



Test 3340

Test KDCG and KDCL can be Opened

This test verifies that relays KDCG and KDCL can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Figure 5-15 shows the measurement paths for subtest 0 and subtest 1.

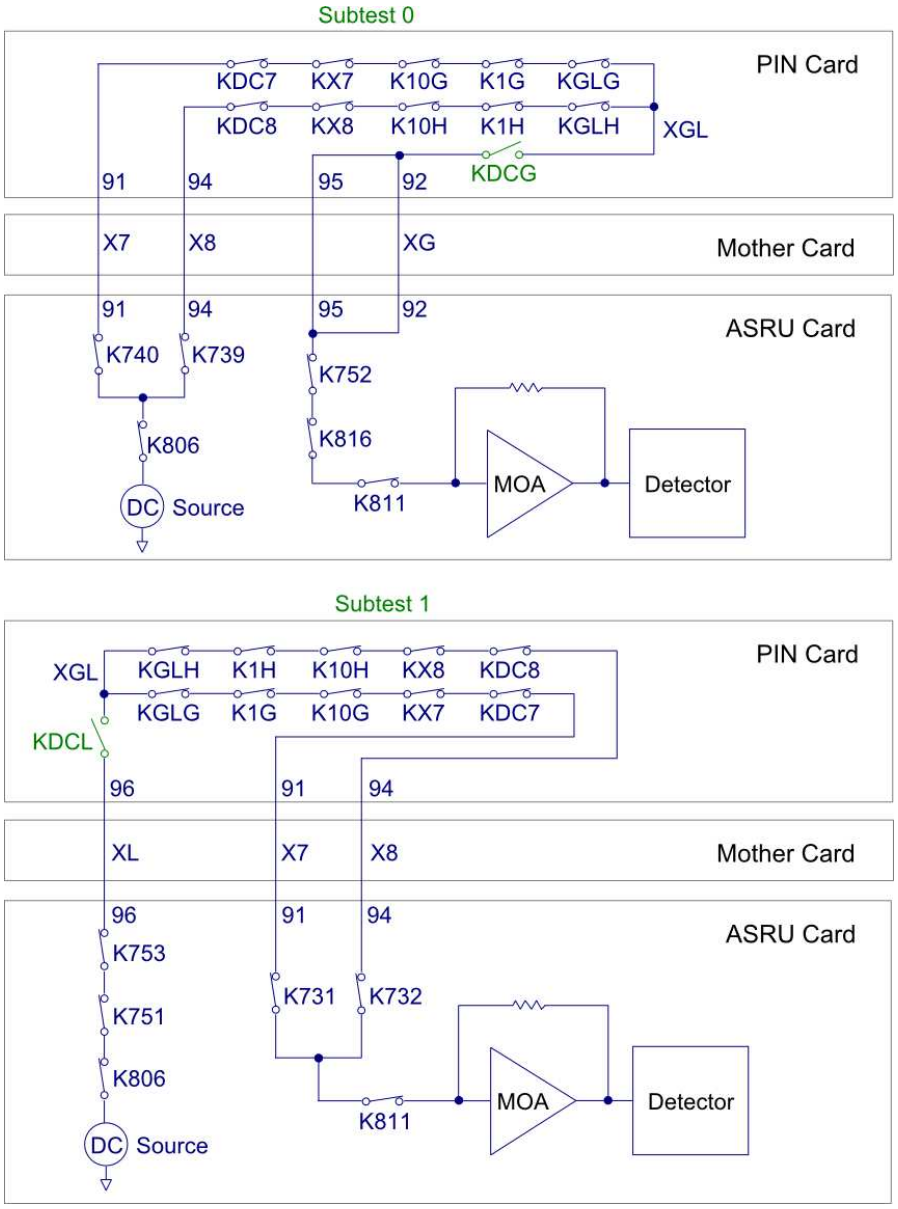
Table 5-25

Subtest	KDC<n>	KDC7	KDC8	KD1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
Page A											
0a	**KDCG**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
1a	**KDCL**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH

Table 5-25

Subtest	KDC<n>	KDC7	KDC8	KD1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
Page B											
0b	**KDCG**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH
1b	**KDCL**	KDC7	KDC8	K1G	K1H	K10G	K10H	KX7	KX8	KGLG	KGLH

Figure 5-15 T3340



Test 3350

Test Receiver to Fixture Interface (MINT) Pin (MUX) Relays can be Opened

This test verifies that the relays that K10A-H can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3350 is dependent on functioning KDC<n>, KX<n>, KGL<a>, and K<d> (driver fixture interface (MINT) pin) relays.

Figure 5-16 shows the subtest path.

Table 5-26

Subtest	K<r>	K<b>	X<n>	KDC<n>	KX<n>	K<d>	KGL<a>
Page A							
0a	**K10A**	K733	X1	KDC1	KX1	K1A	KGLA
1a	**K11A**	K733	X1	KDC1	KX1	K2A	KGLA
2a	**K12A**	K733	X1	KDC1	KX1	K3A	KGLA
3a	**K13A**	K733	X1	KDC1	KX1	K4A	KGLA
4a	**K14A**	K733	X1	KDC1	KX1	K5A	KGLA
5a	**K15A**	K733	X1	KDC1	KX1	K6A	KGLA
6a	**K16A**	K733	X1	KDC1	KX1	K7A	KGLA
7a	**K17A**	K733	X1	KDC1	KX1	K8A	KGLA
8a	**K18A**	K733	X1	KDC1	KX1	K9A	KGLA
9a	**K10B**	K734	X2	KDC2	KX2	K1B	KGLB
10a	**K11B**	K734	X2	KDC2	KX2	K2B	KGLB
11a	**K12B**	K734	X2	KDC2	KX2	K3B	KGLB
12a	**K13B**	K734	X2	KDC2	KX2	K4B	KGLB
13a	**K14B**	K734	X2	KDC2	KX2	K5B	KGLB
14a	**K15B**	K734	X2	KDC2	KX2	K6B	KGLB
15a	**K16B**	K734	X2	KDC2	KX2	K7B	KGLB
16a	**K17B**	K734	X2	KDC2	KX2	K8B	KGLB
17a	**K18B**	K734	X2	KDC2	KX2	K9B	KGLB
18a	**K10C**	K735	X3	KDC3	KX3	K1C	KGLC
19a	**K11C**	K735	X3	KDC3	KX3	K2C	KGLC
20a	**K12C**	K735	X3	KDC3	KX3	K3C	KGLC

Table 5-26

Subtest	K<r>	K<b>	X<n>	KDC<n>	KX<n>	K<d>	KGL<a>
21a	**K13C**	K735	X3	KDC3	KX3	K4C	KGLC
22a	**K14C**	K735	X3	KDC3	KX3	K5C	KGLC
23a	**K15C**	K735	X3	KDC3	KX3	K6C	KGLC
24a	**K16C**	K735	X3	KDC3	KX3	K7C	KGLC
25a	**K17C**	K735	X3	KDC3	KX3	K8C	KGLC
26a	**K18C**	K735	X3	KDC3	KX3	K9C	KGLC
27a	**K10D**	K736	X4	KDC4	KX4	K1D	KGLD
28a	**K11D**	K736	X4	KDC4	KX4	K2D	KGLD
29a	**K12D**	K736	X4	KDC4	KX4	K3D	KGLD
30a	**K13D**	K736	X4	KDC4	KX4	K4D	KGLD
31a	**K14D**	K736	X4	KDC4	KX4	K5D	KGLD
32a	**K15D**	K736	X4	KDC4	KX4	K6D	KGLD
33a	**K16D**	K736	X4	KDC4	KX4	K7D	KGLD
34a	**K17D**	K736	X4	KDC4	KX4	K8D	KGLD
35a	**K18D**	K736	X4	KDC4	KX4	K9D	KGLD
36a	**K10E**	K737	X5	KDC5	KX5	K1E	KGLE
37a	**K11E**	K737	X5	KDC5	KX5	K2E	KGLE
38a	**K12E**	K737	X5	KDC5	KX5	K3E	KGLE
39a	**K13E**	K737	X5	KDC5	KX5	K4E	KGLE
40a	**K14E**	K737	X5	KDC5	KX5	K5E	KGLE
41a	**K15E**	K737	X5	KDC5	KX5	K6E	KGLE
42a	**K16E**	K737	X5	KDC5	KX5	K7E	KGLE
43a	**K17E**	K737	X5	KDC5	KX5	K8E	KGLE
44a	**K18E**	K737	X5	KDC5	KX5	K9E	KGLE
45a	**K10F**	K738	X6	KDC6	KX6	K1F	KGLF
46a	**K11F**	K738	X6	KDC6	KX6	K2F	KGLF
47a	**K12F**	K738	X6	KDC6	KX6	K3F	KGLF
48a	**K13F**	K738	X6	KDC6	KX6	K4F	KGLF
49a	**K14F**	K738	X6	KDC6	KX6	K5F	KGLF
50a	**K15F**	K738	X6	KDC6	KX6	K6F	KGLF

Table 5-26

Subtest	K<r>	K<b>	X<n>	KDC<n>	KX<n>	K<d>	KGL<a>
51a	**K16F**	K738	X6	KDC6	KX6	K7F	KGLF
52a	**K17F**	K738	X6	KDC6	KX6	K8F	KGLF
53a	**K18F**	K738	X6	KDC6	KX6	K9F	KGLF
54a	**K10G**	K739	X7	KDC7	KX7	K1G	KGLG
55a	**K11G**	K739	X7	KDC7	KX7	K2G	KGLG
56a	**K12G**	K739	X7	KDC7	KX7	K3G	KGLG
57a	**K13G**	K739	X7	KDC7	KX7	K4G	KGLG
58a	**K14G**	K739	X7	KDC7	KX7	K5G	KGLG
59a	**K15G**	K739	X7	KDC7	KX7	K6G	KGLG
60a	**K16G**	K739	X7	KDC7	KX7	K7G	KGLG
61a	**K17G**	K739	X7	KDC7	KX7	K8G	KGLG
62a	**K18G**	K739	X7	KDC7	KX7	K9G	KGLG
63a	**K10H**	K740	X8	KDC8	KX8	K1H	KGLH
64a	**K11H**	K740	X8	KDC8	KX8	K2H	KGLH
65a	**K12H**	K740	X8	KDC8	KX8	K3H	KGLH
66a	**K13H**	K740	X8	KDC8	KX8	K4H	KGLH
67a	**K14H**	K740	X8	KDC8	KX8	K5H	KGLH
68a	**K15H**	K740	X8	KDC8	KX8	K6H	KGLH
69a	**K16H**	K740	X8	KDC8	KX8	K7H	KGLH
70a	**K17H**	K740	X8	KDC8	KX8	K8H	KGLH
71a	**K18H**	K740	X8	KDC8	KX8	K9H	KGLH
Page B							
0b	**K10A**	K733	X1	KDC1	KX1	K1A	KGLA
1b	**K11A**	K733	X1	KDC1	KX1	K2A	KGLA
2b	**K12A**	K733	X1	KDC1	KX1	K3A	KGLA
3b	**K13A**	K733	X1	KDC1	KX1	K4A	KGLA
4b	**K14A**	K733	X1	KDC1	KX1	K5A	KGLA
5b	**K15A**	K733	X1	KDC1	KX1	K6A	KGLA
6b	**K16A**	K733	X1	KDC1	KX1	K7A	KGLA
7b	**K17A**	K733	X1	KDC1	KX1	K8A	KGLA

Table 5-26

Subtest	K<r>	K<b>	X<n>	KDC<n>	KX<n>	K<d>	KGL<a>
8b	**K18A**	K733	X1	KDC1	KX1	K9A	KGLA
9b	**K10B**	K734	X2	KDC2	KX2	K1B	KGLB
10b	**K11B**	K734	X2	KDC2	KX2	K2B	KGLB
11b	**K12B**	K734	X2	KDC2	KX2	K3B	KGLB
12b	**K13B**	K734	X2	KDC2	KX2	K4B	KGLB
13b	**K14B**	K734	X2	KDC2	KX2	K5B	KGLB
14b	**K15B**	K734	X2	KDC2	KX2	K6B	KGLB
15b	**K16B**	K734	X2	KDC2	KX2	K7B	KGLB
16b	**K17B**	K734	X2	KDC2	KX2	K8B	KGLB
17b	**K18B**	K734	X2	KDC2	KX2	K9B	KGLB
18b	**K10C**	K735	X3	KDC3	KX3	K1C	KGLC
19b	**K11C**	K735	X3	KDC3	KX3	K2C	KGLC
20b	**K12C**	K735	X3	KDC3	KX3	K3C	KGLC
21b	**K13C**	K735	X3	KDC3	KX3	K4C	KGLC
22b	**K14C**	K735	X3	KDC3	KX3	K5C	KGLC
23b	**K15C**	K735	X3	KDC3	KX3	K6C	KGLC
24b	**K16C**	K735	X3	KDC3	KX3	K7C	KGLC
25b	**K17C**	K735	X3	KDC3	KX3	K8C	KGLC
26b	**K18C**	K735	X3	KDC3	KX3	K9C	KGLC
27b	**K10D**	K736	X4	KDC4	KX4	K1D	KGLD
28b	**K11D**	K736	X4	KDC4	KX4	K2D	KGLD
29b	**K12D**	K736	X4	KDC4	KX4	K3D	KGLD
30b	**K13D**	K736	X4	KDC4	KX4	K4D	KGLD
31b	**K14D**	K736	X4	KDC4	KX4	K5D	KGLD
32b	**K15D**	K736	X4	KDC4	KX4	K6D	KGLD
33b	**K16D**	K736	X4	KDC4	KX4	K7D	KGLD
34b	**K17D**	K736	X4	KDC4	KX4	K8D	KGLD
35b	**K18D**	K736	X4	KDC4	KX4	K9D	KGLD
36b	**K10E**	K737	X5	KDC5	KX5	K1E	KGLE
37b	**K11E**	K737	X5	KDC5	KX5	K2E	KGLE

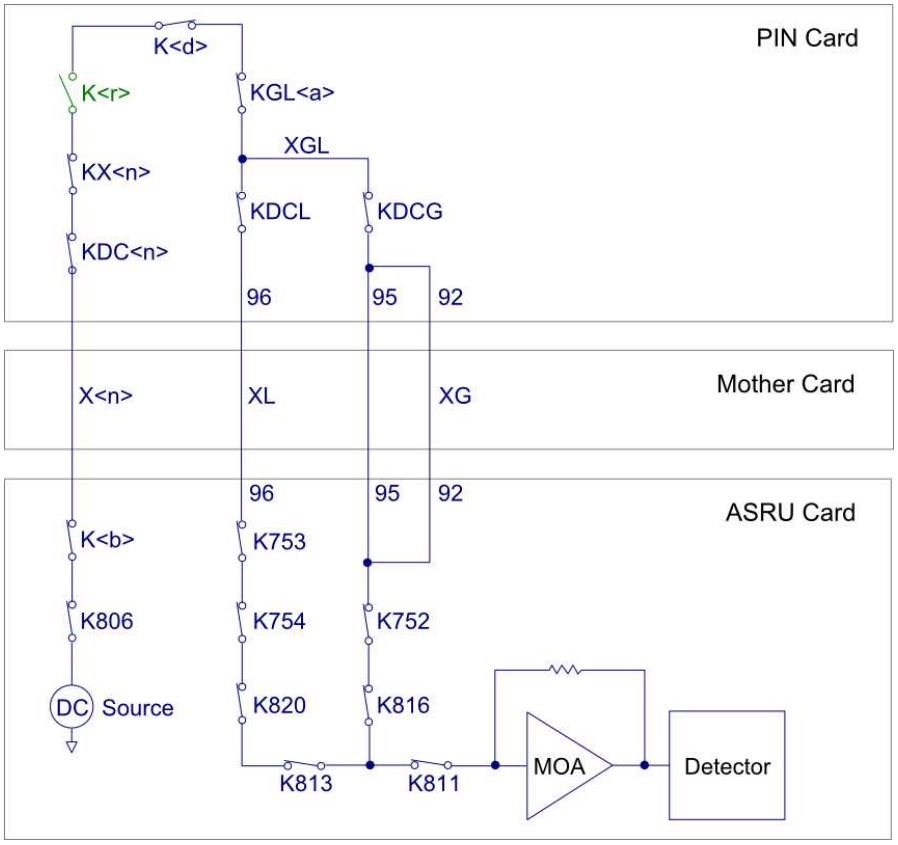
Table 5-26

Subtest	K<r>	K<b>	X<n>	KDC<n>	KX<n>	K<d>	KGL<a>
38b	**K12E**	K737	X5	KDC5	KX5	K3E	KGLE
39b	**K13E**	K737	X5	KDC5	KX5	K4E	KGLE
40b	**K14E**	K737	X5	KDC5	KX5	K5E	KGLE
41b	**K15E**	K737	X5	KDC5	KX5	K6E	KGLE
42b	**K16E**	K737	X5	KDC5	KX5	K7E	KGLE
43b	**K17E**	K737	X5	KDC5	KX5	K8E	KGLE
44b	**K18E**	K737	X5	KDC5	KX5	K9E	KGLE
45b	**K10F**	K738	X6	KDC6	KX6	K1F	KGLF
46b	**K11F**	K738	X6	KDC6	KX6	K2F	KGLF
47b	**K12F**	K738	X6	KDC6	KX6	K3F	KGLF
48b	**K13F**	K738	X6	KDC6	KX6	K4F	KGLF
49b	**K14F**	K738	X6	KDC6	KX6	K5F	KGLF
50b	**K15F**	K738	X6	KDC6	KX6	K6F	KGLF
51b	**K16F**	K738	X6	KDC6	KX6	K7F	KGLF
52b	**K17F**	K738	X6	KDC6	KX6	K8F	KGLF
53b	**K18F**	K738	X6	KDC6	KX6	K9F	KGLF
54b	**K10G**	K739	X7	KDC7	KX7	K1G	KGLG
55b	**K11G**	K739	X7	KDC7	KX7	K2G	KGLG
56b	**K12G**	K739	X7	KDC7	KX7	K3G	KGLG
57b	**K13G**	K739	X7	KDC7	KX7	K4G	KGLG
58b	**K14G**	K739	X7	KDC7	KX7	K5G	KGLG
59b	**K15G**	K739	X7	KDC7	KX7	K6G	KGLG
60b	**K16G**	K739	X7	KDC7	KX7	K7G	KGLG
61b	**K17G**	K739	X7	KDC7	KX7	K8G	KGLG
62b	**K18G**	K739	X7	KDC7	KX7	K9G	KGLG
63b	**K10H**	K740	X8	KDC8	KX8	K1H	KGLH
64b	**K11H**	K740	X8	KDC8	KX8	K2H	KGLH
65b	**K12H**	K740	X8	KDC8	KX8	K3H	KGLH
66b	**K13H**	K740	X8	KDC8	KX8	K4H	KGLH
67b	**K14H**	K740	X8	KDC8	KX8	K5H	KGLH

Table 5-26

Subtest	K<r>	K<b>	X<n>	KDC<n>	KX<n>	K<d>	KGL<a>
68b	**K15H**	K740	X8	KDC8	KX8	K6H	KGLH
69b	**K16H**	K740	X8	KDC8	KX8	K7H	KGLH
70b	**K17H**	K740	X8	KDC8	KX8	K8H	KGLH
71b	**K18H**	K740	X8	KDC8	KX8	K9H	KGLH

Figure 5-16 T3350



Test 3360

Test Driver to Fixture Interface (MINT) Pin (MUX) Relays can be Opened

This test verifies that K1A-H relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3360 is dependent on functioning X-bus, X-bus disconnect, XGL-bus, and receiver to fixture interface (MINT) pin relays.

Figure 5-17 shows the test path.

Table 5-27

Subtest	K<d>	K<b>	X<n>	KDC<n>	KX<n>	K<r>	KGL<a>
Page A							
0a	**K1A**	K733	X1	KDC1	KX1	K10A	KGLA
1a	**K2A**	K733	X1	KDC1	KX1	K11A	KGLA
2a	**K3A**	K733	X1	KDC1	KX1	K12A	KGLA
3a	**K4A**	K733	X1	KDC1	KX1	K13A	KGLA
4a	**K5A**	K733	X1	KDC1	KX1	K14A	KGLA
5a	**K6A**	K733	X1	KDC1	KX1	K15A	KGLA
6a	**K7A**	K733	X1	KDC1	KX1	K16A	KGLA
7a	**K8A**	K733	X1	KDC1	KX1	K17A	KGLA
8a	**K9A**	K733	X1	KDC1	KX1	K18A	KGLA
9a	**K1B**	K734	X2	KDC2	KX2	K10B	KGLB
10a	**K2B**	K734	X2	KDC2	KX2	K11B	KGLB
11a	**K3B**	K734	X2	KDC2	KX2	K12B	KGLB
12a	**K4B**	K734	X2	KDC2	KX2	K13B	KGLB
13a	**K5B**	K734	X2	KDC2	KX2	K14B	KGLB
14a	**K6B**	K734	X2	KDC2	KX2	K15B	KGLB
15a	**K7B**	K734	X2	KDC2	KX2	K16B	KGLB
16a	**K8B**	K734	X2	KDC2	KX2	K17B	KGLB
17a	**K9B**	K734	X2	KDC2	KX2	K18B	KGLB
18a	**K1C**	K735	X3	KDC3	KX3	K10C	KGLC
19a	**K2C**	K735	X3	KDC3	KX3	K11C	KGLC
20a	**K3C**	K735	X3	KDC3	KX3	K12C	KGLC
21a	**K4C**	K735	X3	KDC3	KX3	K13C	KGLC
22a	**K5C**	K735	X3	KDC3	KX3	K14C	KGLC
23a	**K6C**	K735	X3	KDC3	KX3	K15C	KGLC
24a	**K7C**	K735	X3	KDC3	KX3	K16C	KGLC
25a	**K8C**	K735	X3	KDC3	KX3	K17C	KGLC
26a	**K9C**	K735	X3	KDC3	KX3	K18C	KGLC
27a	**K1D**	K736	X4	KDC4	KX4	K10D	KGLD

Table 5-27

Subtest	K<d>	K<b>	X<n>	KDC<n>	KX<n>	K<r>	KGL<a>
28a	**K2D**	K736	X4	KDC4	KX4	K11D	KGLD
29a	**K3D**	K736	X4	KDC4	KX4	K12D	KGLD
30a	**K4D**	K736	X4	KDC4	KX4	K13D	KGLD
31a	**K5D**	K736	X4	KDC4	KX4	K14D	KGLD
32a	**K6D**	K736	X4	KDC4	KX4	K15D	KGLD
33a	**K7D**	K736	X4	KDC4	KX4	K16D	KGLD
34a	**K8D**	K736	X4	KDC4	KX4	K17D	KGLD
35a	**K9D**	K736	X4	KDC4	KX4	K18D	KGLD
36a	**K1E**	K737	X5	KDC5	KX5	K10E	KGLE
37a	**K2E**	K737	X5	KDC5	KX5	K11E	KGLE
38a	**K3E**	K737	X5	KDC5	KX5	K12E	KGLE
39a	**K4E**	K737	X5	KDC5	KX5	K13E	KGLE
40a	**K5E**	K737	X5	KDC5	KX5	K14E	KGLE
41a	**K6E**	K737	X5	KDC5	KX5	K15E	KGLE
42a	**K7E**	K737	X5	KDC5	KX5	K16E	KGLE
43a	**K8E**	K737	X5	KDC5	KX5	K17E	KGLE
44a	**K9E**	K737	X5	KDC5	KX5	K18E	KGLE
45a	**K1F**	K738	X6	KDC6	KX6	K10F	KGLF
46a	**K2F**	K738	X6	KDC6	KX6	K11F	KGLF
47a	**K3F**	K738	X6	KDC6	KX6	K12F	KGLF
48a	**K4F**	K738	X6	KDC6	KX6	K13F	KGLF
49a	**K5F**	K738	X6	KDC6	KX6	K14F	KGLF
50a	**K6F**	K738	X6	KDC6	KX6	K15F	KGLF
51a	**K7F**	K738	X6	KDC6	KX6	K16F	KGLF
52a	**K8F**	K738	X6	KDC6	KX6	K17F	KGLF
53a	**K9F**	K738	X6	KDC6	KX6	K18F	KGLF
54a	**K1G**	K739	X7	KDC7	KX7	K10G	KGLG
55a	**K2G**	K739	X7	KDC7	KX7	K11G	KGLG
56a	**K3G**	K739	X7	KDC7	KX7	K12G	KGLG
57a	**K4G**	K739	X7	KDC7	KX7	K13G	KGLG

Table 5-27

Subtest	K<d>	K<b>	X<n>	KDC<n>	KX<n>	K<r>	KGL<a>
58a	**K5G**	K739	X7	KDC7	KX7	K14G	KGLG
59a	**K6G**	K739	X7	KDC7	KX7	K15G	KGLG
60a	**K7G**	K739	X7	KDC7	KX7	K16G	KGLG
61a	**K8G**	K739	X7	KDC7	KX7	K17G	KGLG
62a	**K9G**	K739	X7	KDC7	KX7	K18G	KGLG
63a	**K1H**	K740	X8	KDC8	KX8	K10H	KGLH
64a	**K2H**	K740	X8	KDC8	KX8	K11H	KGLH
65a	**K3H**	K740	X8	KDC8	KX8	K12H	KGLH
66a	**K4H**	K740	X8	KDC8	KX8	K13H	KGLH
67a	**K5H**	K740	X8	KDC8	KX8	K14H	KGLH
68a	**K6H**	K740	X8	KDC8	KX8	K15H	KGLH
69a	**K7H**	K740	X8	KDC8	KX8	K16H	KGLH
70a	**K8H**	K740	X8	KDC8	KX8	K17H	KGLH
71a	**K9H**	K740	X8	KDC8	KX8	K18H	KGLH
Page B							
0b	**K1A**	K733	X1	KDC1	KX1	K10A	KGLA
1b	**K2A**	K733	X1	KDC1	KX1	K11A	KGLA
2b	**K3A**	K733	X1	KDC1	KX1	K12A	KGLA
3b	**K4A**	K733	X1	KDC1	KX1	K13A	KGLA
4b	**K5A**	K733	X1	KDC1	KX1	K14A	KGLA
5b	**K6A**	K733	X1	KDC1	KX1	K15A	KGLA
6b	**K7A**	K733	X1	KDC1	KX1	K16A	KGLA
7b	**K8A**	K733	X1	KDC1	KX1	K17A	KGLA
8b	**K9A**	K733	X1	KDC1	KX1	K18A	KGLA
9b	**K1B**	K734	X2	KDC2	KX2	K10B	KGLB
10b	**K2B**	K734	X2	KDC2	KX2	K11B	KGLB
11b	**K3B**	K734	X2	KDC2	KX2	K12B	KGLB
12b	**K4B**	K734	X2	KDC2	KX2	K13B	KGLB
13b	**K5B**	K734	X2	KDC2	KX2	K14B	KGLB
14b	**K6B**	K734	X2	KDC2	KX2	K15B	KGLB

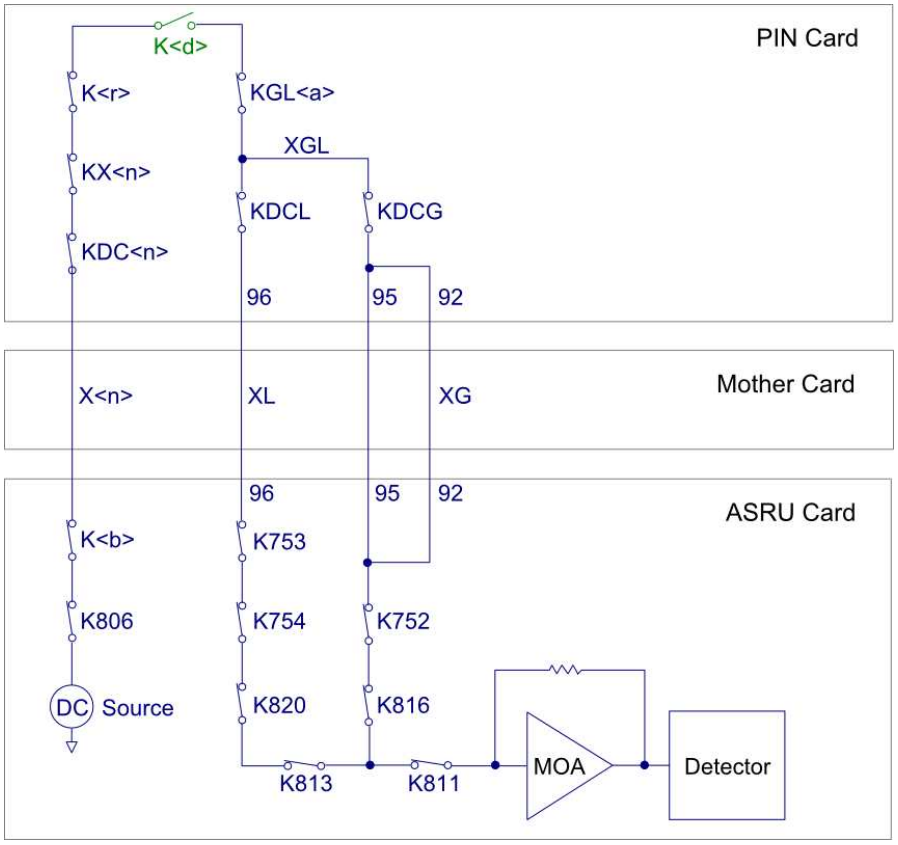
Table 5-27

Subtest	K<d>	K<b>	X<n>	KDC<n>	KX<n>	K<r>	KGL<a>
15b	**K7B**	K734	X2	KDC2	KX2	K16B	KGLB
16b	**K8B**	K734	X2	KDC2	KX2	K17B	KGLB
17b	**K9B**	K734	X2	KDC2	KX2	K18B	KGLB
18b	**K1C**	K735	X3	KDC3	KX3	K10C	KGLC
19b	**K2C**	K735	X3	KDC3	KX3	K11C	KGLC
20b	**K3C**	K735	X3	KDC3	KX3	K12C	KGLC
21b	**K4C**	K735	X3	KDC3	KX3	K13C	KGLC
22b	**K5C**	K735	X3	KDC3	KX3	K14C	KGLC
23b	**K6C**	K735	X3	KDC3	KX3	K15C	KGLC
24b	**K7C**	K735	X3	KDC3	KX3	K16C	KGLC
25b	**K8C**	K735	X3	KDC3	KX3	K17C	KGLC
26b	**K9C**	K735	X3	KDC3	KX3	K18C	KGLC
27b	**K1D**	K736	X4	KDC4	KX4	K10D	KGLD
28b	**K2D**	K736	X4	KDC4	KX4	K11D	KGLD
29b	**K3D**	K736	X4	KDC4	KX4	K12D	KGLD
30b	**K4D**	K736	X4	KDC4	KX4	K13D	KGLD
31b	**K5D**	K736	X4	KDC4	KX4	K14D	KGLD
32b	**K6D**	K736	X4	KDC4	KX4	K15D	KGLD
33b	**K7D**	K736	X4	KDC4	KX4	K16D	KGLD
34b	**K8D**	K736	X4	KDC4	KX4	K17D	KGLD
35b	**K9D**	K736	X4	KDC4	KX4	K18D	KGLD
36b	**K1E**	K737	X5	KDC5	KX5	K10E	KGLE
37b	**K2E**	K737	X5	KDC5	KX5	K11E	KGLE
38b	**K3E**	K737	X5	KDC5	KX5	K12E	KGLE
39b	**K4E**	K737	X5	KDC5	KX5	K13E	KGLE
40b	**K5E**	K737	X5	KDC5	KX5	K14E	KGLE
41b	**K6E**	K737	X5	KDC5	KX5	K15E	KGLE
42b	**K7E**	K737	X5	KDC5	KX5	K16E	KGLE
43b	**K8E**	K737	X5	KDC5	KX5	K17E	KGLE
44b	**K9E**	K737	X5	KDC5	KX5	K18E	KGLE

Table 5-27

Subtest	K<d>	K<b>	X<n>	KDC<n>	KX<n>	K<r>	KGL<a>
45b	**K1F**	K738	X6	KDC6	KX6	K10F	KGLF
46b	**K2F**	K738	X6	KDC6	KX6	K11F	KGLF
47b	**K3F**	K738	X6	KDC6	KX6	K12F	KGLF
48b	**K4F**	K738	X6	KDC6	KX6	K13F	KGLF
49b	**K5F**	K738	X6	KDC6	KX6	K14F	KGLF
50b	**K6F**	K738	X6	KDC6	KX6	K15F	KGLF
51b	**K7F**	K738	X6	KDC6	KX6	K16F	KGLF
52b	**K8F**	K738	X6	KDC6	KX6	K17F	KGLF
53b	**K9F**	K738	X6	KDC6	KX6	K18F	KGLF
54b	**K1G**	K739	X7	KDC7	KX7	K10G	KGLG
55b	**K2G**	K739	X7	KDC7	KX7	K11G	KGLG
56b	**K3G**	K739	X7	KDC7	KX7	K12G	KGLG
57b	**K4G**	K739	X7	KDC7	KX7	K13G	KGLG
58b	**K5G**	K739	X7	KDC7	KX7	K14G	KGLG
59b	**K6G**	K739	X7	KDC7	KX7	K15G	KGLG
60b	**K7G**	K739	X7	KDC7	KX7	K16G	KGLG
61b	**K8G**	K739	X7	KDC7	KX7	K17G	KGLG
62b	**K9G**	K739	X7	KDC7	KX7	K18G	KGLG
63b	**K1H**	K740	X8	KDC8	KX8	K10H	KGLH
64b	**K2H**	K740	X8	KDC8	KX8	K11H	KGLH
65b	**K3H**	K740	X8	KDC8	KX8	K12H	KGLH
66b	**K4H**	K740	X8	KDC8	KX8	K13H	KGLH
67b	**K5H**	K740	X8	KDC8	KX8	K14H	KGLH
68b	**K6H**	K740	X8	KDC8	KX8	K15H	KGLH
69b	**K7H**	K740	X8	KDC8	KX8	K16H	KGLH
70b	**K8H**	K740	X8	KDC8	KX8	K17H	KGLH
71b	**K9H**	K740	X8	KDC8	KX8	K18H	KGLH

Figure 5-17 T3360



Test 3370

Test Receiver Channel Relays can be Opened

This test verifies that relays KRA through KRH can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3370 sets the receiver references (RHI and RLO) to +2.0 and -2.0 volts, enables the receiver's pull-up, opens the relay, and then measures the receiver's input level. A 10-kohm path to ground ensures that the test will pass if the path is open; it eliminates the possibility of a drift value.

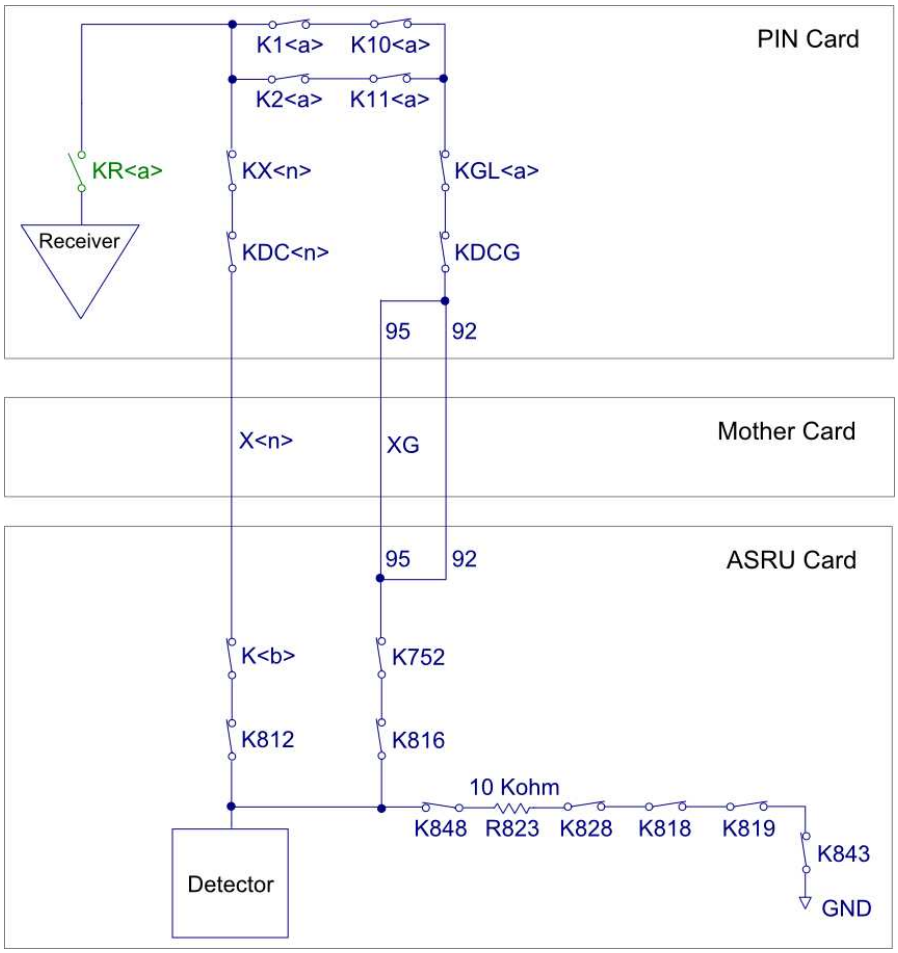
Test 3370 requires the proper operation of X-bus, X-bus disconnect, XGL-bus, and fixture interface (MINT) pin relays.

Figure 5-18 shows the measurement path.

Table 5-28

Subtest	KR<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-18 T3370



Test 3372

Test Receiver to Driver Sense Connect Relays can be Opened

This test verifies the K<x>C relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

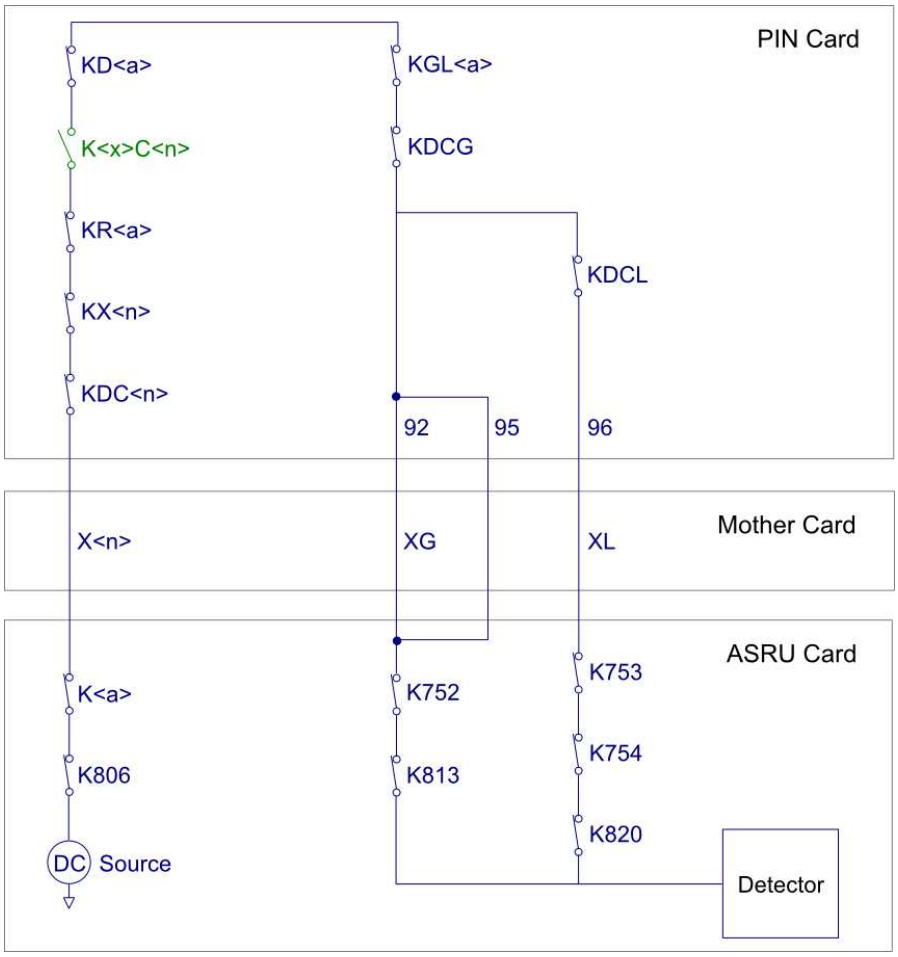
This test can be executed with or without the Pin Verification Fixture. Requires proper operation of: ASRU, Disconnect relays, X-bus relays, Driver relays, Receiver relays.

Figure 5-19 shows the measurement path. It tests the same path as Test 3272.

Table 5-29

Subtest	K<x>C<n>	K<n>	KDC<n>	KX<n>	KR<n>	KD<n>	KGL<n>
Page A							
0a	**KAC0**	K733	KDC1	KX1	KRA	KDA	KGLA
1a	**KAC1**	K734	KDC2	KX2	KRB	KDB	KGLB
2a	**KAC2**	K735	KDC3	KX3	KRC	KDC	KGLC
3a	**KAC3**	K746	KDC4	KX4	KRD	KDD	KGLD
4a	**KAC4**	K737	KDC5	KX5	KRE	KDE	KGLE
5a	**KAC5**	K738	KDC6	KX6	KRF	KDF	KGLF
6a	**KAC6**	K739	KDC7	KX7	KRG	KDG	KGLG
7a	**KAC7**	K740	KDC8	KX8	KRH	KDH	KGLH
Page B							
0b	**KBC0**	K733	KDC1	KX1	KRA	KDA	KGLA
1b	**KBC1**	K734	KDC2	KX2	KRB	KDB	KGLB
2b	**KBC2**	K735	KDC3	KX3	KRC	KDC	KGLC
3b	**KBC3**	K746	KDC4	KX4	KRD	KDD	KGLD
4b	**KBC4**	K737	KDC5	KX5	KRE	KDE	KGLE
5b	**KBC5**	K738	KDC6	KX6	KRF	KDF	KGLF
6b	**KBC6**	K739	KDC7	KX7	KRG	KDG	KGLG
7b	**KBC7**	K740	KDC8	KX8	KRH	KDH	KGLH

Figure 5-19 T3372



Test 3374

Test Driver to XL-Bus Connect Relays can be Opened

This test verifies the K<x>X relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

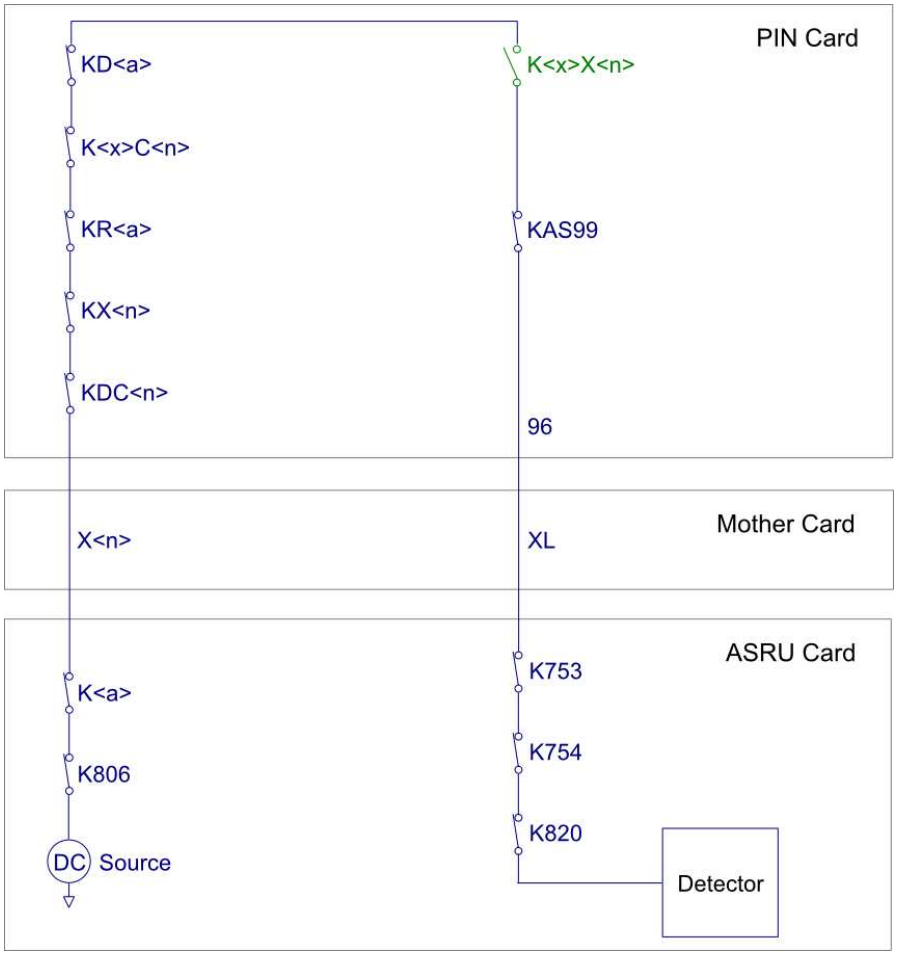
This test can be executed with or without the Pin Verification Fixture.

Figure 5-20 shows the measurement path.

Table 5-30

Subtest	K<x>X<n>9	K<a>	KDC<n>	KX<n>	KR<n>	K<x>C<n>	KD<n>
Page A							
0a	**KAX09**	K733	KDC1	KX1	KRA	KAC0	KDA
1a	**KAX19**	K734	KDC2	KX2	KRB	KAC1	KDB
2a	**KAX29**	K735	KDC3	KX3	KRC	KAC2	KDC
3a	**KAX39**	K746	KDC4	KX4	KRD	KAC3	KDD
4a	**KAX49**	K737	KDC5	KX5	KRE	KAC4	KDE
5a	**KAX59**	K738	KDC6	KX6	KRF	KAC5	KDF
6a	**KAX69**	K739	KDC7	KX7	KRG	KAC6	KDG
7a	**KAX79**	K740	KDC8	KX8	KRH	KAC7	KDH
Page B							
0b	**KBX09**	K733	KDC1	KX1	KRA	KBC0	KDA
1b	**KBX19**	K734	KDC2	KX2	KRB	KBC1	KDB
2b	**KBX29**	K735	KDC3	KX3	KRC	KBC2	KDC
3b	**KBX39**	K746	KDC4	KX4	KRD	KBC3	KDD
4b	**KBX49**	K737	KDC5	KX5	KRE	KBC4	KDE
5b	**KBX59**	K738	KDC6	KX6	KRF	KBC5	KDF
6b	**KBX69**	K739	KDC7	KX7	KRG	KBC6	KDG
7b	**KBX79**	K740	KDC8	KX8	KRH	KBC7	KDH

Figure 5-20 T3374



Test 3376

Test X-Bus Disconnect Relays can be Opened

This test verifies the K<x>S relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

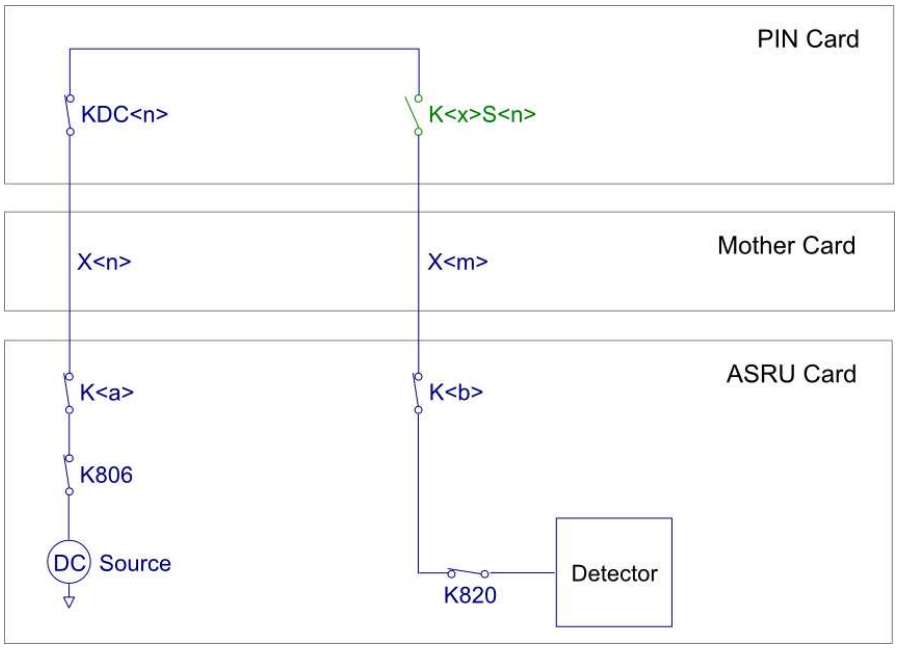
This test can be executed with or without the Pin Verification Fixture.A pair of disconnect relays create a path in and out of the Pin card. One X-bus pin is connected to the ASRU source via the S-bus, another X-bus pin is connected to the ASRU detector (via the L-bus), and a resistor measurement performed.

Figure 5-21 shows the measurement path. It uses the same test path as Test 3276.

Table 5-31

Subtest	KDC<n>	KAS<n>	K<a>	K<b>
Page A				
0a	KDC1	**KAS31**	K733	K719
1a	KDC2	**KAS42**	K734	K720
2a	KDC3	**KAS53**	K735	K721
3a	KDC4	**KAS64**	K736	K722
4a	KDC5	**KAS75**	K737	K723
5a	KDC6	**KAS86**	K738	K724
6a	KDC7	**KAS17**	K739	K717
7a	KDC8	**KAS28**	K740	K718
Page B				
0b	KDC1	**KBS31**	K733	K719
1b	KDC2	**KBS42**	K734	K720
2b	KDC3	**KBS53**	K735	K721
3b	KDC4	**KBS64**	K736	K722
4b	KDC5	**KBS75**	K737	K723
5b	KDC6	**KBS86**	K738	K724
6b	KDC7	**KBS17**	K739	K717
7b	KDC8	**KBS28**	K740	K718

Figure 5-21 T3376



Test 3378

Test Ground-Bounce Relays can be Opened

Requires: Double-density pin card

This test verifies that the KBV<n> relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

This test can be executed with or without the Pin Verification Fixture. It requires the proper operation of: ASRU, Disconnect relays, X-bus relays, and Channel MUX relays. The signal path is the same as in Test 3278, but it tests for 5 Vdc because KBV<n> is open.

Figure 5-22 shows the measurement path.

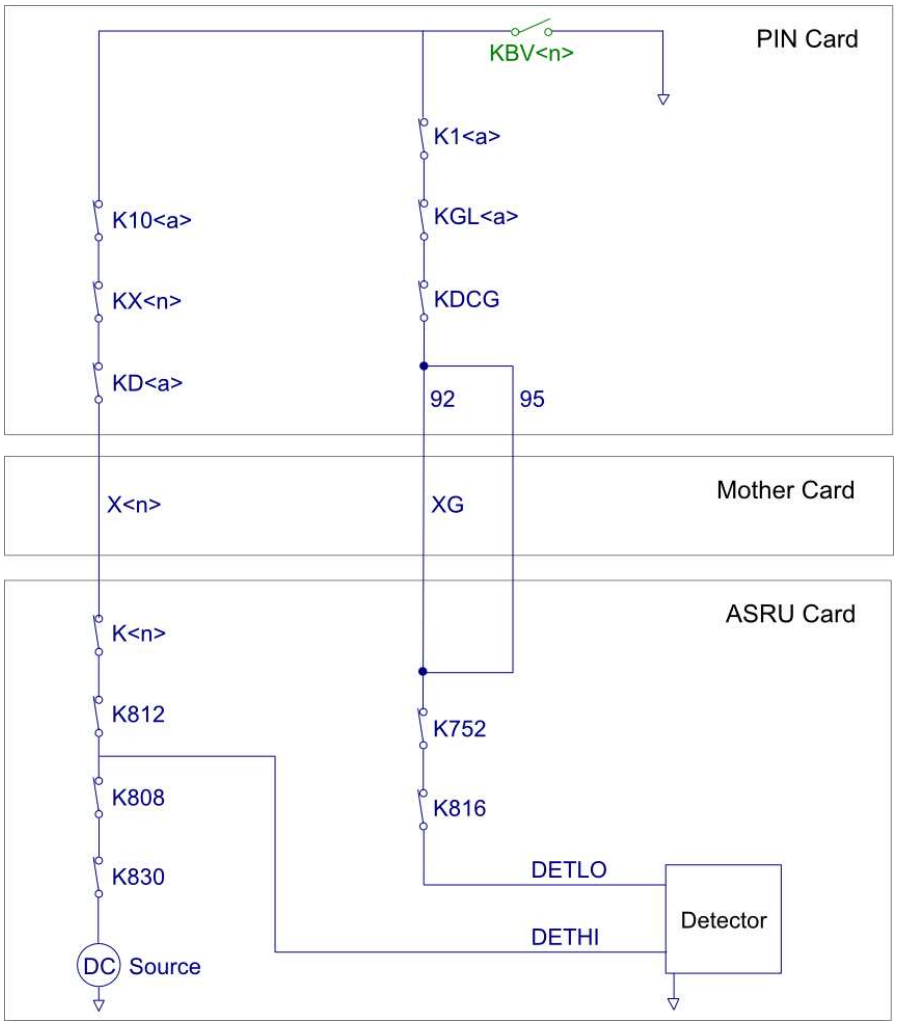
Table 5-32

Subtest	KBV<n>	K1<n>	K10<n>	KX<n>	KGL<n>	KD<n>	K<n>
Page B							
0	**KBV11**	K1B	K10B	KX2	KGLB	KDC2	K726
1	**KBV12**	K2B	K11B	KX2	KGLB	KDC2	K726
2	**KBV13**	K3B	K12B	KX2	KGLB	KDC2	K726
3	**KBV14**	K4B	K13B	KX2	KGLB	KDC2	K726
4	**KBV15**	K5B	K14B	KX2	KGLB	KDC2	K726
5	**KBV16**	K6B	K15B	KX2	KGLB	KDC2	K726
6	**KBV17**	K7B	K16B	KX2	KGLB	KDC2	K726
7	**KBV18**	K8B	K17B	KX2	KGLB	KDC2	K726
8	**KBV19**	K9B	K18B	KX2	KGLB	KDC2	K726
9	**KBV31**	K1D	K10D	KX4	KGLD	KDC4	K728
10	**KBV32**	K2D	K11D	KX4	KGLD	KDC4	K728
11	**KBV33**	K3D	K12D	KX4	KGLD	KDC4	K728
12	**KBV34**	K4D	K13D	KX4	KGLD	KDC4	K728
13	**KBV35**	K5D	K14D	KX4	KGLD	KDC4	K728
14	**KBV36**	K6D	K15D	KX4	KGLD	KDC4	L728
15	**KBV37**	K7D	K16D	KX4	KGLD	KDC4	K728
16	**KBV38**	K8D	K17D	KX4	KGLD	KDC4	K728
17	**KBV39**	K9D	K18D	KX4	KGLD	KDC4	K728
18	**KBV41**	K1E	K10E	KX5	KGLE	KDC5	K729
19	**KBV42**	K2E	K11E	KX5	KGLE	KDC5	K729
20	**KBV43**	K3E	K12E	KX5	KGLE	KDC5	K729
21	**KBV44**	K4E	K13E	KX5	KGLE	KDC5	K729
22	**KBV45**	K5E	K14E	KX5	KGLE	KDC5	K729
23	**KBV46**	K6E	K15E	KX5	KGLE	KDC5	K729
24	**KBV47**	K7E	K16E	KX5	KGLE	KDC5	K729
25	**KBV48**	K8E	K17E	KX5	KGLE	KDC5	K729
26	**KBV49**	K9E	K18E	KX5	KGLE	KDC5	K729
27	**KBV61**	K1G	K10G	KX7	KGLG	KDC7	K731

Table 5-32

Subtest	KBV<n>	K1<n>	K10<n>	KX<n>	KGL<n>	KD<n>	K<n>
28	**KBV62**	K2G	K11G	KX7	KGLG	KDC7	K731
29	**KBV63**	K3G	K12G	KX7	KGLG	KDC7	K731
30	**KBV64**	K4G	K13G	KX7	KGLG	KDC7	K731
31	**KBV65**	K5G	K14G	KX7	KGLG	KDC7	K731
32	**KBV66**	K6G	K15G	KX7	KGLG	KDC7	K731
33	**KBV67**	K7G	K16G	KX7	KGLG	KDC7	K731
34	**KBV68**	K8G	K17G	KX7	KGLG	KDC7	K731
35	**KBV69**	K9G	K18G	KX7	KGLG	KDC7	K731

Figure 5-22 T3378



Test 3380

Test Driver Channel Relays can be Opened

This test verifies that K<x>P0 through K<x>P7 can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3380 sets the driver high (DHI = +3.5 volts and DLO = -3.5 volts), opens the driver channel relay, and then measures the driver output level. A 10-kohm path to ground ensures that the test will fail if the path is open; it eliminates the possibility of a drift value.

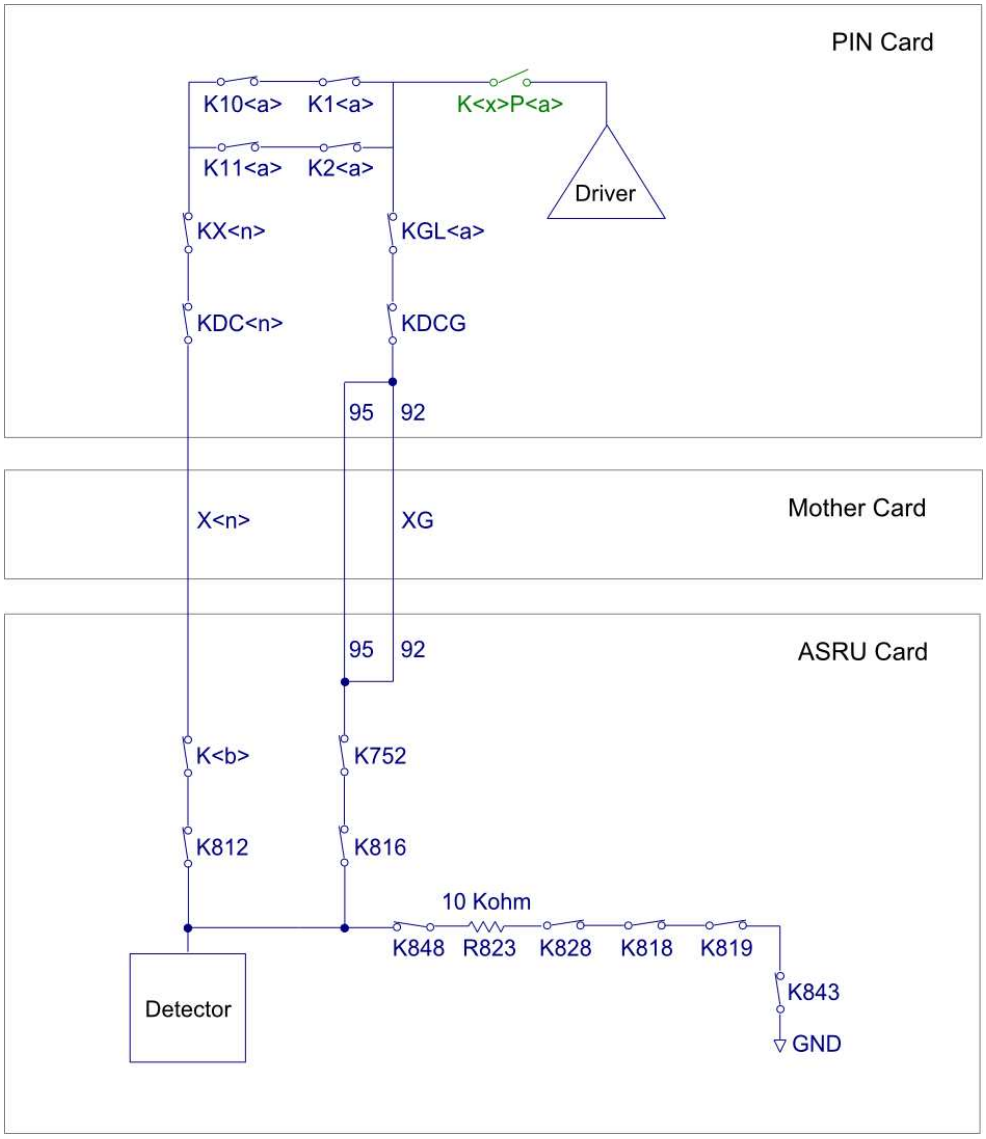
Test 3380 requires the proper operation of X-bus, X-bus disconnect, XGL-bus, and fixture interface (MINT) pin relays.

Figure 5-23 shows the measurement path.

Table 5-33

Subtest	K<x>P<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KAP0**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KAP1**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KAP2**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KAP3**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KAP4**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KAP5**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KAP6**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KAP7**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KBP0**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KBP1**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KBP2**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KBP3**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KBP4**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KBP5**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KBP6**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KBP7**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-23 T3380



Test 3390

Relay Buzz Test[1]

NOTE This test is not run during normal diagnostics. It must be executed by **Test Number Entry**.

This test measures the path resistance to find relays whose contact resistance has gradually increased (as happens with a cracked relay capsule).If this test is performed without the Diagnostic fixture in place, then failure can be localized only to either the KGL or the driver relay. See Figure 5-24, Figure 5-25, Figure 5-26, and Figure 5-27 for test paths.

1. The Mux system system uses reed relays for switching. When reed relays are switched under power, they are self-cleaning; if not, they tend to pick up increasing resistance at the contact points. The buzz test rapidly cycles the relays to be tested in order to clean the contact points (hence the buzzing sound during test), and then takes a resistance measurement.

Table 5-34

Subtest	Description
Page A	
0a-7a	KDC1/KX1 through KDC8/KX8
8a	KDCG
9a	KDCL
10a-18a	K10A/K1A through K18A/K9A
19a-27a	K10B/K1B through K18B/K9B
28a-36a	K10C/K1C through K18C/K9C
37a-45a	K10D/K1D through K18D/K9D
46a-54a	K10E/K1E through K18E/K9E
55a-63a	K10F/K1F through K18F/K9F
64a-72a	K10G/K1G through K18G/K9G
73a-81a	K10H/K1H through K18H/K9H
82a-89a	KDA through KDH
Page B	
0b-7b	KDC1/KX1 through KDC8/KX8
8b	KDCG
9b	KDGL
10b-18b	K10A/K1A through K18A/K9A

Table 5-34

Subtest	Description
19b-27b	K10B/K1B through K18B/K9B
28b-36b	K10C/K1C through K18C/K9C
37b-45b	K10D/K1D through K18D/K9D
46b-54b	K10E/K1E through K18E/K9E
55b-63b	K10F/K1F through K18F/K9F
64b-72b	K10G/K1G through K18G/K9G
73b-81b	K10H/K1H through K18H/K9H
82b-89b	KDA through KDH

Figure 5-24 T3390 (subtests 0-7)

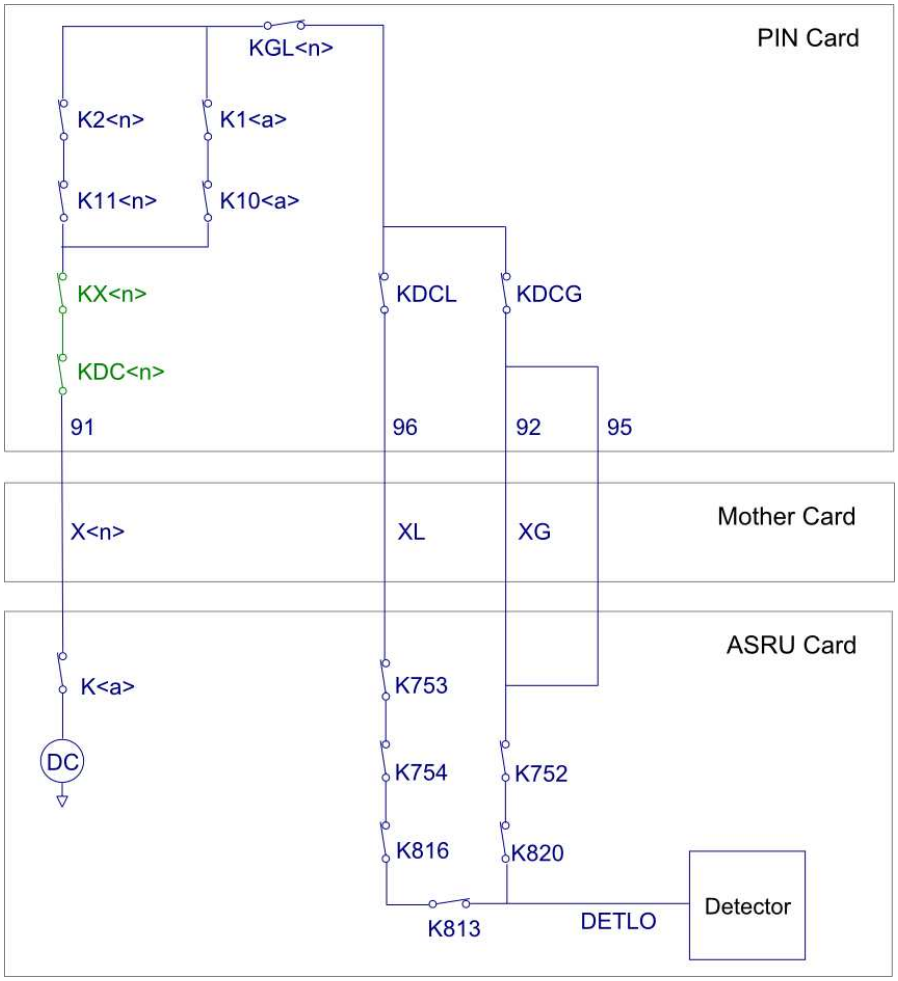


Figure 5-25 T3390 (subtests 8)

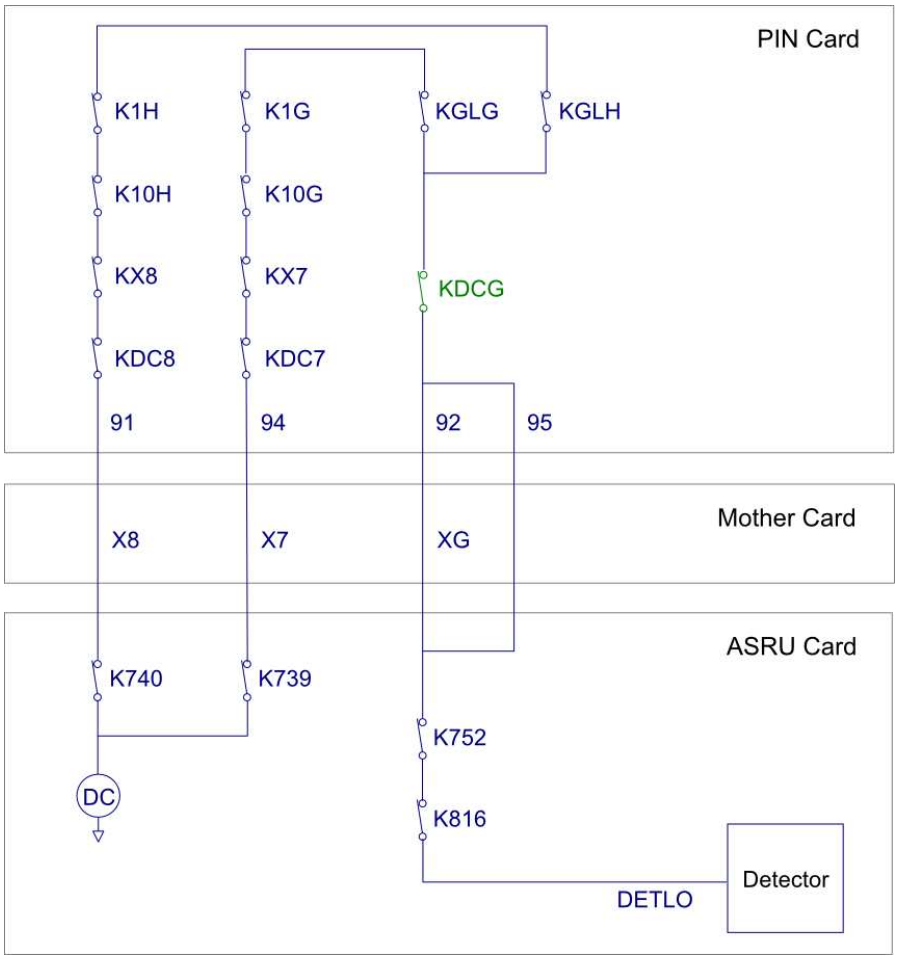


Figure 5-26 T3390 (subtests 9)

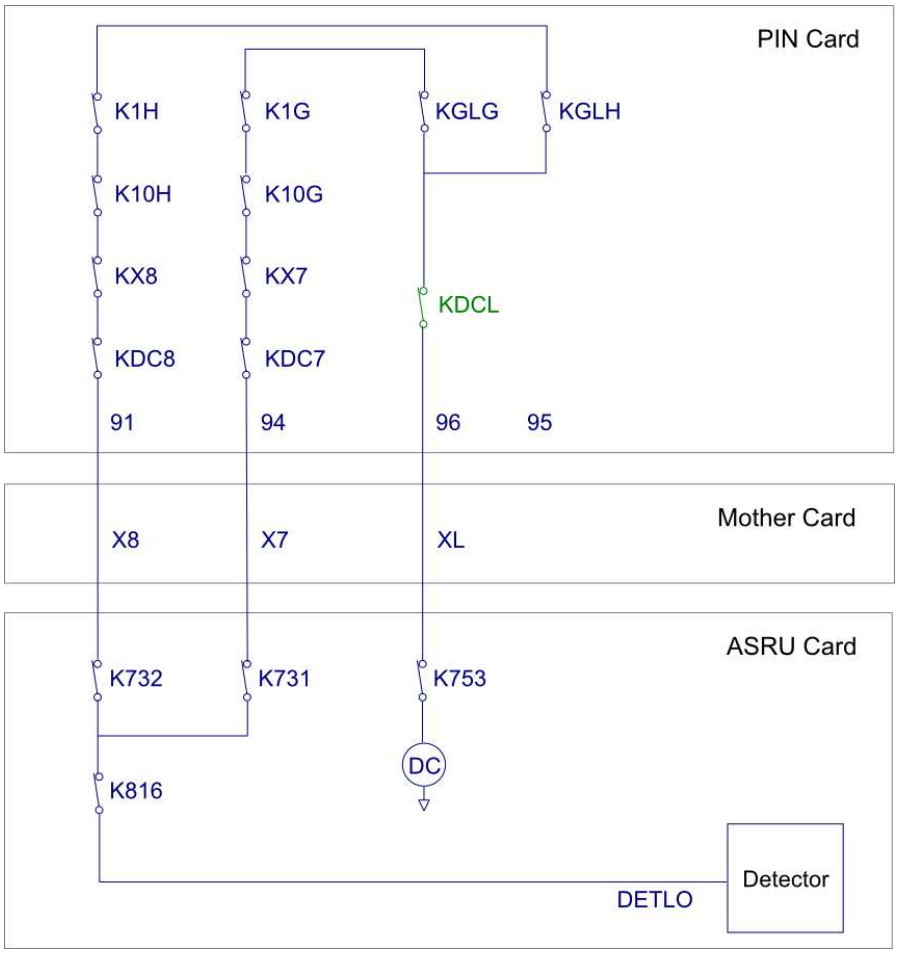
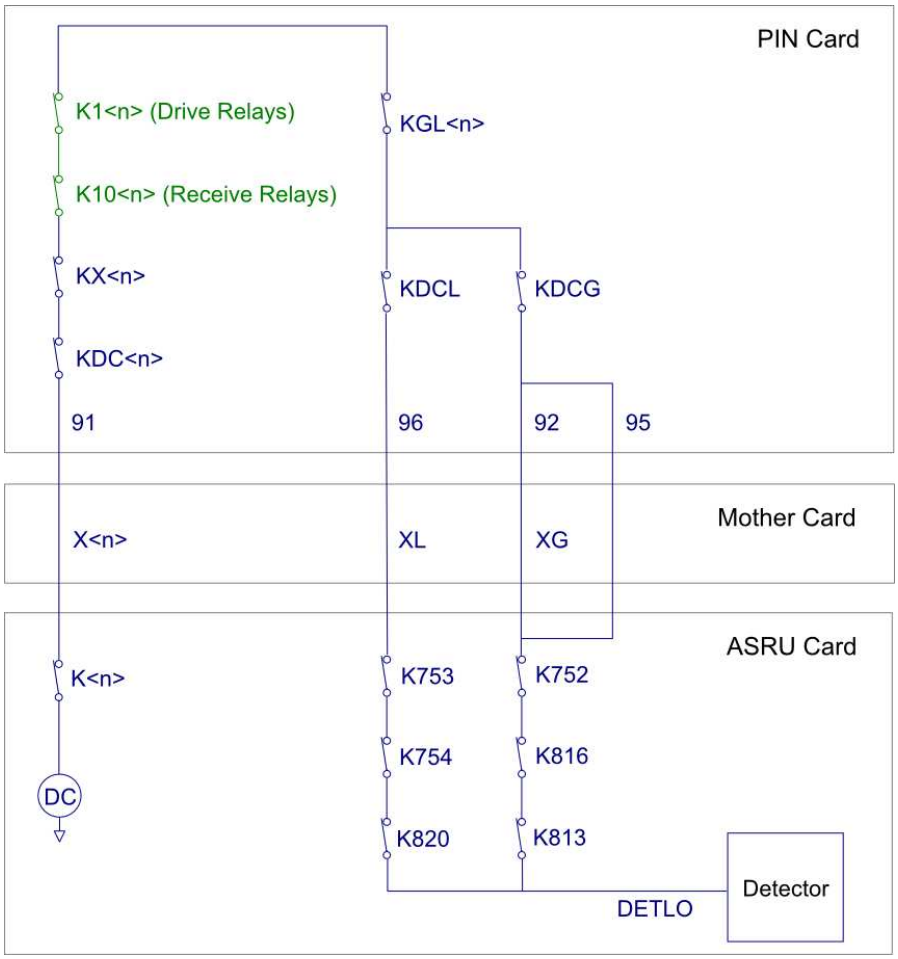


Figure 5-27 T3390 (subtests 10-89)



Test 3395

Test Driver Relay Coils Shorted Together

NOTE This test is not run during normal diagnostics. It must be executed by **Test Number Entry**.

This test is designed to determine if any of driver relay coils are shorted together by defective relay drivers.

If this test fails without the Pin Verification Fixture in place, the fault can be localized only to either the driver relay or KGL. See Figure 5-28, Figure 5-29, Figure 5-30, and Figure 5-31 that show the test paths.

Table 5-35

Subtest	Description
Page A	**Page A**
0a-8a	Checks K10A through K18A
9a-17a	Checks K10B through K18B
18a-26a	Checks K10C through K18C
27a-35a	Checks K10D through K18D
36a-44a	Checks K10E through K18E
45a-53a	Checks K10F through K18F
54a-62a	Checks K10G through K18G
63a-71a	Checks K10H through K18H
72a-79a	Checks KGLA (Closed) and KDC1/KX1 (Open) through KGLH and KDC8/KX8
80a	Checks KDC and KX
81a	Checks KDCG and KDCL
Page B	**Page B**
0b-8b	Checks K10A through K18A
9b-17b	Checks K10B through K18B
18b-26b	Checks K10C through K18C
27b-35b	Checks K10D through K18D
36b-44b	Checks K10E through K18E
45b-53b	Checks K10F through K18F
54b-62b	Checks K10G through K18G
63b-71b	Checks K10H through K18H
72b-79b	Checks KGLA (Closed) and KDC1/KX1 (Open) through KGLH and KDC8/KX8
80b	Checks KDC and KX
81b	Checks KDCG and KDCL

Figure 5-28 T3395 (subtests 0-71)

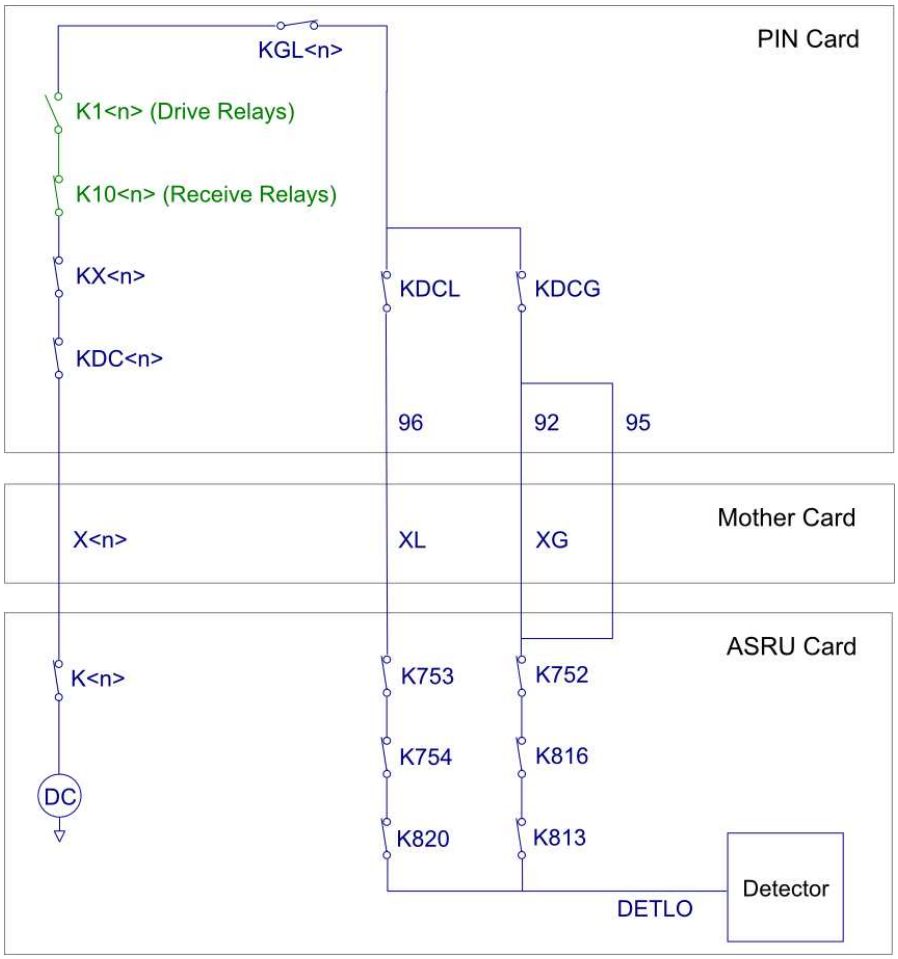


Figure 5-29 T3395 (subtests 72-79)

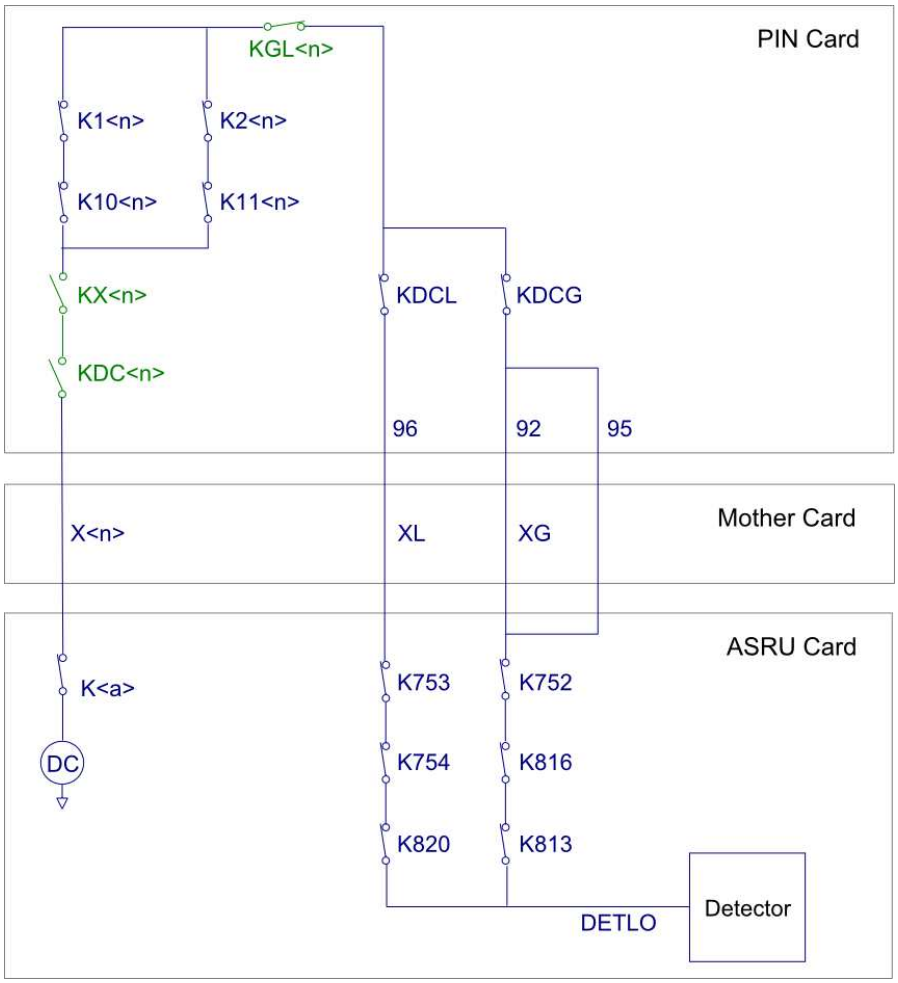


Figure 5-30 T3395 (subtests 80)

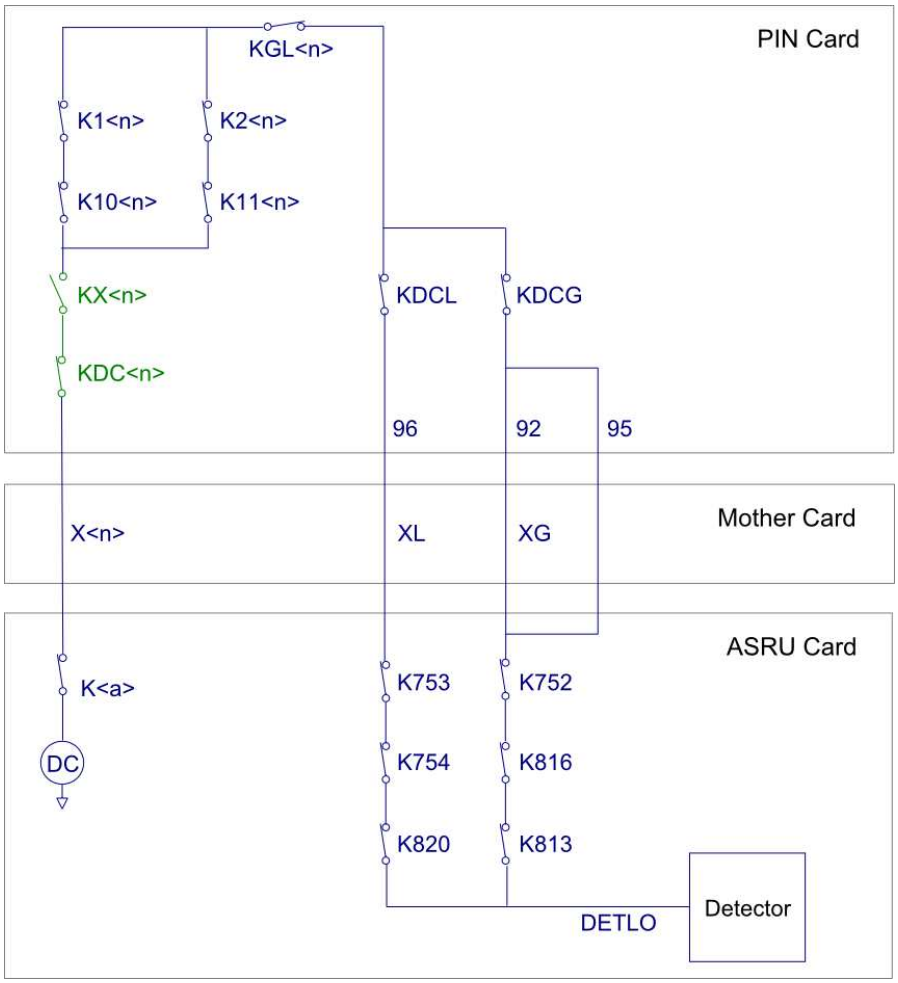
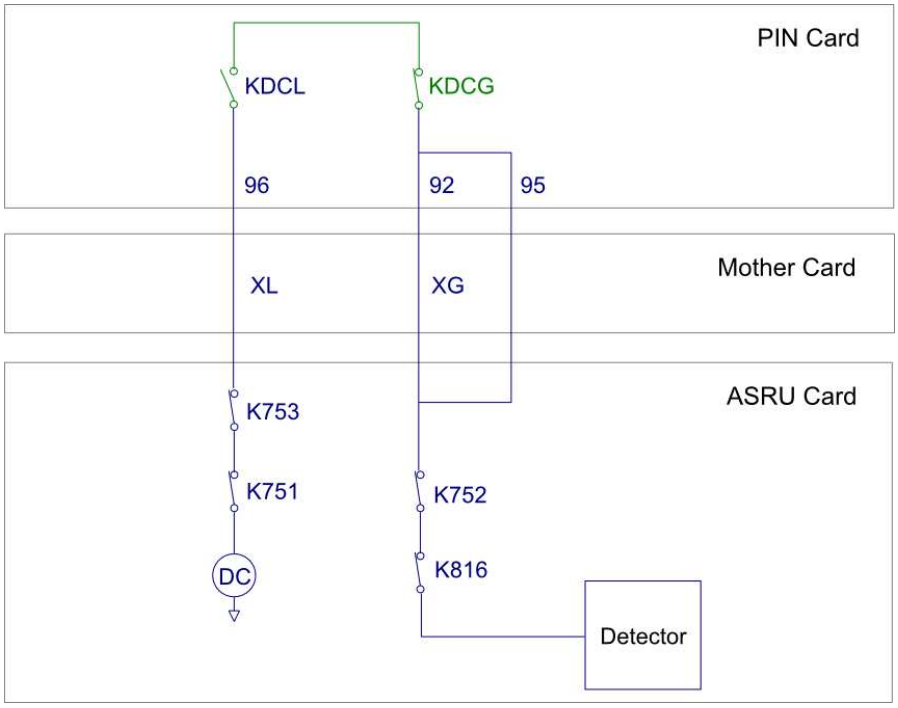


Figure 5-31 T3395 (subtests 0-81)



Test 3397

Test Receiver Channel Relays can be Opened (AnalogPlus Pin Card ONLY)

This test verifies KRA through KRH can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3397 uses the ASRU source and detector to determine if a relay is stuck closed. A 10-kohm path to ground ensures that the test will pass if the path is open; it eliminates the possibility of a drift value that fails.

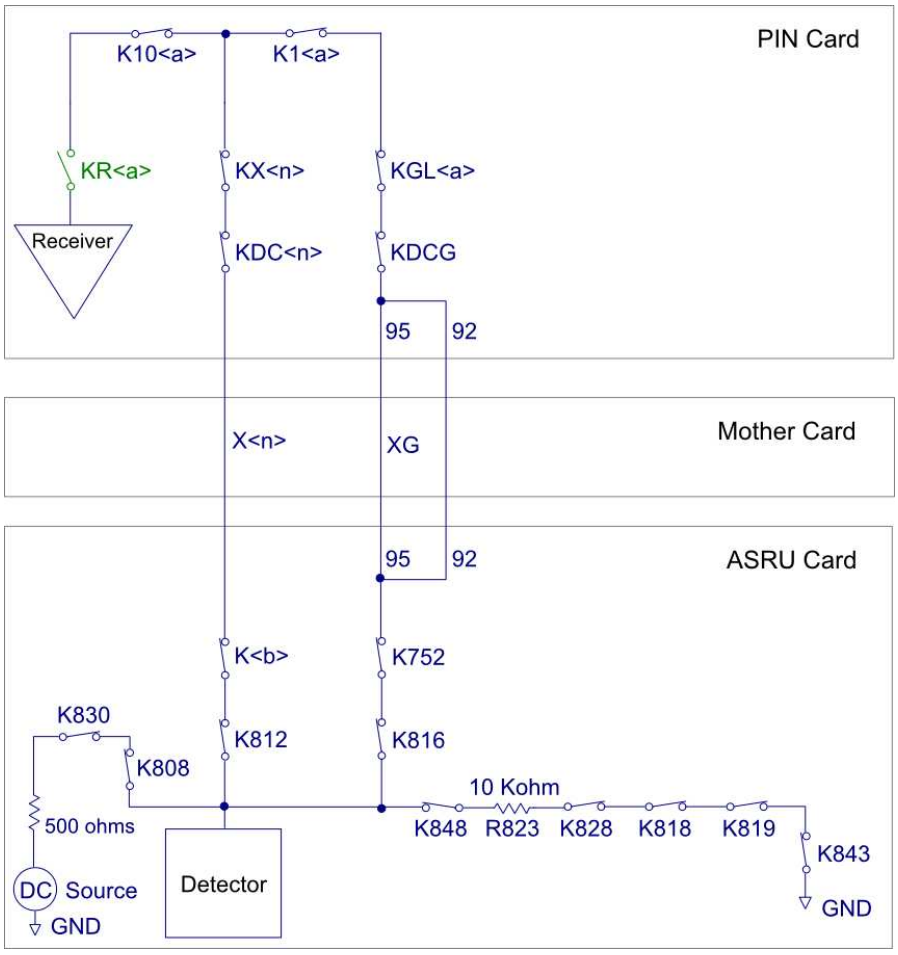
Test 3397 requires the proper operation of X-bus, X-bus disconnect, XGL-bus, and fixture interface (MINT) pin relays.

Figure 5-32 shows the measurement path.

Table 5-36

Subtest	KR<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KRA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KRB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KRC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KRD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KRE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KRF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KRG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KRH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-32 T3397



Test 3399

Test Driver Channel Relays can be opened (AnalogPlus Pin Card ONLY)

This test verifies KDA through KDH can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

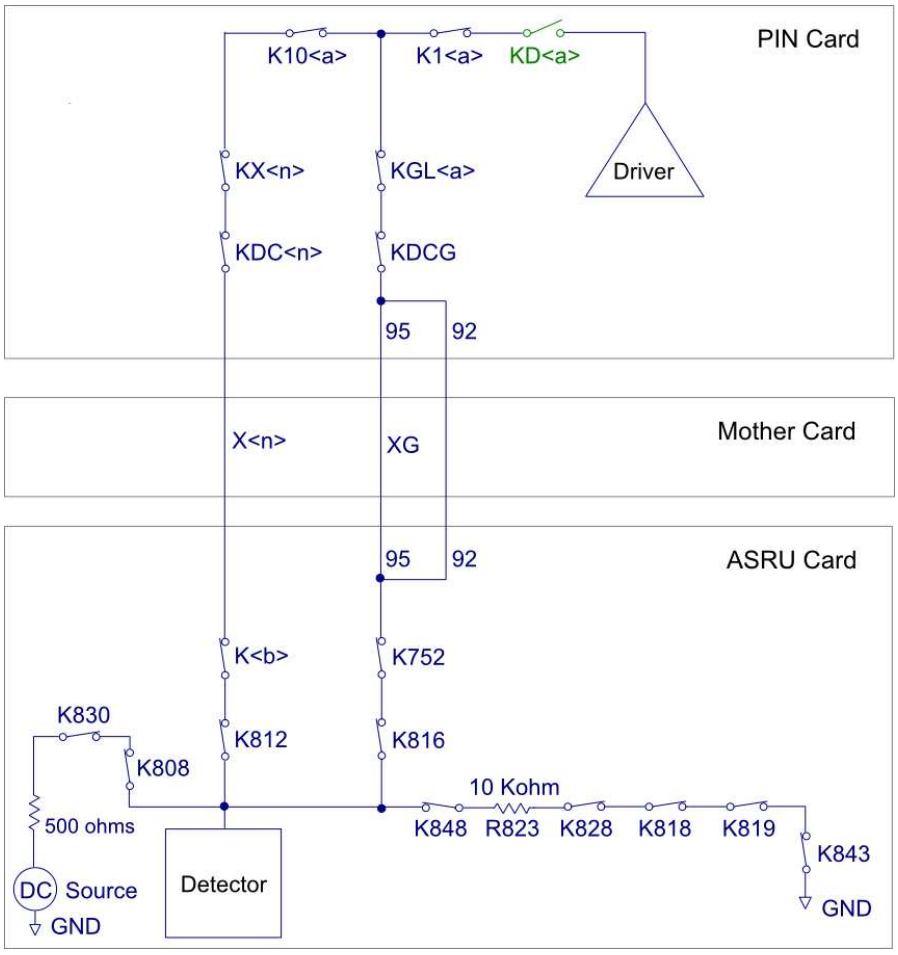
Test 3399 uses the ASRU source and detector to determine if a relay is stuck closed. A 10-kohm path to ground ensures that the test will pass if the path is open; it eliminates the possibility of a drift value that passes.

Test 3399 requires the proper operation of X-bus, X-bus disconnect, XGL-bus, and fixture interface (MINT) pin relays. Figure 5-33 shows the measurement path.

Table 5-37

Subtest	KD<a>	K<b>	KGL<a>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>
Page A									
0a	**KDA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1a	**KDB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2a	**KDC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3a	**KDD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4a	**KDE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5a	**KDF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6a	**KDG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7a	**KDH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H
Page B									
0b	**KDA**	K725	KGLA	KDC1	KX1	K1A	K2A	K10A	K11A
1b	**KDB**	K726	KGLB	KDC2	KX2	K1B	K2B	K10B	K11B
2b	**KDC**	K727	KGLC	KDC3	KX3	K1C	K2C	K10C	K11C
3b	**KDD**	K728	KGLD	KDC4	KX4	K1D	K2D	K10D	K11D
4b	**KDE**	K729	KGLE	KDC5	KX5	K1E	K2E	K10E	K11E
5b	**KDF**	K730	KGLF	KDC6	KX6	K1F	K2F	K10F	K11F
6b	**KDG**	K731	KGLG	KDC7	KX7	K1G	K2G	K10G	K11G
7b	**KDH**	K732	KGLH	KDC8	KX8	K1H	K2H	K10H	K11H

Figure 5-33 T3399



Format Chip

Test 3410

Verify Driver Data from ADRV and Format Chip

This test verifies that the format chip can drive and receive data on each channel.

Subtests 0 to 127 are grouped in eight sections (eight channels) of 16. Of the 16 subtests for each channel, eight use the ADRV0 and ADRV1 lines from the Module Control Card to set driver data on the Pin Card; the other eight use data from the format chip's flip-flops, FF1 and FF2. After driving the data, each subtest reads 1's and 0's from the receiver GTL and GTH lines. The receiver data are returned to the Module Control Card via the ARCV0 line.

Test 3410 runs 16 types of subtests, affecting eight channels. Each subtest type repeats every 16 subtests. Given the following table and the description of the first 16 subtests, you can determine the function and channel for any subtest.

For example, Table 5-38 shows that subtest 67 affects driver channel E. You can figure subtest 67's function by dividing the subtest number by 16 (recall each subtest type repeats every 16 subtests); the remainder of the division is the subtest type:
67/16 = 4, remainder = 3

Subtest 67, like subtest 3, sends a 0 from ADRV0 and checks the receiver GTL line.

Table 5-38 T3410 subtest driver channels

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a-15a	16a-31a	32a-47a	48a-63a	64a-79a	80a-95a	96a-111a	112a-127a
Page B							
0b-15b	16b-31b	32b-47b	48b-63b	64b-79b	80b-95b	96b-111b	112b-127b

Table 5-39

Subtest	Function
0	Send a 1 from ADRV0 and check receiver GTH data: Channel <c>
1	Send a 1 from ADRV0 and check receiver GTL data: Channel <c>
2	Send a 0 from ADRV0 and check receiver GTH data: Channel <c>
3	Send a 0 from ADRV0 and check receiver GTL data: Channel <c>
4	Send a 1 from ADRV1 and check receiver GTH data: Channel <c>
5	Send a 1 from ADRV1 and check receiver GTL data: Channel <c>
6	Send a 0 from ADRV1 and check receiver GTH data: Channel <c>
7	Send a 0 from ADRV1 and check receiver GTL data: Channel <c>
8	Send a 1 from FF1 and check receiver GTH data: Channel <c>
9	Send a 1 from FF1 and check receiver GTL data: Channel <c>
10	Send a 0 from FF1 and check receiver GTH data: Channel <c>
11	Send a 0 from FF1 and check receiver GTL data: Channel <c>
12	Send a 1 from FF2 and check receiver GTH data: Channel <c>
13	Send a 1 from FF2 and check receiver GTL data: Channel <c>
14	Send a 0 from FF2 and check receiver GTH data: Channel <c>
15	Send a 0 from FF2 and check receiver GTL data: Channel <c>

Test 3411

Verify Driver Three-State from ADRV, Format Chip, or CPU

This test checks the ability to three-state the drivers.

Subtests 0 through 79 are grouped in eight sections (eight channels) of 10. Each group of subtests tests the three-stating of the drivers by five methods. The first two subtests verify the three-stating via the ADRV0 line from Module Control Card. The next two subtests verify three-stating via ADRV1. The third and fourth pairs of subtests verify three-stating via the format chip's three-state flip-flops. The fifth pair verifies the master three-state (MTSP) set by the Module Control Card.

All the odd subtests read GTH; the even subtests read GTL. Receiver data are returned to the Module Control Card on ADRV0. Since all subtests verify the driver can be three-stated, all results are expected to be 0.

Test 3411 runs 10 types of subtests, affecting eight channels. Each subtest type repeats every 10 subtests. Given the following table and the description of the first 10 subtests, you can determine the function and channel for any subtest.

For example, Table 5-40 shows that subtest 67 affects driver channel G. You can figure subtest 67's function by dividing the subtest number by 10 (recall each subtest type repeats every 10 subtests); the remainder of the division is the subtest type:

67/10 = 6, remainder = 7

Subtest 67, like subtest 7, selects FF2 for three-stating and checks the receiver GTH line.

Table 5-40 T3411 subtest driver channels

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a-9a	10a-19a	20a-29a	30a-39a	40a-49a	50a-59a	60a-69a	70a-79a
Page B							
0b-9b	10b-19b	20b-29b	30b-39b	40b-49b	50b-59b	60b-69b	70b-79b

Table 5-41

Subtest	Function
0	Select ADRV0 for three-stating and check receiver GTL: Channel <c>
1	Select ADRV0 for three-stating and check receiver GTH: Channel <c>
2	Select ADRV1 for three-stating and check receiver GTL: Channel <c>
3	Select ADRV1 for three-stating and check receiver GTH: Channel <c>
4	Select FF1 for three-stating and check receiver GTL: Channel <c>
5	Select FF1 for three-stating and check receiver GTH: Channel <c>
6	Select FF2 for three-stating and check receiver GTL: Channel <c>
7	Select FF2 for three-stating and check receiver GTH: Channel <c>
8	Select Module Control Card MTSP and check receiver GTL: Channel <c>
9	Select Module Control Card MTSP and check receiver GTH: Channel <c>

Test 3412

Verify Receiver Data from ARCV

This test verifies receiver response. The drive data are set by ADRV0 and ADRV1. Receiver data are returned to the Module Control Card via ARCV0 and ARCV1.

Subtests 0 through 63 divide into eight groups (eight channels) of eight subtests. The first pair of subtests uses ADRV0 to produce a 1 for the driver data and ARCV0 to return the response. The second pair uses ADRV0 to produce a driver 0 and returns the response on ARCV0. The third and fourth pairs use ADRV1 instead of ADRV0 for driver data and ARCV1 instead of ARCV0 for the receiver return path. Half of the subtests check GTH; the other half check GTL.

Test 3412 runs eight types of subtests, affecting eight channels. Each subtest type repeats every eight subtests. Given the following table and the description of the first eight subtests, you can determine the function and channel for any subtest.

For example, Table 5-42 shows that subtest 37 affects receiver channel E. You can figure subtest 37's function by dividing the subtest number by eight (recall each subtest type repeats every eight subtests); the remainder of the division is the subtest type:

37/8 = 4, remainder = 5

Subtest 37, like subtest 5, sets ADRV0 to 1, checks GTL, and returns the response to the Module Control Card via ARCV1.

Table 5-42 3412 subtest receiver channels

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a-7a	8a-15a	16a-23a	24a-31a	32a-39a	40a-47a	48a-55a	56a-63a
Page B							
0b-7b	8b-15b	16b-23b	24b-31b	32b-39b	40b-47b	48b-55b	56b-63b

Table 5-43

Subtest	Function
0	Set ADRV0 to 1, check GTH, and send response via ARCV0: Channel <c>
1	Set ADRV0 to 1, check GTL, and send response via ARCV0: Channel <c>
2	Set ADRV0 to 0, check GTH, and send response via ARCV0: Channel <c>
3	Set ADRV0 to 0, check GTL, and send response via ARCV0: Channel <c>
4	Set ADRV0 to 1, check GTH, and send response via ARCV1: Channel <c>
5	Set ADRV0 to 1, check GTL, and send response via ARCV1: Channel <c>
6	Set ADRV0 to 0, check GTH, and send response via ARCV1: Channel <c>
7	Set ADRV0 to 0, check GTL, and send response via ARCV1: Channel <c>

Test 3413

Verify GTH and GTL from ARCV

This test checks the GTH and GTL signals from ARCV by using various receiver levels.

The 192 subtests are organized in eight groups (eight channels). The 24 subtests for each channel are divided into two groups of 12. One group uses ADRV0 to drive data and ARCV0 to return the GTH and GTL data; the other group uses ADRV1 and ARCV1.

Six subtests are run with low receiver levels; the other six are run with high receiver levels. Of each group of six, two subtests have the driver force a true low. The next two drive to a level (an invalid mid-level) between the receiver high and low. The final two subtests drive a valid high. Even subtests measure GTH; odd subtests measure GTL.

Test 3413 runs 12 types of subtests, affecting eight channels. Given the following table and the description of the first 12 subtests, you can determine the function and channel for any subtest.

For example, Table 5-44 shows that subtest 67 measures the receiver level of channel C using ARCV1. You can figure subtest 67's function by dividing the subtest number by 12 (recall each subtest type repeats every 12 subtests); the remainder of the division is the subtest type:

67/12= 5, remainder = 7

Subtest 67, like subtest 7, sets ADRV1 to 1, sets RHI to +2.0 volts and RLO to 0.0 volts, and checks GTL via ARVC1.

Table 5-44 T3413 subtest receiver channels

	Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A								
ARCV0	0a-11a	24a-35a	48a-59a	72a-83a	96a-107a	120a-131a	144a-155a	168a-179a
ARCV1	12a-23a	36a-47a	60a-71a	84a-95a	108a-119a	132a-143a	156a-167a	180a-191a
Page B								
ARCV0	0b-11b	24b-35b	48b-59b	72b-83b	96b-107b	120b-131b	144b-155b	168b-179b
ARCV1	12b-23b	36b-47b	60b-71b	84b-95b	108b-119b	132b-143b	156b-167b	180b-191b

Table 5-45

Subtest	Function
0	Set ADRV to 1, set receiver level to RHI = 0 V and RLO = -2 V, and check GTH via ARCV: Channel <c>
1	Set ADRV to 1, set receiver level to RHI = 0 V and RLO = -2 V, and check GTL via ARCV: Channel <c>
2	Set ADRV to 0, set receiver level to RHI = 0 V and RLO = -2 V, and check GTH via ARCV: Channel <c>
3	Set ADRV to 0, set receiver level to RHI = 0 V and RLO = -2 V, and check GTL via ARCV: Channel <c>
4	Set ADRV to 1, set receiver level to RHI = 0 V and RLO = -2 V, and check GTH via ARCV: Channel <c>
5	Set ADRV to 1, set receiver level to RHI = 0 V and RLO = -2 V, and check GTL via ARCV: Channel <c>
6	Set ADRV to 1, set receiver level to RHI = 2 V and RLO = 0 V, and check GTH via ARCV: Channel <c>
7	Set ADRV to 1, set receiver level to RHI = 2 V and RLO = 0 V, and check GTL via ARCV: Channel <c>
8	Set ADRV to 0, set receiver level to RHI = 2 V and RLO = 0 V, and check GTH via ARCV: Channel <c>
9	Set ADRV to 0, set receiver level to RHI = 2 V and RLO = 0 V, and check GTL via ARCV: Channel <c>
10	Set ADRV to 1, set receiver level to RHI = 2 V and RLO = 0 V, and check GTH via ARCV: Channel <c>
11	Set ADRV to 1, set receiver level to RHI = 2 V and RLO = 0 V, and check GTL via ARCV: Channel <c>

Test 3414

Verify Driver / Receiver Data

This test checks the functioning of the drivers and receivers by running three sequencer programs that use the driver and receiver states 1, 0, K (keep), T (toggle), X (receiver don't care), Z (driver three-state), enable/disable, and NOP. After each program is run, test 3414 checks the sequencer status and the P/F log contents.

Table 5-46

Subtest	Function
Page A	
0a	Check sequencer status with enable pull-down
1a-8a	Check fail log data with enable pull-down: Channel A through H
9a	Check sequencer status with enable pull-up
10a-17a	Check fail log data with enable pull-up: Channel A through H
18a	Check sequencer status with NOP
19a-2a6	Check fail log data with NOP: Channel A through H
Page B	
0b	Check sequencer status with enable pull-down
1b-8b	Check fail log data with enable pull-down: Channel A through H
9b	Check sequencer status with enable pull-up
10b-17b	Check fail log data with enable pull-up: Channel A through H
18b	Check sequencer status with NOP
19b-2b6	Check fail log data with NOP: Channel A through H

Test 3415

Verify Driver Duty Cycle

This test checks the duty cycle (symmetry) of each channel's driver waveform. The TIC (time interval counter) measures vector pair timing, and then test 3415 calculates the duty cycle for each channel.

Table 5-47

Subtest	Function	Measurement Path Relays
Page A		
0a	Calculate duty cycle: Channel A	K1604, K1605, K1614, KDA, KGLA, KDCL
1a	Calculate duty cycle: Channel B	K1604, K1605, K1614, KDB, KGLB, KDCL
2a	Calculate duty cycle: Channel C	K1604, K1605, K1614, KDC, KGLC, KDCL
3a	Calculate duty cycle: Channel D	K1604, K1605, K1614, KDD, KGLD, KDCL
4a	Calculate duty cycle: Channel E	K1604, K1605, K1614, KDE, KGLE, KDCL
5a	Calculate duty cycle: Channel F	K1604, K1605, K1614, KDF, KGLF, KDCL
6a	Calculate duty cycle: Channel G	K1604, K1605, K1614, KDG, KGLG, KDCL
7a	Calculate duty cycle: Channel H	K1604, K1605, K1614, KDH, KGLH, KDCL
Page B		
0b	Calculate duty cycle: Channel A	K1604, K1605, K1614, KDA, KGLA, KDCL
1b	Calculate duty cycle: Channel B	K1604, K1605, K1614, KDB, KGLB, KDCL
2b	Calculate duty cycle: Channel C	K1604, K1605, K1614, KDC, KGLC, KDCL
3b	Calculate duty cycle: Channel D	K1604, K1605, K1614, KDD, KGLD, KDCL
4b	Calculate duty cycle: Channel E	K1604, K1605, K1614, KDE, KGLE, KDCL
5b	Calculate duty cycle: Channel F	K1604, K1605, K1614, KDF, KGLF, KDCL
6b	Calculate duty cycle: Channel G	K1604, K1605, K1614, KDG, KGLG, KDCL
7b	Calculate duty cycle: Channel H	K1604, K1605, K1614, KDH, KGLH, KDCL

Test 3416

State Capture Enable Test – Receiver Response

This test verifies the operation of the format chip's hold register and SC (State Capture) pointer.

Table 5-48

Subtest	Function
Page A	
0a-3a	Read Hold register
4a-7a	Read SC RAM pointer
8a-11a	Read Hold register
12a-15a	Read SC RAM pointer
16a-48a	Read SC RAM for channel 0
49a-80a	Read SC RAM for channel 1
81a-112a	Read SC RAM for channel 2
113a-144a	Read SC RAM for channel 3
145a-176a	Read SC RAM for channel 4
177a-208a	Read SC RAM for channel 5
209a-240a	Read SC RAM for channel 6
241a-256a	Read SC RAM for channel 7
Page B	
0b-3b	Read Hold register
4b-7b	Read SC RAM pointer
8b-11b	Read Hold register
12b-15b	Read SC RAM pointer
16b-48b	Read SC RAM for channel 0
49b-80b	Read SC RAM for channel 1
81b-112b	Read SC RAM for channel 2
113b-144b	Read SC RAM for channel 3
145b-176b	Read SC RAM for channel 4
177b-208b	Read SC RAM for channel 5

Table 5-48

Subtest	Function
209b-240b	Read SC RAM for channel 6
241b-256b	Read SC RAM for channel 7

Test 3417

Verify Sequencer Halt on Failure

This test verifies that data stored in the Pass/Fail log on each format chip can be used to halt the sequencer. The sequencer is set to halt on a failure (the same as test 3414), but this test produces failures in one channel at a time using eight different sequencer programs. As each channel produces a failure, test 3417 checks the status of the sequencer to verify that it halted on a failure.

Table 5-49

Subtest	Function
Page A	
0a–7a	Check status of sequencer
Page B	
0b–7b	Check status of sequencer

Test 3419

Verify ARCV Signals

This test verifies the format chip's ARCV signals. Test 3419 runs sequencer programs that set a driver level and select various signals; the Module Control Card then reads the ARCV lines.

Table 5-50

Subtest	Function
Page A	
0a	Set driver level to 1, select RRESP, and check ARCV0
1a	Set driver level to 1, select RRESP, and check ARCV1
2a	Set driver level to 0, select RRESP, and check ARCV0
3a	Set driver level to 0, select RRESP, and check ARCV1
4a	Set driver level to 1, select ER, and check ARCV0
5a	Set driver level to 1, select ER, and check ARCV1
6a	Set driver level to 0, select ER, and check ARCV0
7a	Set driver level to 0, select ER, and check ARCV1
8a	Set driver level to 1, select WERR, and check ARCV0
9a	Set driver level to 1, select WERR, and check ARCV1
10a	Set driver level to 0, select WERR, and check ARCV0
11a	Set driver level to 0, select WERR, and check ARCV1
12a	Set mid driver level, select WERR, and check ARCV0
13a	Set mid driver level, select WERR, and check ARCV1
14a	Set driver level to 1, select REN, and check ARCV0
15a	Set driver level to 1, select REN, and check ARCV1
16a	Disable receiver, select REN, and check ARCV0
17a	Disable receiver, select REN, and check ARCV1
Page B	
0b	Set driver level to 1, select RRESP, and check ARCV0
1b	Set driver level to 1, select RRESP, and check ARCV1
2b	Set driver level to 0, select RRESP, and check ARCV0
3b	Set driver level to 0, select RRESP, and check ARCV1
4b	Set driver level to 1, select ER, and check ARCV0

Table 5-50

Subtest	Function
5b	Set driver level to 1, select ER, and check ARCV1
6b	Set driver level to 0, select ER, and check ARCV0
7b	Set driver level to 0, select ER, and check ARCV1
8b	Set driver level to 1, select WERR, and check ARCV0
9b	Set driver level to 1, select WERR, and check ARCV1
10b	Set driver level to 0, select WERR, and check ARCV0
11b	Set driver level to 0, select WERR, and check ARCV1
12b	Set mid driver level, select WERR, and check ARCV0
13b	Set mid driver level, select WERR, and check ARCV1
14b	Set driver level to 1, select REN, and check ARCV0
15b	Set driver level to 1, select REN, and check ARCV1
16b	Disable receiver, select REN, and check ARCV0
17b	Disable receiver, select REN, and check ARCV1

Test 3420

Verify Driver Tap Delay Accuracy

This test verifies the format chips' driver delay lines.

Test 3420 sets the TCLK to 625.0 kHz and routes it to TIC channel B to be used as a reference. The drivers are connected to the Module Control Card's TIC channel A. Test 3420 measures the delay for each driver channel, tap delay, and format chip delay line.

The 128 subtests divide into eight groups (eight channels) of 16 subtests. Of the 16 subtests for each channel, the first eight measure delays on delay line A; the other eight check delay line B. Subtests within each group of eight subtests correspond to different delay times.

Test 3420 runs 16 types of subtests, affecting eight channels. Each subtest type repeats every 16 subtests. Given the following table and the description of the first 16 subtests, you can determine the function and channel for any subtest.

For example, Table 5-51 shows that subtest 67 affects driver channel E. You can figure subtest 67's function by dividing the subtest number by 16 (recall each subtest type repeats every 16 subtests); the remainder of the division is the subtest type:
67/16 = 4, remainder = 3

Subtest 67, like subtest 3, calculates the driver tap delay on delay line A using delay 3.

Table 5-51 T3420 subtest driver channels

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a-15a	16a-31a	32a-47a	48a-63a	64a-79a	80a-95a	96a-111a	112a-127a
Page B							
0b-15b	16b-31b	32b-47b	48b-63b	64b-79b	80b-95b	96b-111b	112b-127b

Table 5-52

Subtest	Function
0	Calculate driver tap delay using line A and delay 0: Channel <c>
1	Calculate driver tap delay using line A and delay 1: Channel <c>
2	Calculate driver tap delay using line A and delay 2: Channel <c>
3	Calculate driver tap delay using line A and delay 3: Channel <c>
4	Calculate driver tap delay using line A and delay 4: Channel <c>
5	Calculate driver tap delay using line A and delay 5: Channel <c>
6	Calculate driver tap delay using line A and delay 6: Channel <c>
7	Calculate driver tap delay using line A and delay 7: Channel <c>
8	Calculate driver tap delay using line B and delay 0: Channel <c>
9	Calculate driver tap delay using line B and delay 1: Channel <c>
10	Calculate driver tap delay using line B and delay 2: Channel <c>
11	Calculate driver tap delay using line B and delay 3: Channel <c>
12	Calculate driver tap delay using line B and delay 4: Channel <c>
13	Calculate driver tap delay using line B and delay 5: Channel <c>
14	Calculate driver tap delay using line B and delay 6: Channel <c>
15	Calculate driver tap delay using line B and delay 7: Channel <c>

Test 3421

Verify Receiver Tap Delay Accuracy

This test verifies the format chip's receiver delay lines.

Test 3421 sets the TCLK to 625.0 kHz and routes it to TIC channel B to be used as a reference. The receivers are connected to the Module Control Card's TIC channel A. Test 3421 measures the delay for each receiver channel, tap delay, and format chip delay line.

The 128 subtests divide into 16 groups of eight subtests. Each group of eight subtests corresponds to eight different delay times. The first 64 subtests check delay line A (using ARCV0); the remaining subtests check delay line B (using ARCV1).

Test 3421 runs eight types of subtests, affecting eight channels. Each subtest type repeats every eight subtests. Given the following table and the description of the first eight subtests, you can determine the function and channel for any subtest.

For example, Table 5-53 shows that subtest 67 affects driver channel A. You can figure subtest 67's function by dividing the subtest number by eight (recall each subtest type repeats every eight subtests); the remainder of the division is the subtest type:

67/8= 8, remainder = 3

Since 67 is greater than 64, subtest 67 tests delay line B. Subtest 67, like subtest 3, calculates the receiver tap delay on delay line B using delay 3.

Table 5-53 T3421 subtest receiver channels

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a-7a 64a-71a	8a-15a 72a-79a	16a-23a 80a-87a	24a-31a 88a-95a	32a-39a 96a-103a	40a-47a 104a-111a	48a-55a 112a-119a	56a-63a 120a-127a
Page B							
0b-7b 64b-71b	8b-15b 72b-79b	16b-23b 80b-87b	24b-31b 88b-95b	32b-39b 96b-103b	40b-47b 104b-111b	48b-55b 112b-119b	56b-63b 120b-127b

Table 5-54

Subtest	Function
0	Calculate receiver delay using line A (B) and delay 0: Channel <c>
1	Calculate receiver delay using line A (B) and delay 1: Channel <c>
2	Calculate receiver delay using line A (B) and delay 2: Channel <c>
3	Calculate receiver delay using line A (B) and delay 3: Channel <c>
4	Calculate receiver delay using line A (B) and delay 4: Channel <c>
5	Calculate receiver delay using line A (B) and delay 5: Channel <c>
6	Calculate receiver delay using line A (B) and delay 6: Channel <c>
7	Calculate receiver delay using line A (B) and delay 7: Channel <c>

Test 3422

Verify Three-State of ARCV Signal

This test verifies the format chip's ability to three-state its ARCV0 and ARCV1 lines. The sequencer program enables each format chip to drive its ARCV lines and disable the other format chips' ARCV outputs. The disabled format chips are set to the opposite data state of the active chip.

Subtests 0 through 31 are divided into two groups of 16. The first group tests ARCV0; the second tests ARCV1. The groups of 16 divide into four sets of four subtests. The first four sets groups correspond to every other receiver channel (channels A, C, E, and G). The second four sets corresponds to channels B, D, F, and H. The four subtests for each of the eight sets select GTH or GTL and drive either a 0 or a 1.

Test 3422 runs four types of subtests, affecting eight channels. Given the subtest number, the following table, and the description of the first four subtests, you can determine the function and channel for any subtest.

For example, Table 5-55 shows that subtest 27 affects receiver channel F. Since 27 is between 16 and 31, subtest 27 checks ARCV1. You can figure subtest 27's function by dividing the subtest number by four (recall each subtest type repeats every four subtests); the remainder of the division is the subtest type:

27/4= 6, remainder = 3

Subtest 27, like subtest 3, selects GTL, drives a 0, and checks the ARCV1 line.

Table 5-55 T3422 subtest receiver channel

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a-3a	16a-19a	4a-7a	20a-23a	8a-11a	24a-27a	12a-15a	28a-31a
Page B							
0b-3b	16b-19b	4b-7b	20b-23b	8b-11b	24b-27b	12b-15b	28b-31b

Table 5-56

Subtest	Function
0	Select GTH, drive 1, and check ARCV: Channel <c>
1	Select GTL, drive 1, and check ARCV: Channel <c>
2	Select GTH, drive 0, and check ARCV: Channel <c>
3	Select GTL, drive 0, and check ARCV: Channel <c>

Test 3423

Verify State Capture Data

This test verifies the format chip's state capture data. Test 3423 connects all the drivers to their receivers and then runs a sequencer program.

Subtests 0 through 7 read the hold registers and state capture RAM. Subtests 8 through 15 perform the same function as subtests 0 through 7 but check the hold registers and state capture RAM after the sequencer run. The first eight subtests for test 3423 are shown below.

Table 5-57

Subtest	Function
0	Check hold register: Channels A and B
1	Check hold register: Channels C and D
2	Check hold register: Channels E and F
3	Check hold register: Channels G and H
4	Check SC RAM pointer: Channels A and B
5	Check SC RAM pointer: Channels C and D
6	Check SC RAM pointer: Channels E and F
7	Check SC RAM pointer: Channels G and H

Subtests 16 through 527 check the state capture RAM contents for each address. The four functions of subtests 16 through 19 repeat every four subtests. The functions for subtests 16 through 19 are shown below.

Table 5-58

Subtest	Function
16	Check SC RAM: Channels A and B
17	Check SC RAM: Channels C and D
18	Check SC RAM: Channels E and F
19	Check SC RAM: Channels G and H

Test 3424

Verify Driver at 20 MHz

This test measures the output frequency of each driver at 20 MHz. The drivers are run via the ADRV lines and are measured with the TIC on Module Control Card. Driver data are multiplexed from the Module Control Card DUTCLK generator on ADRV0 (channels A through D) and ADRV1 (channels E through H). Subtests 0 through 7 measure the driver frequency for each channel.

Table 5-59

Subtest	Function
Page A	
0a-3a	Measure driver frequency using ADRV0: Channel A through D
4a-7a	Measure driver frequency using ADRV1: Channel E through H
Page B	
0b-3b	Measure driver frequency using ADRV0: Channel A through D
4b-7b	Measure driver frequency using ADRV1: Channel E through H

Test 3434

Verify Driver and Receiver Data

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test is a fast-mode[1] version of test 3414. The following functions are verified for the driver and receiver data in fast-mode: 1, 0, keep, toggle, enable/disable, and NOP (no operation).

1. When the pattern rate of the system is greater than 12 MP/s, piping circuitry is activated which puts the system in what is called fast-mode. All systems which operating at 20 MP/s run in fast-mode.

Test 3435

Verify FAIL Pipe Enable/Disable[1]

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test verifies that the FAIL pipe enable/disable bit from the I/O chip is functional.

1. The pipe is a sequence of registers in control signal paths between cards. These registers regulate the flow of data passed between cards in systems running faster than 12 MP/s. The enable/disable lines select either a piped or non-piped output of their respective data lines to the Mother Card.

Test 3436

Verify ARCV0 Pipe Enable/Disable

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test verifies that the ARCV0 pipe enable/disable bit from the I/O chip is functional.

Test 3437

Verify ARCV1 Pipe Enable/Disable

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test verifies that the ARCV1 pipe enable/disable bit from the I/O chip is functional.

Test 3438

Check FAIL, ARCV0, and ARCV1 Pipe Enable / Disable Interaction

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test verifies that the FAIL, ARCV0, and ARCV1 pipe enable/disable bits are independent (not shorted together) and functional.

Driver

Test 3439

Verify Driver Level

This test checks the driver high (DHI) and driver low (DLO) voltage levels on all drivers. The output of the drivers is measured on the ASRU DC detector.

Subtests 0 through 143 are divided into eight groups (for eight channels) of 18 subtests per group. Within each group of 18 subtests, the first nine subtests measure driver high levels, and the second nine subtests measure driver low levels.

Given the following table and the description of the first 18 subtests, you can determine the function and channel for any subtest.

To find the test type for any failed subtest, do this simple calculation: for example, if subtest 67 fails, divide 67 by 18 (the number of subtests). That yields 3 with a remainder of 13. So subtest 67 is Channel D (67 is in the group 54–71), and subtest 13 is DLO = 0.5 volts.

Table 5-60 T3439 subtest driver channels

Channel A	Channel B	Channel C	Channel D	Channel E	Channel F	Channel G	Channel H
Page A							
0a–17a	18a–35a	36a–53a	54a–71a	72a–89a	90a–107a	108a–125a	126a–143a
Page B							
0b–17b	18b–35b	36b–53b	54b–71b	72b–89b	90b–107b	108b–125b	126b–143bf

Table 5-61

Subtest	Function	
0	Measure driver high level with DHI = -2.5 V:	Channel <c>
1	Measure driver high level with DHI = -1.5 V:	Channel <c>
2	Measure driver high level with DHI = -0.5 V:	Channel <c>
3	Measure driver high level with DHI = 0.5 V:	Channel <c>
4	Measure driver high level with DHI = 1.5 V:	Channel <c>
5	Measure driver high level with DHI = 2.5 V:	Channel <c>
6	Measure driver high level with DHI = 3.5 V:	Channel <c>
7	Measure driver high level with DHI = 0 V:	Channel <c>
8	Measure driver high level with DHI = 5.0 V:	Channel <c>
9	Measure driver low level with DLO = -3.5 V:	Channel <c>
10	Measure driver low level with DLO = -2.5 V:	Channel <c>
11	Measure driver low level with DLO = -1.5 V:	Channel <c>
12	Measure driver low level with DLO = -0.5 V:	Channel <c>
13	Measure driver low level with DLO = 0.5 V:	Channel <c>
14	Measure driver low level with DLO = 1.5 V:	Channel <c>
15	Measure driver low level with DLO = 2.5 V:	Channel <c>
16	Measure driver low level with DLO = 3.5 V:	Channel <c>
17	Measure driver low level with DLO = 0 V:	Channel <c>

Test 3440

Check Ground-Bounce Control

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test verifies that the ground bounce control can be enabled and disabled by reading the I/O register following enable and disable commands only on the single-density HybridPlus-20 Pin Card. It also verifies that the ground bounce test relay (KGB14) is functional by reading the I/O register after closing the relay and then reading the register again after opening the relay.

Test 3441

AC Ground Relay Test

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test verifies that relays KGB1 through KGB14, which make the connection between digital ground and SW_GND, are functionalonly only on the single-density HybridPlus-20 Pin Card.

This test does not isolate the failing relay, and will not fail when a single relay is stuck open. This is because all of these relays are in parallel.

Failure only occurs if one or more relays are stuck closed or if all fourteen relays are stuck open. If a relay is stuck closed, problems with analog measurements may arise. If they are all stuck open, there may be problems with high-frequency digital testing.

Table 5-62

Subtest	Function
0	Relay stuck closed test
1	All relays stuck open test
2	Ground bounce disable

NOTE **Failure of KGB14 will make KGB1 through KGB13 appear to fail, since it is in the test path. If failure of the entire relay set occurs, try replacing KGB14 first. Also, failure of test 3440 will cause misleading results in this test.**

Test 3450

Check Receiver Ringing Clamp Enable and Disable

Requires: Either HybridPlus-6 Pin Card, HybridPlus-12 Pin Card, or HybridPlus-20

This test checks bits on the I/O chip that enable the receiver ringing clamps for channels A through H.

Table 5-63

Subtest	Function
Page A	
0a-7a	Check clamp enable for channels A through H
8a-15a	Check clamp disable for channels A through H
16a	Check simultaneous enable of channels A through H
17a	Check simultaneous disable of channels A through H
Page B	
0b-7b	Check clamp enable for channels A through H
8b-15b	Check clamp disable for channels A through H
16b	Check simultaneous enable of channels A through H
17b	Check simultaneous disable of channels A through H

Test 3451

Check Receiver Ringing Clamps

Requires: Either HybridPlus-6 Pin Card, HybridPlus-12 Pin Card, or HybridPlus-20

This test verifies that the receiver ringing clamps are operating properly. The amount of current that the clamps push or pull at different voltages is measured. All measurements are made with the clamps set at standard TTL levels.

Table 5-64

Subtest	Function
Page A	
0a-5a	Check channel A
6a-11a	Check channel B
12a-17a	Check channel C
18a-23a	Check channel D
24a-29a	Check channel E
30a-35a	Check channel F
36a-41a	Check channel G
42a-47a	Check channel H
Page B	
0b-5b	Check channel A
6b-11b	Check channel B
12b-17b	Check channel C
18b-23b	Check channel D
24b-29b	Check channel E
30b-35b	Check channel F
36b-41b	Check channel G
42b-47b	Check channel H

Test 3519

Verify Driver Timing Accuracy

This test checks driver timing accuracy by using two delay lines and eight delay times: -30, -10, 0, 10, 30, 50, 70, and 100 nanoseconds.

Table 5-65

Subtest	Function
Page A	
0a-15a	Measure driver delay using delay lines A and B: Channel A
16a-31a	Measure driver delay using delay lines A and B: Channel B
32a-4a7	Measure driver delay using delay lines A and B: Channel C
48a-63a	Measure driver delay using delay lines A and B: Channel D
64a-79a	Measure driver delay using delay lines A and B: Channel E
80a-95a	Measure driver delay using delay lines A and B: Channel F
96a-111a	Measure driver delay using delay lines A and B: Channel G
112a-127a	Measure driver delay using delay lines A and B: Channel H
Page B	
0b-15b	Measure driver delay using delay lines A and B: Channel A
16b-31b	Measure driver delay using delay lines A and B: Channel B
32b-4b7	Measure driver delay using delay lines A and B: Channel C
48b-63b	Measure driver delay using delay lines A and B: Channel D
64b-79b	Measure driver delay using delay lines A and B: Channel E
80b-95b	Measure driver delay using delay lines A and B: Channel F
96b-111b	Measure driver delay using delay lines A and B: Channel G
112b-127b	Measure driver delay using delay lines A and B: Channel H

Test 3529

Verify Driver and Receiver at 12 MP/s

This test verifies that the drivers and receivers are working by running three sequencer programs and checking the HybridPlus Pin Card status and fail log flag.

Table 5-66

Subtest	Function
Page A	
0a-1a	Check sequencer and card status, drive 1 and 0 both pass
2a-9a	Check fail log flag, drive 1 and 0 both pass
10a-11a	Check sequencer and card status, drive 1 fail
12a-19a	Check fail log flag, drive 1 fail
20a-21a	Check sequencer and card status, drive 0 fail
22a-29a	Check fail log flag, drive 0 fail
Page B	
0b-1b	Check sequencer and card status, drive 1 and 0 both pass
2b-9b	Check fail log flag, drive 1 and 0 both pass
10b-11b	Check sequencer and card status, drive 1 fail
12b-19b	Check fail log flag, drive 1 fail
20b-21b	Check sequencer and card status, drive 0 fail
22b-29b	Check fail log flag, drive 0 fail

Test 3530

Driver Receiver Working Test for 317X Systems

This is the same test as Test 3529, except the test pattern rate is 6 MP/s.

This test verifies that the drivers and receivers arte working by running three sequencer programs and checking the HybridPlus Pin Card status and fail log flag.

Table 5-67

Subtest	Function
Page A	
0a-1a	Check sequencer and card status, drive 1 and 0 both pass.
2a-9a	Check fail log flag, drive 1 and 0 both pass
10a-11a	Check sequencer and card status, drive 1 fail
12a-19a	Check fail log flag, drive 1 fail
20a-21a	Check sequencer and card status, drive 0 fail
22a-29a	Check fail log flag, drive 0 fail
Page B	
0b-1b	Check sequencer and card status, drive 1 and 0 both pass.
2b-9b	Check fail log flag, drive 1 and 0 both pass
10b-11b	Check sequencer and card status, drive 1 fail
12b-19b	Check fail log flag, drive 1 fail
20b-21b	Check sequencer and card status, drive 0 fail
22b-29b	Check fail log flag, drive 0 fail

Test 3539

Verify Driver and Receiver

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test is a fast-mode version of Test 3529 with the receiver ringing clamp circuit disabled. The subtests are the same as those in test 3529.

Test 3540

Verify Driver and Receiver with Clamp Circuit

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test is a fast-mode version of Test 3529 with the receiver ringing clamp circuit enabled. The subtests are the same as those in test 3529.

Test 3541

Verify Driver and Receiver with Ground Bounce Disable Off

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test is the same as Test 3539 with the ground bounce disable off. The subtests are the same as those in Test 3529.

Test 3559

Verify Driver Frequency at 6.25 MHz

This test uses 16 subtests to verify that the Pin Card drivers operate at 6.25 MHz (6 MP/s). Even subtests check the sequencer status, and odd subtests measure the driver frequency for each channel.

Table 5-68

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Check sequencer status for Channel A through H
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure driver frequency for Channel A through H
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Check sequencer status for Channel A through H
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure driver frequency for Channel A through H

Test 3560

Verify Driver Frequency at 10 MHz

Requires: 20 MP/s system

This test verifies that the drivers for the HybridPlus-20 Pin Card can operate at 10 MHz (20 MP/s).

Table 5-69

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Check sequencer status for Channel A through H
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure driver frequency for Channel A through H
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Check sequencer status for Channel A through H
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure driver frequency for Channel A through H

Test 3589

Verify Driver Current Limit (Source and Sink)

This test verifies the current limit detection and level for each driver channel. Of the 32 subtests, the even subtests check for overcurrent detection, and the odd subtests verify the current at which the limit was detected. Subtests 0 through 15 check all eight drivers sourcing current; subtests 16 through 31 check the drivers sinking current.

Test 3595

Driver Backmatch Resistor Test

This test checks the determine whether the driver backmatch resistor is present and of the correct resistance. The backmatch resistor is used for driver termination during functional tests and driver protection during overdrive tests.

Table 5-70

Subtest	Function
Page A	
0a	Backmatch resistor on channel 0 enabled
1a	Backmatch resistor on channel 0 disabled
2a-3a	Check the Backmatch resistor on channel 1 is enabled/disabled
4a-5a	Check the Backmatch resistor on channel 2 is enabled/disabled
6a-7a	Check the Backmatch resistor on channel 3 is enabled/disabled
8a-9a	Check the Backmatch resistor on channel 4 is enabled/disabled
10a-11a	Check the Backmatch resistor on channel 5 is enabled/disabled
12a-13a	Check the Backmatch resistor on channel 6 is enabled/disabled
14a-15a	Check the Backmatch resistor on channel 7 is enabled/disabled
Page B	
0b	Backmatch resistor on channel 0 enabled
1b	Backmatch resistor on channel 0 disabled
2b-3b	Check the Backmatch resistor on channel 1 is enabled/disabled
4b-5b	Check the Backmatch resistor on channel 2 is enabled/disabled
6b-7b	Check the Backmatch resistor on channel 3 is enabled/disabled
8b-9b	Check the Backmatch resistor on channel 4 is enabled/disabled
10b-11b	Check the Backmatch resistor on channel 5 is enabled/disabled
12b-13b	Check the Backmatch resistor on channel 6 is enabled/disabled
14b-15b	Check the Backmatch resistor on channel 7 is enabled/disabled

Test 3596

Verify Driver Enable and Disable

This test verifies the driver enable and disable functions. The 45 subtests are divided into five groups of nine subtests, each group representing results from a sequencer program. The groups of nine consist of one sequencer status check and fail log flag checks for each driver. Of the five sequencer programs, only the first contains no failures.

Table 5-71

Subtest	Function
Page A	
0a	Check sequencer status after driving a square wave
1a-8a	Check fail log flag after driving a square wave
9a	Check sequencer status after driving high during driver disable and enable pull-down
10a-17a	Check fail log flag after driving high during driver disable and enable pull-down
18a	Check sequencer status after driving low during driver disable and enable pull-up
19a-26a	Check fail log flag after driving low during driver disable and enable pull-up
27a	Check sequencer status after driving Z (driver three-state) with default 1 and enable pull-down
28a-35a	Check fail log flag after driving Z (driver three-state) with default 1 and enable pull-down
36a	Check sequencer status after driving Z (driver three-state) with default 0 and enable pull-up
37a-44a	Check fail log flag after driving Z (driver three-state) with default 0 and enable pull-up
Page B	
0b	Check sequencer status after driving a square wave
1b-8b	Check fail log flag after driving a square wave
9b	Check sequencer status after driving high during driver disable and enable pull-down
10b-17b	Check fail log flag after driving high during driver disable and enable pull-down
18b	Check sequencer status after driving low during driver disable and enable pull-up
19b-26b	Check fail log flag after driving low during driver disable and enable pull-up
27b	Check sequencer status after driving Z (driver three-state) with default 1 and enable pull-down
28b-35b	Check fail log flag after driving Z (driver three-state) with default 1 and enable pull-down

Table 5-71

Subtest	Function
36b	Check sequencer status after driving Z (driver three-state) with default 0 and enable pull-up
37b-44b	Check fail log flag after driving Z (driver three-state) with default 0 and enable pull-up

Test 3597

Verify Driver Overvoltage

This test checks the drivers' ability to respond to overvoltage conditions. The ASRU card applies four voltages to each driver (+5.0 volts, +10.0 volts, -3.5 volts, and -5.0 volts), and then test 3597 checks the Pin Card status for overvoltage detections.

Table 5-72

Subtest	Function
Page A	
0a-7a	Check card status after driving 5.0 volts: Channel A through H
8a-15a	Check card status after driving 10.0 volts: Channel A through H
16a-23a	Check card status after driving -3.5 volts: Channel A through H
24a-31a	Check card status after driving -5.0 volts: Channel A through H
Page B	
0b-7b	Check card status after driving 5.0 volts: Channel A through H
8b-15b	Check card status after driving 10.0 volts: Channel A through H
16b-23b	Check card status after driving -3.5 volts: Channel A through H
24b-31b	Check card status after driving -5.0 volts: Channel A through H

Test 3598

Verify Driver Enable and Disable

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test is a fast-mode version of Test 3596.

Test 3599

Verify Fatal Error Mask

This test uses 48 subtests to checks the card's ability to ignore overpower conditions. These subtests are grouped into three groups of 16.

Subtests 0 through 15 generate overpower and overcurrent on each channel, creating a FATER condition. Subtests 0, 2, 4, 6, 8, 10, 12, and 14 read the overpower and overcurrent register, expecting each channel to report both conditions. Subtests 1, 3, 5, 7, 9, 11, 13, and 15 read the status register to prove a FATER occurred.

Subtests 16 through 31 create and mask overpower on all the channels. No FATER conditions should occur. Subtests 16, 18, 20, 22, 24, 26, 28, and 30 read the overpower and overcurrent register to show that overpower was detected for each channel. Subtest, 19, 21, 23, 25, 27, 29, and 31 read the status register to prove a FATER did not occur.

Subtests 32 through 47 create overpower on all the channels, creating a FATER condition. Subtests 32, 34, 36, 38, 40, 42, 44, and 46 check the overpower and overcurrent register for overpower conditions for each channel. Subtests 33, 35, 37, 39, 41, 43, 45, and 47 read the status register.

Test 3600

Double-Density Card Driver Overvoltage

This test checks the driver's ability to respond to overvoltage conditions. The ASRU card applies four voltages (+5, +10, -3.5 and -8 volts) and checks the double-density pin card status for overvoltage detection.

Table 5-73

Subtest	Function
Page A	
0a-2a	Check status of: pin, Driver module, Cleared Driver module for channel 0 at +5 V
3a-5a	Check status of: pin, Driver module, Cleared Driver module for channel 1 at +5 V
6a-23a	Check status of: pin, Driver module, Cleared Driver module for channels 2-7 at +5 V
24a-47a	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at +10 V
48a-71a	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -3.5 V
72a-95a	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -8 V

Table 5-73

Subtest	Function
Page B	
0b-2b	Check status of: pin, Driver module, Cleared Driver module for channel 0 at +5 V
3b-5b	Check status of: pin, Driver module, Cleared Driver module for channel 1 at +5 V
6b-23b	Check status of: pin, Driver module, Cleared Driver module for channels 2-7 at +5 V
24b-47b	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at +10 V
48b-71b	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -3.5 V
72b-95b	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -8 V

Test 3601

Double-Density Card Driver Overvoltage

This test is the same as Test 3600, but for the Series 3 double-density card.

Receiver

Test 3619

Verify Receiver Timing

This test verifies receiver timing at different delay settings: -10, 10, 30, 70, and 100 nanoseconds. The 96 subtests are grouped in 16 sets of six subtests. These six subtests measure (via the Module Control Card TIC) receiver channel delay at one of six different delay settings. The 16 sets represent delay lines A and B for the eight channels.

Table 5-74

Subtest	Function
Page A	**Page A**
0a-5a	Measure receiver delay using delay line A: Channel A
6a-11a	Measure receiver delay using delay line A: Channel B
12a-17a	Measure receiver delay using delay line A: Channel C
18a-23a	Measure receiver delay using delay line A: Channel D
24a-29a	Measure receiver delay using delay line A: Channel E
30a-35a	Measure receiver delay using delay line A: Channel F
36a-41a	Measure receiver delay using delay line A: Channel G
42a-47a	Measure receiver delay using delay line A: Channel H
48a-53a	Measure receiver delay using delay line B: Channel A
54a-59a	Measure receiver delay using delay line B: Channel B

Table 5-74

Subtest	Function
60a-65a	Measure receiver delay using delay line B: Channel C
66a-71a	Measure receiver delay using delay line B: Channel D
72a-77a	Measure receiver delay using delay line B: Channel E
78a-83a	Measure receiver delay using delay line B: Channel F
84a-89a	Measure receiver delay using delay line B: Channel G
90a-95a	Measure receiver delay using delay line B: Channel H
Page B	**Page B**
0b-5b	Measure receiver delay using delay line A: Channel A
6b-11b	Measure receiver delay using delay line A: Channel B
12b-17b	Measure receiver delay using delay line A: Channel C
18b-23b	Measure receiver delay using delay line A: Channel D
24b-29b	Measure receiver delay using delay line A: Channel E
30b-35b	Measure receiver delay using delay line A: Channel F
36b-41b	Measure receiver delay using delay line A: Channel G
42b-47b	Measure receiver delay using delay line A: Channel H
48b-53b	Measure receiver delay using delay line B: Channel A
54b-59b	Measure receiver delay using delay line B: Channel B
60b-65b	Measure receiver delay using delay line B: Channel C
66b-71b	Measure receiver delay using delay line B: Channel D
72b-77b	Measure receiver delay using delay line B: Channel E
78b-83b	Measure receiver delay using delay line B: Channel F
84b-89b	Measure receiver delay using delay line B: Channel G
90b-95b	Measure receiver delay using delay line B: Channel H

Test 3629

Verify Receiver Sense Range

This test calculates the sense level for each receiver channel by measuring the source voltage (from the ASRU Card) before and after a sequencer run and then checking the Pin Card's state capture RAM for the sense level. Each receiver is tested four ways: at +5.0 volts on the rising edge, at +5.0 volts on the falling edge, at -3.5 volts on the rising edge, and at -3.5 volts on the falling edge.

Table 5-75

Subtest	Function
Page A	
0a-7a	Calculate receiver sense level with rising edge at 5.0 V
8a-15a	Calculate receiver sense level with falling edge at 5.0 V
16a-23a	Calculate receiver sense level with rising edge at -3.5 V
24a-31a	Calculate receiver sense level with falling edge at -3.5 V
Page B	
0b-7b	Calculate receiver sense level with rising edge at 5.0 V
8b-15b	Calculate receiver sense level with falling edge at 5.0 V
16b-23b	Calculate receiver sense level with rising edge at -3.5 V
24b-31b	Calculate receiver sense level with falling edge at -3.5 V

Test 3648

Double-Density Card Receiver Overvoltage

This test verifies the double-density cards overvoltage range: -14.4 volts to 13.8 volts.

Table 5-76

Subtest	Function
Page A	
0a-2a	Check status of: pin, Driver module, Cleared Driver module for channel 0 at +5 V
3a-5a	Check status of: pin, Driver module, Cleared Driver module for channel 1 at +5 V
6a-23a	Check status of: pin, Driver module, Cleared Driver module for channels 2-7 at +5 V
24a-47a	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at +10 V
48a-71a	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -5 V
72a-95a	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -10 V
Page B	
0b-2b	Check status of: pin, Driver module, Cleared Driver module for channel 0 at +5 V
3b-5b	Check status of: pin, Driver module, Cleared Driver module for channel 1 at +5 V
6b-23b	Check status of: pin, Driver module, Cleared Driver module for channels 2-7 at +5 V
24b-47b	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at +10 V
48b-71b	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -5 V
72b-95b	Check status of: pin, Driver module, Cleared Driver module for channels 0-7 at -10 V

Test 3649

Verify Receiver Overvoltage

This test checks each receiver four times, at +5.0 volts, +10.0 volts, -3.5 volts, and -5.0 volts. The ASRU card applies one of the four voltages to each receiver, and then test 3649 checks the Pin Card for an overvoltage condition.

Table 5-77

Subtest	Function
Page A	
0a-7a	Set driver level to 5.0 V and check card status: Channel A through H
8a-15a	Set driver level to 10.0 V and check card status: Channel A through H
16a-23a	Set driver level to -3.5 V and check card status: Channel A through H
24a-31a	Set driver level to -5.0 V and check card status: Channel A through H
Page B	
0b-7b	Set driver level to 5.0 V and check card status: Channel A through H
8b-15b	Set driver level to 10.0 V and check card status: Channel A through H
16b-23b	Set driver level to -3.5 V and check card status: Channel A through H
24b-31b	Set driver level to -5.0 V and check card status: Channel A through H

Test 3650

Verify Receiver Pull-Up and Pull-Down Level

This test verifies the pull-up and pull-down capability of the receivers. Subtests 0 through 7 measure the receiver levels (with the ASRU AC detector) with the pull-up hardware enabled, and subtests 8 through 15 check the receiver levels with the pull-down hardware enabled.

Test 3651

Double-Density Card Receiver Pull Up / Down Test

This test is similar to test 3650, with the addition of closing the 10-kohm resistor from Xg to ground. This is needed for receiver input loading.

Table 5-78

Subtest	Receiver Pull-up	Receiver Pull-down	Channels Tested (in order)
Page A			
0a-7a	Enabled	Disabled	Channels 0-7
8a-15a	Disabled	Enabled	Channels 0-7
Page B			
0b-7b	Enabled	Disabled	Channels 0-7
8b-15b	Disabled	Enabled	Channels 0-7

Test 3659

Verify Receiver Pull-Up and Pull-Down Current

This test verifies the receiver pull-up and pull-down current. Subtests 0 through 15 test the receivers' pull-up hardware sourcing current. Subtests 16 through 31 test the receivers' pull-down hardware sinking current.

Table 5-79

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Calculate pull-up current with bias level = -2.0 V: Channel <c>
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Calculate pull-up current with bias level = -1.0 V: Channel <c>
16a, 18a, 20a, 22a, 24a, 26a, 28a, 30a	Calculate pull-down current with bias level = 3.0 V: Channel <c>
17a, 19a, 21a, 23a, 25a, 27a, 29a, 31a	Calculate pull-down current with bias level = 4.0 V: Channel <c>
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Calculate pull-up current with bias level = -2.0 V: Channel <c>
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Calculate pull-up current with bias level = -1.0 V: Channel <c>
16b, 18b, 20b, 22b, 24b, 26b, 28b, 30b	Calculate pull-down current with bias level = 3.0 V: Channel <c>
17b, 19b, 21b, 23b, 25b, 27b, 29b, 31b	Calculate pull-down current with bias level = 4.0 V: Channel <c>

Test 3668

Verify Receiver Level Accuracy

This test checks receiver level accuracy at +2.0 volts and +0.8 volts.

Subtests 0 through 47 use the rising-edge and falling-edge receiver levels to calculate the receivers' hysteresis. The remaining subtests, 48 through 79, enable the receiver pull-ups and pull-downs and then calculate the rising-edge levels and the falling-edge levels.

Table 5-80

Subtest	Function	Channel
Page A		
0a-7a	Set RHI = 2.0 V and calculate rising-edge receiver level:	Channel A through H
8a, 10a, 12a, 14a, 16a, 18a, 20a, 22a	Set RLO = 2.0 V and calculate falling-edge receiver level:	Channel A through H
9a, 11a, 13a, 15a, 17a, 19a, 21a, 23a	Calculate receiver hysteresis:	Channel A through H
24a-31a	Set RHI = 0.8 V and calculate rising-edge receiver level:	Channel A through H
32a, 34a, 36a, 38a, 40a, 42a, 44a, 46a	Set RLO = 0.8 V and calculate falling-edge receiver level:	Channel A through H
33a, 35a, 37a, 39a, 41a, 43a, 45a, 47a	Calculate receiver hysteresis:	Channel A through H
48a-55a	Set RHI = 2.0 V, enable receiver pull-up, and calculate rising-edge receiver level:	Channel A through H
56a-63a	Set RLO = 2.0 V, enable receiver pull-up, and calculate falling-edge receiver level:	Channel A through H
64a-71a	Set RHI = 0.8 V, enable receiver pull-down, and calculate rising-edge receiver level:	Channel A through H
72a-79a	Set RLO = 0.8 V, enable receiver pull-down, and calculate falling-edge receiver level:	Channel A through H
Page B		
0b-7b	Set RHI = 2.0 V and calculate rising-edge receiver level:	Channel A through H
8b, 10b, 12b, 14b, 16b, 18b, 20b, 22b	Set RLO = 2.0 V and calculate falling-edge receiver level:	Channel A through H
9b, 11b, 13b, 15b, 17b, 19b, 21b, 23b	Calculate receiver hysteresis:	Channel A through H
24b-31b	Set RHI = 0.8 V and calculate rising-edge receiver level:	Channel A through H
32b, 34b, 36b, 38b, 40b, 42b, 44b, 46b	Set RLO = 0.8 V and calculate falling-edge receiver level:	Channel A through H
33b, 35b, 37b, 39b, 41b, 43b, 45b, 47b	Calculate receiver hysteresis:	Channel A through H
48b-55b	Set RHI = 2.0 V, enable receiver pull-up, and calculate rising-edge receiver level:	Channel A through H

Table 5-80

Subtest	Function	Channel
56b-63b	Set RLO = 2.0 V, enable receiver pull-up, and calculate falling-edge receiver level:	Channel A through H
64b-71b	Set RHI = 0.8 V, enable receiver pull-down, and calculate rising-edge receiver level:	Channel A through H
72b-79b	Set RLO = 0.8 V, enable receiver pull-down, and calculate falling-edge receiver level:	Channel A through H

Test 3678

Verify Receiver Frequency

This test checks the receivers at 6.25 MHz. The even subtests read the sequencer status, and the odd subtests measure the frequency for each receiver.

Table 5-81

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Check sequencer status: Channel A through H
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure receiver frequency: Channel A through H
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Check sequencer status: Channel A through H
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure receiver frequency: Channel A through H

Test 3679

Verify Receiver Enable and Disable

This test verifies the ability to enable and disable the receivers. The 27 subtests are grouped in three sets of nine, each set representing results from a sequencer program. The groups of nine consist of one sequencer status check and fail log flag checks for each receiver.

Table 5-82

Subtest	Function
Page A	
0a	Check sequencer status after sending *don't care* data
1a-8a	Check fail log flag after sending *don't care* data
9a	Check sequencer status after driving 1 and receiving 0 or driving 0 and receiving 1
10a-17a	Check fail log flag after driving 1 and receiving 0 or driving 0 and receiving 1
18a	Check sequencer status after disabling receiver line
19a-26a	Check fail log flag after disabling receiver line
Page B	
0b	Check sequencer status after sending *don't care* data
1b-8b	Check fail log flag after sending *don't care* data
9b	Check sequencer status after driving 1 and receiving 0 or driving 0 and receiving 1
10b-17b	Check fail log flag after driving 1 and receiving 0 or driving 0 and receiving 1
18b	Check sequencer status after disabling receiver line
19b-26b	Check fail log flag after disabling receiver line

Test 3680

Receiver Enable / Disable for 317X Systems

This is the same as test 3679, written for 317X systems. The pattern rate is 6.66 MHz.

This test verifies the ability to enable and disable the receivers. The 27 subtests are grouped in three sets of nine, each set representing results from a sequencer program. The group of nine consists of one sequencer status check and fail log flag checks for each receiver.

Table 5-83

Subtest	Function
Page A	
0a	Check sequencer status after sending **don't care** data
1a-8a	Check fail log flag on channels 0-7 after sending **don't care** data
9a	Check sequencer status after driving 1 and receiving 0 or driving 0 and receiving 1
10a-17a	Check fail log flag after driving 1 and receiving 0 or driving 1 and receiving 0
18a	Check sequencer status after disabling receiver line
19a-26a	Check fail log flag on channels 0-7 after disabling receiver line
Page B	
0b	Check sequencer status after sending **don't care** data
1b-8b	Check fail log flag on channels 0-7 after sending **don't care** data
9b	Check sequencer status after driving 1 and receiving 0 or driving 0 and receiving 1
10b-17b	Check fail log flag after driving 1 and receiving 0 or driving 1 and receiving 0
18b	Check sequencer status after disabling receiver line
19b-26b	Check fail log flag on channels 0-7 after disabling receiver line

Test 3689

Verify Receiver Enable and Disable

Requires: ControlPlus or ControlXT Card, ASRU-B or ASRU-C Card, and HybridPlus-20 Pin Card

This test is a fast-mode version of Test 3679.

Timing

Test 3734

Confirm Driver and Receiver at Speed

This confirmation test verifies that the HybridPlus Pin Card drivers and receivers operate at 3.33 MHz for the 3073 system.

Table 5-84

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Check sequencer status
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure driver frequency of DCHA through DCHH
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Check sequencer status
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure driver frequency of DCHA through DCHH

Test 3758

Verify Receiver Frequency

This test checks the receivers at 3.33 MHz. The even subtests read the sequencer status, and the odd subtests measure the frequency for each receiver.

Table 5-85

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Check sequencer status: Channel A through H
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure receiver frequency: Channel A through H
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Check sequencer status: Channel A through H
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure receiver frequency: Channel A through H

Test 3759

Verify Driver Frequency at 3.33 MHz

This test verifies the Pin Card drivers on the 3073 systems operate at 3.33 MHz. Of the 16 subtests, the even subtests check the sequencer status, and odd subtests measure the driver frequency for each channel.

Table 5-86

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Check sequencer status for Channel A through H1, 3, 5, 7, 9, 11, 13, 15
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Measure driver frequency for Channel A through H
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Check sequencer status for Channel A through H1, 3, 5, 7, 9, 11, 13, 15
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Measure driver frequency for Channel A through H

Test 3760

Driver Offset and Slew Rate Test

This test checks the driver offset and slew rate for channels 0-7.

Other Driver

Test 3769

Driver Three-State Leakage Current

This test checks the driver's three-state leakage current. Each driver is tested at two bias voltages: –2.0 volts and +3.0 volts. Test 3769 contains 16 subtests (eight driver channels and two bias voltages). The even subtests calculate the leakage current for a –2.0 volt bias level; the odd subtests use a +3.0 volt bias level.

Table 5-87

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Calculate three-state leakage current with bias level = –2.0 V: Channel A through H
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Calculate three-state leakage current with bias level = 3.0 V: Channel A through H
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Calculate three-state leakage current with bias level = –2.0 V: Channel A through H
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Calculate three-state leakage current with bias level = 3.0 V: Channel A through H

Test 3770

Double-Density Card Driver Three-State Leakage Current

This test is the same as Test 3769.

This test checks the three-state leakage current of channels A through H drivers at both -2 volts and +3 volts.

Table 5-88

Subtest	Function
Page A	
0a, 2a, 4a, 6a, 8a, 10a, 12a, 14a	Calculate three-state leakage current with bias level = -2.0 V for Channel A-H.
1a, 3a, 5a, 7a, 9a, 11a, 13a, 15a	Calculate three-state leakage current with bias level = 3.0 V for channel A-H.
Page B	
0b, 2b, 4b, 6b, 8b, 10b, 12b, 14b	Calculate three-state leakage current with bias level = -2.0 V for Channel A-H.
1b, 3b, 5b, 7b, 9b, 11b, 13b, 15b	Calculate three-state leakage current with bias level = 3.0 V for channel A-H.

Test 3818

Double-Density Card Output Impedance

This test verifies the output impedance of each channel's driver. All the channels will be measured while driving high first, followed by the channels driving low.

Table 5-89

Subtest	Function
Page A	
0a-7a	Checks the source impedance on channels 0-7
8a-15a	Checks the sink impedance on channels 0-7
Page B	
0b-7b	Checks the source impedance on channels 0-7
8b-15b	Checks the sink impedance on channels 0-7

Test 3819

Driver Output Impedance

This test verifies the output impedance of the drivers. By measuring the driver level without and with a 1.5-kohm load, test 3819 calculates each driver's output impedance.

Test 3820

Driver Slew Rate – Rising Edge

This test verifies the drivers by measuring their rising-edge slew rates. The 80 subtests are grouped into eight sets (eight driver channels) of 10 subtests. Test 3820 checks each driver at ten different slew rates. The slew rate ranges from 25 volts/µs to 250 volts/µs.

Test 3822

Double-Density Card Driver Slew Rate – Rising Edge

This test is the same as test 3820 but with different slew rates.

This test checks the double-density card drivers rising edge slew rate. Each channel is checked at eight different slew rates: 300, 400, 500, 600, 700, 800, 900, and 1000 volts/µs.

Test 3829

Driver Slew Rate – Falling Edge

This test verifies the drivers' falling-edge slew rate. The 80 subtests are grouped into eight sets (eight driver channels) of 10 subtests. Test 3829 checks each driver at ten different slew rates. The slew rate ranges from 25 volts/µs to 250 volts/µs.

Test 3831

Double-density Card Driver Slew Rate – Falling Edge

This test is the same as Test 3829 but with different slew rates.

This test checks the double-density card drivers falling edge slew rate. Each channel is checked at eight different slew rates: 300, 400, 500, 600, 700, 800, 900, and 1000 volts/µs.

Test 3839

CRC Data Acquisition

This test verifies the CRC (cyclic redundancy check) circuitry. After reading the CRC register for each channel, test 3839 runs a sequencer program and rechecks the card status, P/F log contents, and the CRC register.

Table 5-90

Subtest	Function
Page A	
0a-7a	Check CRC register: Channel A through H
8a	Check card status
9a-16a	Check fail log flag: Channel A through H
17a-24a	Check CRC register: Channel A through H
Page B	
0b-7b	Check CRC register: Channel A through H
8b	Check card status
9b-16b	Check fail log flag: Channel A through H
17b-24b	Check CRC register: Channel A through H

Test 3840

Receiver Ones Catcher

This test verifies the receiver's ones catcher capability. Each channel's pre-latch status, latch status, and clear status is checked.

Table 5-91

Subtest	Function
Page A	
0a-2a	Checks the pre-latch, latch, and clear condition of channel 0
3a-23a	Checks the pre-latch, latch, and clear condition of channels 1-7
Page B	
0b-2b	Checks the pre-latch, latch, and clear condition of channel 0
3b-23b	Checks the pre-latch, latch, and clear condition of channels 1-7

Test 3842

Pin Driver Module Reset

This test checks the pin driver module reset by evaluating GTH and GTL for each channel before and after the reset command.

Test 3849

Driver Overpower

This test verifies the driver overpower circuitry. The 96 subtests test each driver at four loads:

- DHI = +3.5 volts with a load of 24.5 ohms in parallel with 1.5 kohms,
- DHI = +2.5 volts with a load of 5 ohms in parallel with 1.5 kohms,
- DLO = -2.5 volts with a load of 24.5 ohms in parallel with 1.5 kohms, and
- DLO = -2.0 volts with a load of 5 ohms in parallel with 1.5 kohms.

For each driver and load, test 3849 checks the length of time for an overpower detection to occur, the sequencer status register, and the over power/current register to find which driver caused an overpower condition.

Test 3859

Driver Current Limit Test (Source)

This test verifies driver current limit. Of the 16 subtests, the even subtests read the over current/power register to determine that the tested driver has detected a current limit. The odd subtests display the current that caused the current limit.

Test 3860

Driver Current

This test is the same as test 3859, except for different current levels. It now tests 700 milliamps for 2 milliseconds and 50 milliamps for 100 milliseconds. These values should not trip the over-temperature switch.

Receiver Bias Current

Test 3970

Receiver Input Bias

This test verifies receiver input bias current. Test 3970 calculates the bias current for each receiver by setting the MOA bias level to one of three values and comparing the MOA's voltages when the receiver is disconnected and connected.

The 24 subtests divide into eight groups (eight channels) of three. The first subtest of the group sets the MOA bias level to -1.0 volt. The second subtest sets a +1.0 volt bias level, and the third sets the bias level to +3.0 volts.

Relay with Fixture: Test 3971 - 3976

Test 3971

Test Pairs of Receiver to X-bus Connect and X-Bus Disconnect Relays can be Closed

Requires: Pin Verification Fixture

This test verifies pairs of KDC and KX relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

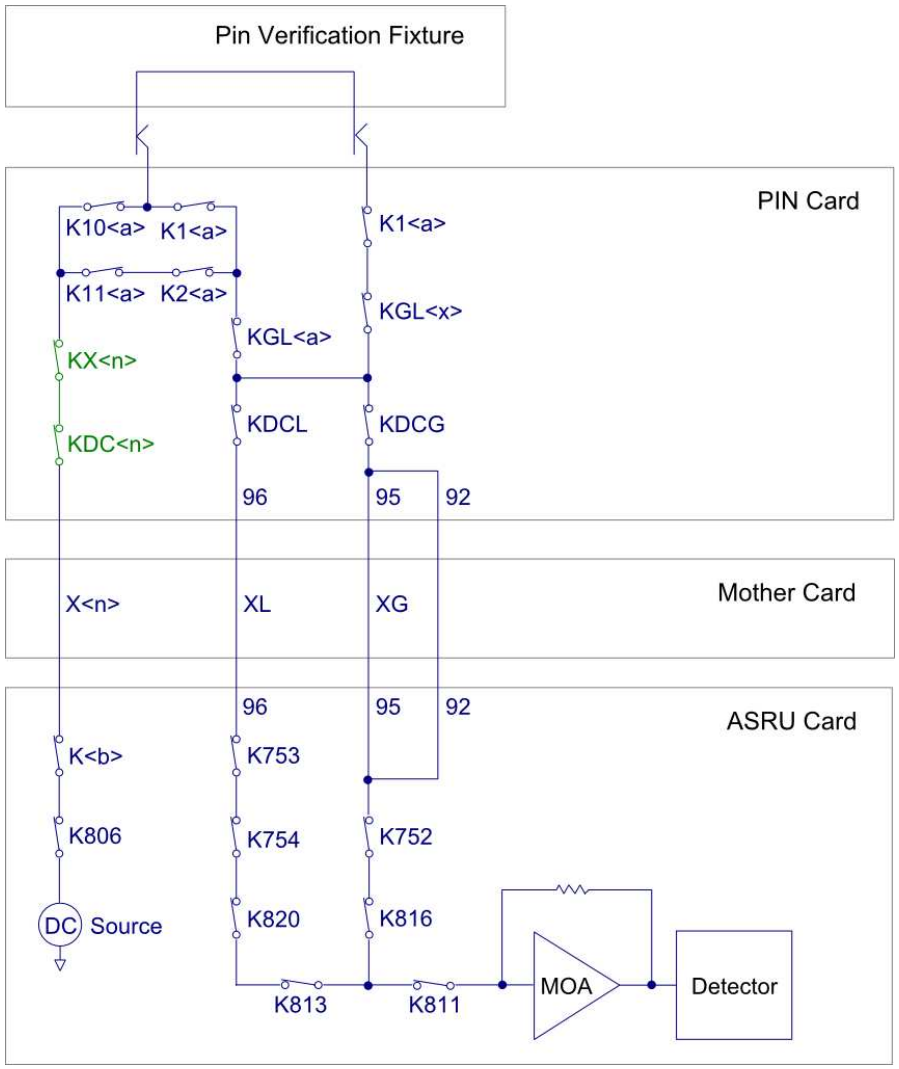
Test 3210 tests the same relays but does not contain the redundant path through the Pin Verification Fixture. With this redundant path, test 3971 can isolate KDC<n> and KX<n> failures from KGL<a> failures. Because the KDC<n> and KX<n> relays are in series, this test cannot isolate an open KDC<n> relay from an open KX<n> relay.

Figure 5-34 shows the measurement path.

Table 5-92

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	K1<x>	KGL<a>	KGL<x>
Page A											
0a	K733	X1	**KDC1**	**KX1**	K1A	K2A	K10A	K11A	K1B	KGLA	KGLB
1a	K734	X2	**KDC2**	**KX2**	K1B	K2B	K10B	K11B	K1C	KGLB	KGLC
2a	K735	X3	**KDC3**	**KX3**	K1C	K2C	K10C	K11C	K1D	KGLC	KGLD
3a	K736	X4	**KDC4**	**KX4**	K1D	K2D	K10D	K11D	K1E	KGLD	KGLE
4a	K737	X5	**KDC5**	**KX5**	K1E	K2E	K10E	K11E	K1F	KGLE	KGLF
5a	K738	X6	**KDC6**	**KX6**	K1F	K2F	K10F	K11F	K1G	KGLF	KGLG
6a	K739	X7	**KDC7**	**KX7**	K1G	K2G	K10G	K11G	K1H	KGLG	KGLH
7a	K740	X8	**KDC8**	**KX8**	K1H	K2H	K10H	K11H	K1A	KGLH	KGLA
Page B											
0b	K733	X1	**KDC1**	**KX1**	K1A	K2A	K10A	K11A	K1B	KGLA	KGLB
1b	K734	X2	**KDC2**	**KX2**	K1B	K2B	K10B	K11B	K1C	KGLB	KGLC
2b	K735	X3	**KDC3**	**KX3**	K1C	K2C	K10C	K11C	K1D	KGLC	KGLD
3b	K736	X4	**KDC4**	**KX4**	K1D	K2D	K10D	K11D	K1E	KGLD	KGLE
4b	K737	X5	**KDC5**	**KX5**	K1E	K2E	K10E	K11E	K1F	KGLE	KGLF
5b	K738	X6	**KDC6**	**KX6**	K1F	K2F	K10F	K11F	K1G	KGLF	KGLG
6b	K739	X7	**KDC7**	**KX7**	K1G	K2G	K10G	K11G	K1H	KGLG	KGLH
7b	K740	X8	**KDC8**	**KX8**	K1H	K2H	K10H	K11H	K1A	KGLH	KGLA

Figure 5-34 T3971



Test 3972

Test Driver to XGL-Bus Connect Relays can be Closed

Requires: Pin Verification Fixture

This test verifies KGLA through KGLH relays can be closed. A test failure is caused when the relay being tested fails to close. The relays being tested are shown in bold, by subtest, in the table below.

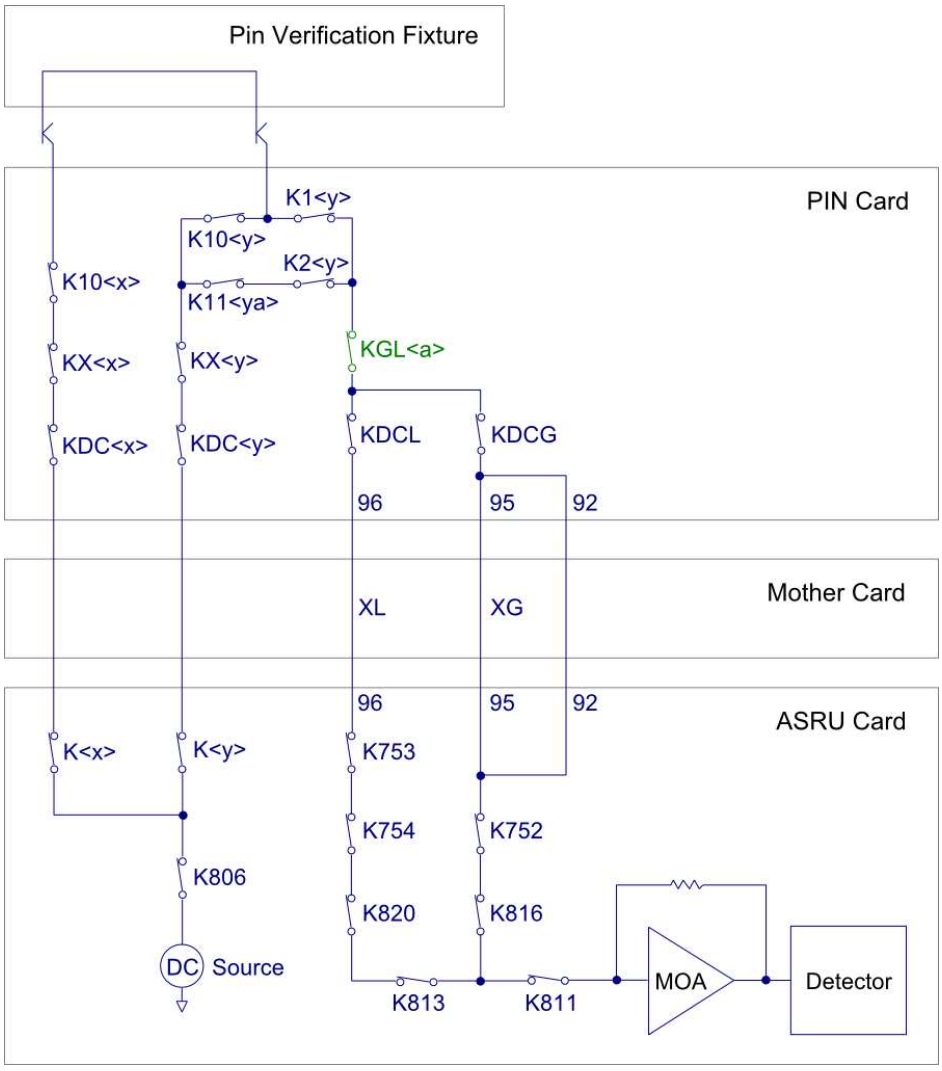
Test 3210 tests the same relays but does not contain the redundant path through the Pin Verification Fixture. With this redundant path, test 3972 can isolate KGL<a> failures from KDC<n> and KX<n> failures.

Figure 5-35 shows the measurement path.

Table 5-93

Subtest	K<x>	K<y>	KDC<x>	KDC<y>	KX<x>	KX<y>	K10<x>	K10<y>	K11<y>	K1<y>	K2<y>	KGL<a>
Page A												
0a	K734	K733	KDC2	KDC1	KX2	KX1	K10B	K10A	K11A	K1A	K2A	**KGLA**
1a	K735	K734	KDC3	KDC2	KX3	KX2	K10C	K10B	K11B	K1B	K2B	**KGLB**
2a	K736	K735	KDC4	KDC3	KX4	KX3	K10D	K10C	K11C	K1C	K2C	**KGLC**
3a	K737	K736	KDC5	KDC4	KX5	KX4	K10E	K10D	K11D	K1D	K2D	**KGLD**
4a	K738	K737	KDC6	KDC5	KX6	KX5	K10F	K10E	K11E	K1E	K2E	**KGLE**
5a	K739	K738	KDC7	KDC6	KX7	KX6	K10G	K10F	K11F	K1F	K2F	**KGLF**
6a	K740	K739	KDC8	KDC7	KX8	KX7	K10H	K10G	K11G	K1G	K2G	**KGLG**
7a	K733	K740	KDC1	KDC8	KX1	KX8	K10A	K10H	K11H	K1H	K2H	**KGLH**
Page B												
0b	K734	K733	KDC2	KDC1	KX2	KX1	K10B	K10A	K11A	K1A	K2A	**KGLA**
1b	K735	K734	KDC3	KDC2	KX3	KX2	K10C	K10B	K11B	K1B	K2B	**KGLB**
2b	K736	K735	KDC4	KDC3	KX4	KX3	K10D	K10C	K11C	K1C	K2C	**KGLC**
3b	K737	K736	KDC5	KDC4	KX5	KX4	K10E	K10D	K11D	K1D	K2D	**KGLD**
4b	K738	K737	KDC6	KDC5	KX6	KX5	K10F	K10E	K11E	K1E	K2E	**KGLE**
5b	K739	K738	KDC7	KDC6	KX7	KX6	K10G	K10F	K11F	K1F	K2F	**KGLF**
6b	K740	K739	KDC8	KDC7	KX8	KX7	K10H	K10G	K11G	K1G	K2G	**KGLG**
7b	K733	K740	KDC1	KDC8	KX1	KX8	K10A	K10H	K11H	K1H	K2H	**KGLH**

Figure 5-35 T3972



Test 3974

Test Receiver to Fixture Interface (MINT) Pin (MUX) Relays can be Closed

Requires: Pin Verification Fixture

This test verifies K10A-H relays can be closed. A test failure is caused when the relay being tested fails to closed. The relays being tested are shown in bold, by subtest, in the table below.

Test 3974 is similar to Test 3240, but it contains a redundant path through the Pin Verification Fixture, allowing it to isolate open driver fixture interface (MINT) pin relays from open receiver to fixture interface (MINT) pin relays. This test can fail due to dirty fixture interface (MINT) pins.

Figure 5-36 shows the measurement path.

Table 5-94

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
Page A								
0a	K733	KDC1	KX1	**K10A**	K1A	K1B	KGLA	KGLB
1a	K733	KDC1	KX1	**K11A**	K2A	K2B	KGLA	KGLB
2a	K733	KDC1	KX1	**K12A**	K3A	K3B	KGLA	KGLB
3a	K733	KDC1	KX1	**K13A**	K4A	K4B	KGLA	KGLB
4a	K733	KDC1	KX1	**K14A**	K5A	K5B	KGLA	KGLB
5a	K733	KDC1	KX1	**K15A**	K6A	K6B	KGLA	KGLB
6a	K733	KDC1	KX1	**K16A**	K7A	K7B	KGLA	KGLB
7a	K733	KDC1	KX1	**K17A**	K8A	K8B	KGLA	KGLB
8a	K733	KDC1	KX1	**K18A**	K9A	K9B	KGLA	KGLB
9a	K734	KDC2	KX2	**K10B**	K1B	K1C	KGLB	KGLC
10a	K734	KDC2	KX2	**K11B**	K2B	K2C	KGLB	KGLC
11a	K734	KDC2	KX2	**K12B**	K3B	K3C	KGLB	KGLC
12a	K734	KDC2	KX2	**K13B**	K4B	K4C	KGLB	KGLC
13a	K734	KDC2	KX2	**K14B**	K5B	K5C	KGLB	KGLC
14a	K734	KDC2	KX2	**K15B**	K6B	K6C	KGLB	KGLC
15a	K734	KDC2	KX2	**K16B**	K7B	K7C	KGLB	KGLC
16a	K734	KDC2	KX2	**K17B**	K8B	K8C	KGLB	KGLC
17a	K734	KDC2	KX2	**K18B**	K9B	K9C	KGLB	KGLC

Table 5-94

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
18a	K735	KDC3	KX3	**K10C**	K1C	K1D	KGLC	KGLD
19a	K735	KDC3	KX3	**K11C**	K2C	K2D	KGLC	KGLD
20a	K735	KDC3	KX3	**K12C**	K3C	K3D	KGLC	KGLD
21a	K735	KDC3	KX3	**K13C**	K4C	K4D	KGLC	KGLD
22a	K735	KDC3	KX3	**K14C**	K5C	K5D	KGLC	KGLD
23a	K735	KDC3	KX3	**K15C**	K6C	K6D	KGLC	KGLD
24a	K735	KDC3	KX3	**K16C**	K7C	K7D	KGLC	KGLD
25a	K735	KDC3	KX3	**K17C**	K8C	K8D	KGLC	KGLD
26a	K735	KDC3	KX3	**K18C**	K9C	K9D	KGLC	KGLD
27a	K736	KDC4	KX4	**K10D**	K1D	K1E	KGLD	KGLE
28a	K736	KDC4	KX4	**K11D**	K2D	K2E	KGLD	KGLE
29a	K736	KDC4	KX4	**K12D**	K3D	K3E	KGLD	KGLE
30a	K736	KDC4	KX4	**K13D**	K4D	K4E	KGLD	KGLE
31a	K736	KDC4	KX4	**K14D**	K5D	K5E	KGLD	KGLE
32a	K736	KDC4	KX4	**K15D**	K6D	K6E	KGLD	KGLE
33a	K736	KDC4	KX4	**K16D**	K7D	K7E	KGLD	KGLE
34a	K736	KDC4	KX4	**K17D**	K8D	K8E	KGLD	KGLE
35a	K736	KDC4	KX4	**K18D**	K9D	K9E	KGLD	KGLE
36a	K737	KDC5	KX5	**K10E**	K1E	K1F	KGLE	KGLF
37a	K737	KDC5	KX5	**K11E**	K2E	K2F	KGLE	KGLF
38a	K737	KDC5	KX5	**K12E**	K3E	K3F	KGLE	KGLF
39a	K737	KDC5	KX5	**K13E**	K4E	K4F	KGLE	KGLF
40a	K737	KDC5	KX5	**K14E**	K5E	K5F	KGLE	KGLF
41a	K737	KDC5	KX5	**K15E**	K6E	K6F	KGLE	KGLF
42a	K737	KDC5	KX5	**K16E**	K7E	K7F	KGLE	KGLF
43a	K737	KDC5	KX5	**K17E**	K8E	K8F	KGLE	KGLF
44a	K737	KDC5	KX5	**K18E**	K9E	K9F	KGLE	KGLF
45a	K738	KDC6	KX6	**K10F**	K1F	K1G	KGLF	KGLG
46a	K738	KDC6	KX6	**K11F**	K2F	K2G	KGLF	KGLG
47a	K738	KDC6	KX6	**K12F**	K3F	K3G	KGLF	KGLG

Table 5-94

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
48a	K738	KDC6	KX6	**K13F**	K4F	K4G	KGLF	KGLG
49a	K738	KDC6	KX6	**K14F**	K5F	K5G	KGLF	KGLG
50a	K738	KDC6	KX6	**K15F**	K6F	K6G	KGLF	KGLG
51a	K738	KDC6	KX6	**K16F**	K7F	K7G	KGLF	KGLG
52a	K738	KDC6	KX6	**K17F**	K8F	K8G	KGLF	KGLG
53a	K738	KDC6	KX6	**K18F**	K9F	K9G	KGLF	KGLG
54a	K739	KDC7	KX7	**K10G**	K1G	K1H	KGLG	KGLH
55a	K739	KDC7	KX7	**K11G**	K2G	K2H	KGLG	KGLH
56a	K739	KDC7	KX7	**K12G**	K3G	K3H	KGLG	KGLH
57a	K739	KDC7	KX7	**K13G**	K4G	K4H	KGLG	KGLH
58a	K739	KDC7	KX7	**K14G**	K5G	K5H	KGLG	KGLH
59a	K739	KDC7	KX7	**K15G**	K6G	K6H	KGLG	KGLH
60a	K739	KDC7	KX7	**K16G**	K7G	K7H	KGLG	KGLH
61a	K739	KDC7	KX7	**K17G**	K8G	K8H	KGLG	KGLH
62a	K739	KDC7	KX7	**K18G**	K9G	K9H	KGLG	KGLH
63a	K740	KDC8	KX8	**K10H**	K1H	K1A	KGLH	KGLA
64a	K740	KDC8	KX8	**K11H**	K2H	K2A	KGLH	KGLA
65a	K740	KDC8	KX8	**K12H**	K3H	K3A	KGLH	KGLA
66a	K740	KDC8	KX8	**K13H**	K4H	K4A	KGLH	KGLA
67a	K740	KDC8	KX8	**K14H**	K5H	K5A	KGLH	KGLA
68a	K740	KDC8	KX8	**K15H**	K6H	K6A	KGLH	KGLA
69a	K740	KDC8	KX8	**K16H**	K7H	K7A	KGLH	KGLA
70a	K740	KDC8	KX8	**K17H**	K8H	K8A	KGLH	KGLA
71a	K740	KDC8	KX8	**K18H**	K9H	K9A	KGLH	KGLA
Page B								
0b	K733	KDC1	KX1	**K10A**	K1A	K1B	KGLA	KGLB
1b	K733	KDC1	KX1	**K11A**	K2A	K2B	KGLA	KGLB
2b	K733	KDC1	KX1	**K12A**	K3A	K3B	KGLA	KGLB
3b	K733	KDC1	KX1	**K13A**	K4A	K4B	KGLA	KGLB
4b	K733	KDC1	KX1	**K14A**	K5A	K5B	KGLA	KGLB

Table 5-94

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
5b	K733	KDC1	KX1	**K15A**	K6A	K6B	KGLA	KGLB
6b	K733	KDC1	KX1	**K16A**	K7A	K7B	KGLA	KGLB
7b	K733	KDC1	KX1	**K17A**	K8A	K8B	KGLA	KGLB
8b	K733	KDC1	KX1	**K18A**	K9A	K9B	KGLA	KGLB
9b	K734	KDC2	KX2	**K10B**	K1B	K1C	KGLB	KGLC
10b	K734	KDC2	KX2	**K11B**	K2B	K2C	KGLB	KGLC
11b	K734	KDC2	KX2	**K12B**	K3B	K3C	KGLB	KGLC
12b	K734	KDC2	KX2	**K13B**	K4B	K4C	KGLB	KGLC
13b	K734	KDC2	KX2	**K14B**	K5B	K5C	KGLB	KGLC
14b	K734	KDC2	KX2	**K15B**	K6B	K6C	KGLB	KGLC
15b	K734	KDC2	KX2	**K16B**	K7B	K7C	KGLB	KGLC
16b	K734	KDC2	KX2	**K17B**	K8B	K8C	KGLB	KGLC
17b	K734	KDC2	KX2	**K18B**	K9B	K9C	KGLB	KGLC
18b	K735	KDC3	KX3	**K10C**	K1C	K1D	KGLC	KGLD
19b	K735	KDC3	KX3	**K11C**	K2C	K2D	KGLC	KGLD
20b	K735	KDC3	KX3	**K12C**	K3C	K3D	KGLC	KGLD
21b	K735	KDC3	KX3	**K13C**	K4C	K4D	KGLC	KGLD
22b	K735	KDC3	KX3	**K14C**	K5C	K5D	KGLC	KGLD
23b	K735	KDC3	KX3	**K15C**	K6C	K6D	KGLC	KGLD
24b	K735	KDC3	KX3	**K16C**	K7C	K7D	KGLC	KGLD
25b	K735	KDC3	KX3	**K17C**	K8C	K8D	KGLC	KGLD
26b	K735	KDC3	KX3	**K18C**	K9C	K9D	KGLC	KGLD
27b	K736	KDC4	KX4	**K10D**	K1D	K1E	KGLD	KGLE
28b	K736	KDC4	KX4	**K11D**	K2D	K2E	KGLD	KGLE
29b	K736	KDC4	KX4	**K12D**	K3D	K3E	KGLD	KGLE
30b	K736	KDC4	KX4	**K13D**	K4D	K4E	KGLD	KGLE
31b	K736	KDC4	KX4	**K14D**	K5D	K5E	KGLD	KGLE
32b	K736	KDC4	KX4	**K15D**	K6D	K6E	KGLD	KGLE
33b	K736	KDC4	KX4	**K16D**	K7D	K7E	KGLD	KGLE
34b	K736	KDC4	KX4	**K17D**	K8D	K8E	KGLD	KGLE

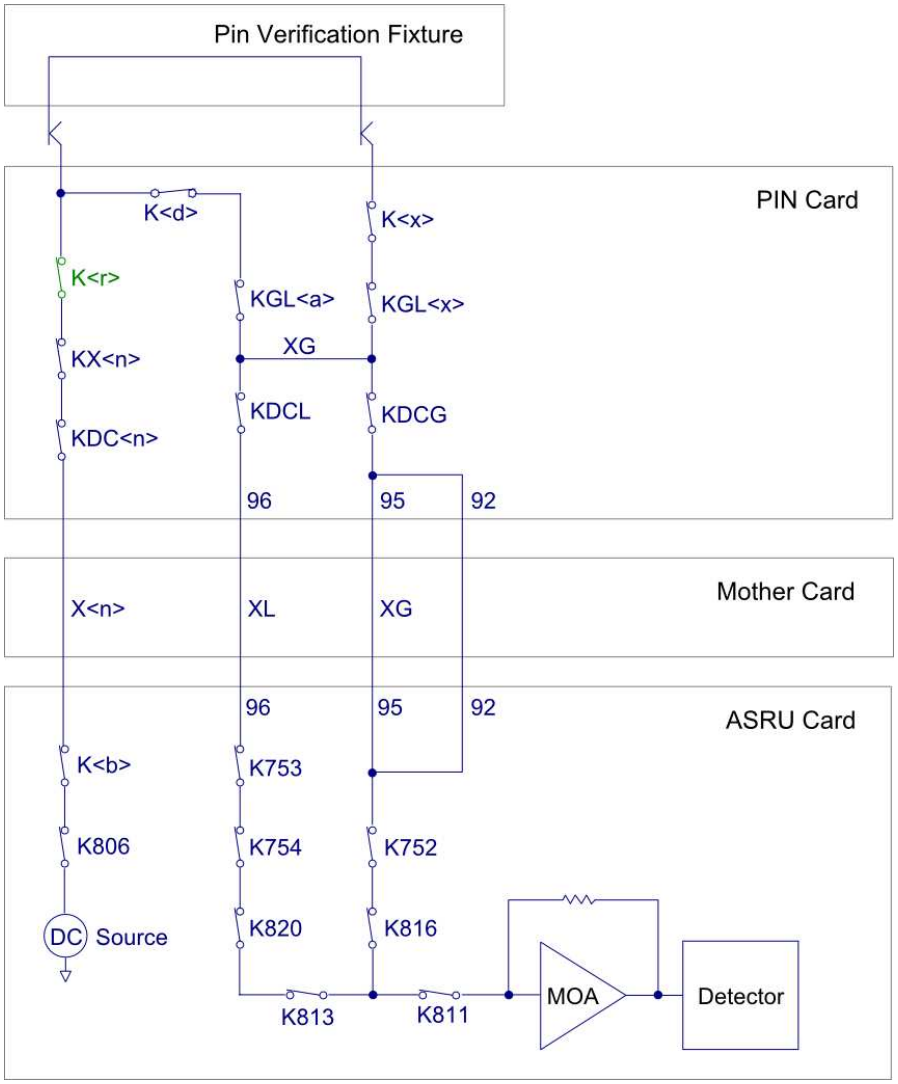
Table 5-94

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
35b	K736	KDC4	KX4	**K18D**	K9D	K9E	KGLD	KGLE
36b	K737	KDC5	KX5	**K10E**	K1E	K1F	KGLE	KGLF
37b	K737	KDC5	KX5	**K11E**	K2E	K2F	KGLE	KGLF
38b	K737	KDC5	KX5	**K12E**	K3E	K3F	KGLE	KGLF
39b	K737	KDC5	KX5	**K13E**	K4E	K4F	KGLE	KGLF
40b	K737	KDC5	KX5	**K14E**	K5E	K5F	KGLE	KGLF
41b	K737	KDC5	KX5	**K15E**	K6E	K6F	KGLE	KGLF
42b	K737	KDC5	KX5	**K16E**	K7E	K7F	KGLE	KGLF
43b	K737	KDC5	KX5	**K17E**	K8E	K8F	KGLE	KGLF
44b	K737	KDC5	KX5	**K18E**	K9E	K9F	KGLE	KGLF
45b	K738	KDC6	KX6	**K10F**	K1F	K1G	KGLF	KGLG
46b	K738	KDC6	KX6	**K11F**	K2F	K2G	KGLF	KGLG
47b	K738	KDC6	KX6	**K12F**	K3F	K3G	KGLF	KGLG
48b	K738	KDC6	KX6	**K13F**	K4F	K4G	KGLF	KGLG
49b	K738	KDC6	KX6	**K14F**	K5F	K5G	KGLF	KGLG
50b	K738	KDC6	KX6	**K15F**	K6F	K6G	KGLF	KGLG
51b	K738	KDC6	KX6	**K16F**	K7F	K7G	KGLF	KGLG
52b	K738	KDC6	KX6	**K17F**	K8F	K8G	KGLF	KGLG
53b	K738	KDC6	KX6	**K18F**	K9F	K9G	KGLF	KGLG
54b	K739	KDC7	KX7	**K10G**	K1G	K1H	KGLG	KGLH
55b	K739	KDC7	KX7	**K11G**	K2G	K2H	KGLG	KGLH
56b	K739	KDC7	KX7	**K12G**	K3G	K3H	KGLG	KGLH
57b	K739	KDC7	KX7	**K13G**	K4G	K4H	KGLG	KGLH
58b	K739	KDC7	KX7	**K14G**	K5G	K5H	KGLG	KGLH
59b	K739	KDC7	KX7	**K15G**	K6G	K6H	KGLG	KGLH
60b	K739	KDC7	KX7	**K16G**	K7G	K7H	KGLG	KGLH
61b	K739	KDC7	KX7	**K17G**	K8G	K8H	KGLG	KGLH
62b	K739	KDC7	KX7	**K18G**	K9G	K9H	KGLG	KGLH
63b	K740	KDC8	KX8	**K10H**	K1H	K1A	KGLH	KGLA
64b	K740	KDC8	KX8	**K11H**	K2H	K2A	KGLH	KGLA

Table 5-94

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
65b	K740	KDC8	KX8	**K12H**	K3H	K3A	KGLH	KGLA
66b	K740	KDC8	KX8	**K13H**	K4H	K4A	KGLH	KGLA
67b	K740	KDC8	KX8	**K14H**	K5H	K5A	KGLH	KGLA
68b	K740	KDC8	KX8	**K15H**	K6H	K6A	KGLH	KGLA
69b	K740	KDC8	KX8	**K16H**	K7H	K7A	KGLH	KGLA
70b	K740	KDC8	KX8	**K17H**	K8H	K8A	KGLH	KGLA
71b	K740	KDC8	KX8	**K18H**	K9H	K9A	KGLH	KGLA

Figure 5-36 T3974



Test 3975

Test Driver to Fixture Interface (MINT) Pin (MUX) Relays can be Closed

Requires: Pin Verification Fixture

This test verifies K1A-H relays can be closed. A test failure is caused when the relay being tested fails to closed. The relays being tested are shown in bold, by subtest, in the table below.

This test is similar to Test 3240, but it contains a redundant path through the Pin Verification Fixture that allows isolating open driver relays from open receiver relays. This test can fail due to dirty fixture interface (MINT) pins.

Figure 5-37 shows the measurement path.

Table 5-95

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
Page A										
0a	K733	K734	KDC1	KDC2	KX1	KX2	K10B	K10A	**K1A**	KGLA
1a	K733	K734	KDC1	KDC2	KX1	KX2	K11B	K11A	**K2A**	KGLA
2a	K733	K734	KDC1	KDC2	KX1	KX2	K12B	K12A	**K3A**	KGLA
3a	K733	K734	KDC1	KDC2	KX1	KX2	K13B	K13A	**K4A**	KGLA
4a	K733	K734	KDC1	KDC2	KX1	KX2	K14B	K14A	**K5A**	KGLA
5a	K733	K734	KDC1	KDC2	KX1	KX2	K15B	K15A	**K6A**	KGLA
6a	K733	K734	KDC1	KDC2	KX1	KX2	K16B	K16A	**K7A**	KGLA
7a	K733	K734	KDC1	KDC2	KX1	KX2	K17B	K17A	**K8A**	KGLA
8a	K733	K734	KDC1	KDC2	KX1	KX2	K18B	K18A	**K9A**	KGLA
9a	K734	K735	KDC2	KDC3	KX2	KX3	K10C	K10B	**K1B**	KGLB
10a	K734	K735	KDC2	KDC3	KX2	KX3	K11C	K11B	**K2B**	KGLB
11a	K734	K735	KDC2	KDC3	KX2	KX3	K12C	K12B	**K3B**	KGLB
12a	K734	K735	KDC2	KDC3	KX2	KX3	K13C	K13B	**K4B**	KGLB
13a	K734	K735	KDC2	KDC3	KX2	KX3	K14C	K14B	**K5B**	KGLB
14a	K734	K735	KDC2	KDC3	KX2	KX3	K15C	K15B	**K6B**	KGLB
15a	K734	K735	KDC2	KDC3	KX2	KX3	K16C	K16B	**K7B**	KGLB
16a	K734	K735	KDC2	KDC3	KX2	KX3	K17C	K17B	**K8B**	KGLB
17a	K734	K735	KDC2	KDC3	KX2	KX3	K18C	K18B	**K9B**	KGLB
18a	K735	K736	KDC3	KDC4	KX3	KX4	K10D	K10C	**K1C**	KGLC

Table 5-95

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
19a	K735	K736	KDC3	KDC4	KX3	KX4	K11D	K11C	**K2C**	KGLC
20a	K735	K736	KDC3	KDC4	KX3	KX4	K12D	K12C	**K3C**	KGLC
21a	K735	K736	KDC3	KDC4	KX3	KX4	K13D	K13C	**K4C**	KGLC
22a	K735	K736	KDC3	KDC4	KX3	KX4	K14D	K14C	**K5C**	KGLC
23a	K735	K736	KDC3	KDC4	KX3	KX4	K15D	K15C	**K6C**	KGLC
24a	K735	K736	KDC3	KDC4	KX3	KX4	K16D	K16C	**K7C**	KGLC
25a	K735	K736	KDC3	KDC4	KX3	KX4	K17D	K17C	**K8C**	KGLC
26a	K735	K736	KDC3	KDC4	KX3	KX4	K18D	K18C	**K9C**	KGLC
27a	K736	K737	KDC4	KDC5	KX4	KX5	K10E	K10D	**K1D**	KGLD
28a	K736	K737	KDC4	KDC5	KX4	KX5	K11E	K11D	**K2D**	KGLD
29a	K736	K737	KDC4	KDC5	KX4	KX5	K12E	K12D	**K3D**	KGLD
30a	K736	K737	KDC4	KDC5	KX4	KX5	K13E	K13D	**K4D**	KGLD
31a	K736	K737	KDC4	KDC5	KX4	KX5	K14E	K14D	**K5D**	KGLD
32a	K736	K737	KDC4	KDC5	KX4	KX5	K15E	K15D	**K6D**	KGLD
33a	K736	K737	KDC4	KDC5	KX4	KX5	K16E	K16D	**K7D**	KGLD
34a	K736	K737	KDC4	KDC5	KX4	KX5	K17E	K17D	**K8D**	KGLD
35a	K736	K737	KDC4	KDC5	KX4	KX5	K18E	K18D	**K9D**	KGLD
36a	K737	K738	KDC5	KDC6	KX5	KX6	K10F	K10E	**K1E**	KGLE
37a	K737	K738	KDC5	KDC6	KX5	KX6	K11F	K11E	**K2E**	KGLE
38a	K737	K738	KDC5	KDC6	KX5	KX6	K12F	K12E	**K3E**	KGLE
39a	K737	K738	KDC5	KDC6	KX5	KX6	K13F	K13E	**K4E**	KGLE
40a	K737	K738	KDC5	KDC6	KX5	KX6	K14F	K14E	**K5E**	KGLE
41a	K737	K738	KDC5	KDC6	KX5	KX6	K15F	K15E	**K6E**	KGLE
42a	K737	K738	KDC5	KDC6	KX5	KX6	K16F	K16E	**K7E**	KGLE
43a	K737	K738	KDC5	KDC6	KX5	KX6	K17F	K17E	**K8E**	KGLE
44a	K737	K738	KDC5	KDC6	KX5	KX6	K18F	K18E	**K9E**	KGLE
45a	K738	K739	KDC6	KDC7	KX6	KX7	K10G	K10F	**K1F**	KGLF
46a	K738	K739	KDC6	KDC7	KX6	KX7	K11G	K11F	**K2F**	KGLF
47a	K738	K739	KDC6	KDC7	KX6	KX7	K12G	K12F	**K3F**	KGLF
48a	K738	K739	KDC6	KDC7	KX6	KX7	K13G	K13F	**K4F**	KGLF

Table 5-95

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
49a	K738	K739	KDC6	KDC7	KX6	KX7	K14G	K14F	**K5F**	KGLF
50a	K738	K739	KDC6	KDC7	KX6	KX7	K15G	K15F	**K6F**	KGLF
51a	K738	K739	KDC6	KDC7	KX6	KX7	K16G	K16F	**K7F**	KGLF
52a	K738	K739	KDC6	KDC7	KX6	KX7	K17G	K17F	**K8F**	KGLF
53a	K738	K739	KDC6	KDC7	KX6	KX7	K18G	K18F	**K9F**	KGLF
54a	K739	K740	KDC7	KDC8	KX7	KX8	K10H	K10G	**K1G**	KGLG
55a	K739	K740	KDC7	KDC8	KX7	KX8	K11H	K11G	**K2G**	KGLG
56a	K739	K740	KDC7	KDC8	KX7	KX8	K12H	K12G	**K3G**	KGLG
57a	K739	K740	KDC7	KDC8	KX7	KX8	K13H	K13G	**K4G**	KGLG
58a	K739	K740	KDC7	KDC8	KX7	KX8	K14H	K14G	**K5G**	KGLG
59a	K739	K740	KDC7	KDC8	KX7	KX8	K15H	K15G	**K6G**	KGLG
60a	K739	K740	KDC7	KDC8	KX7	KX8	K16H	K16G	**K7G**	KGLG
61a	K739	K740	KDC7	KDC8	KX7	KX8	K17H	K17G	**K8G**	KGLG
62a	K739	K740	KDC7	KDC8	KX7	KX8	K18H	K18G	**K9G**	KGLG
63a	K740	K733	KDC8	KDC1	KX8	KX1	K10A	K10H	**K1H**	KGLH
64a	K740	K733	KDC8	KDC1	KX8	KX1	K11A	K11H	**K2H**	KGLH
65a	K740	K733	KDC8	KDC1	KX8	KX1	K12A	K12H	**K3H**	KGLH
66a	K740	K733	KDC8	KDC1	KX8	KX1	K13A	K13H	**K4H**	KGLH
67a	K740	K733	KDC8	KDC1	KX8	KX1	K14A	K14H	**K5H**	KGLH
68a	K740	K733	KDC8	KDC1	KX8	KX1	K15A	K15H	**K6H**	KGLH
69a	K740	K733	KDC8	KDC1	KX8	KX1	K16A	K16H	**K7H**	KGLH
70a	K740	K733	KDC8	KDC1	KX8	KX1	K17A	K17H	**K8H**	KGLH
71a	K740	K733	KDC8	KDC1	KX8	KX1	K18A	K18H	**K9H**	KGLH

Table 5-95

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
Page B										
0b	K733	K734	KDC1	KDC2	KX1	KX2	K10B	K10A	**K1A**	KGLA
1b	K733	K734	KDC1	KDC2	KX1	KX2	K11B	K11A	**K2A**	KGLA
2b	K733	K734	KDC1	KDC2	KX1	KX2	K12B	K12A	**K3A**	KGLA
3b	K733	K734	KDC1	KDC2	KX1	KX2	K13B	K13A	**K4A**	KGLA
4b	K733	K734	KDC1	KDC2	KX1	KX2	K14B	K14A	**K5A**	KGLA
5b	K733	K734	KDC1	KDC2	KX1	KX2	K15B	K15A	**K6A**	KGLA
6b	K733	K734	KDC1	KDC2	KX1	KX2	K16B	K16A	**K7A**	KGLA
7b	K733	K734	KDC1	KDC2	KX1	KX2	K17B	K17A	**K8A**	KGLA
8b	K733	K734	KDC1	KDC2	KX1	KX2	K18B	K18A	**K9A**	KGLA
9b	K734	K735	KDC2	KDC3	KX2	KX3	K10C	K10B	**K1B**	KGLB
10b	K734	K735	KDC2	KDC3	KX2	KX3	K11C	K11B	**K2B**	KGLB
11b	K734	K735	KDC2	KDC3	KX2	KX3	K12C	K12B	**K3B**	KGLB
12b	K734	K735	KDC2	KDC3	KX2	KX3	K13C	K13B	**K4B**	KGLB
13b	K734	K735	KDC2	KDC3	KX2	KX3	K14C	K14B	**K5B**	KGLB
14b	K734	K735	KDC2	KDC3	KX2	KX3	K15C	K15B	**K6B**	KGLB
15b	K734	K735	KDC2	KDC3	KX2	KX3	K16C	K16B	**K7B**	KGLB
16b	K734	K735	KDC2	KDC3	KX2	KX3	K17C	K17B	**K8B**	KGLB
17b	K734	K735	KDC2	KDC3	KX2	KX3	K18C	K18B	**K9B**	KGLB
18b	K735	K736	KDC3	KDC4	KX3	KX4	K10D	K10C	**K1C**	KGLC
19b	K735	K736	KDC3	KDC4	KX3	KX4	K11D	K11C	**K2C**	KGLC
20b	K735	K736	KDC3	KDC4	KX3	KX4	K12D	K12C	**K3C**	KGLC
21b	K735	K736	KDC3	KDC4	KX3	KX4	K13D	K13C	**K4C**	KGLC
22b	K735	K736	KDC3	KDC4	KX3	KX4	K14D	K14C	**K5C**	KGLC
23b	K735	K736	KDC3	KDC4	KX3	KX4	K15D	K15C	**K6C**	KGLC
24b	K735	K736	KDC3	KDC4	KX3	KX4	K16D	K16C	**K7C**	KGLC
25b	K735	K736	KDC3	KDC4	KX3	KX4	K17D	K17C	**K8C**	KGLC
26b	K735	K736	KDC3	KDC4	KX3	KX4	K18D	K18C	**K9C**	KGLC
27b	K736	K737	KDC4	KDC5	KX4	KX5	K10E	K10D	**K1D**	KGLD
28b	K736	K737	KDC4	KDC5	KX4	KX5	K11E	K11D	**K2D**	KGLD

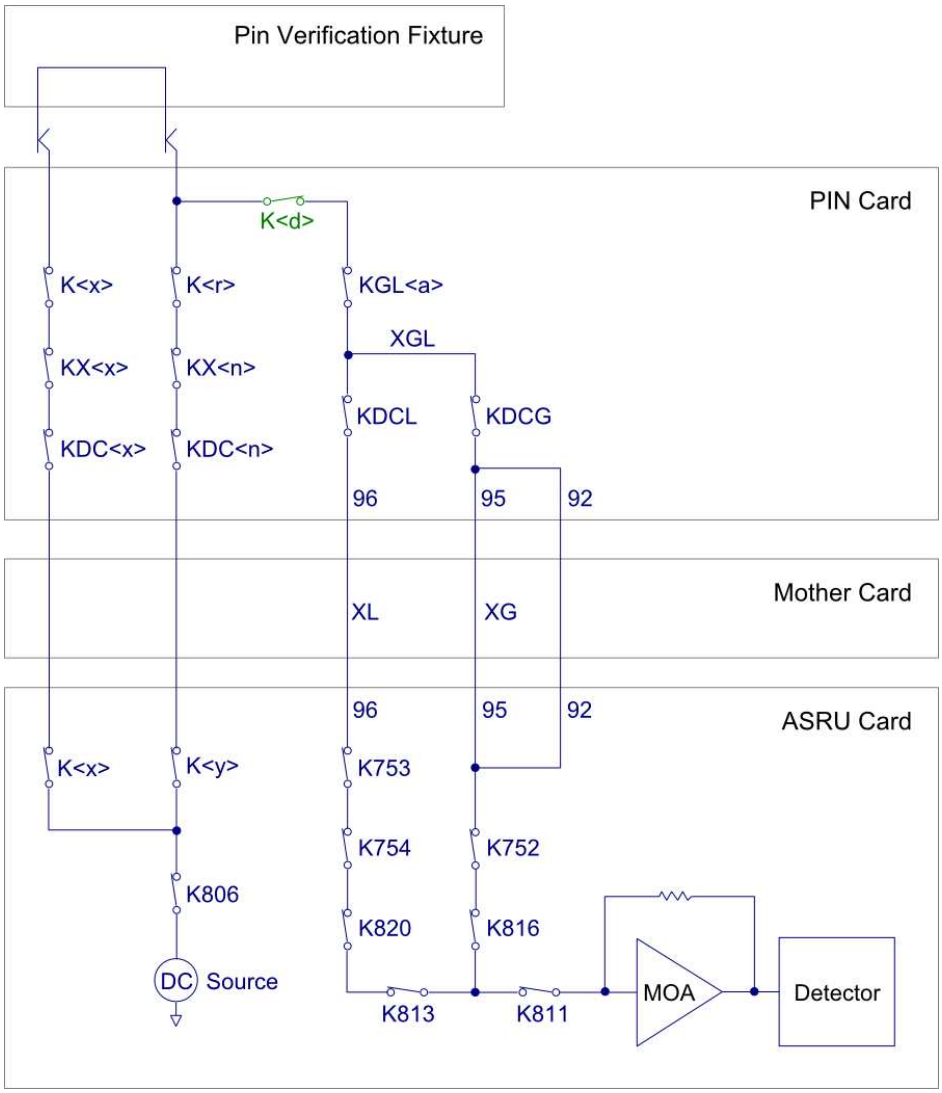
Table 5-95

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
29b	K736	K737	KDC4	KDC5	KX4	KX5	K12E	K12D	**K3D**	KGLD
30b	K736	K737	KDC4	KDC5	KX4	KX5	K13E	K13D	**K4D**	KGLD
31b	K736	K737	KDC4	KDC5	KX4	KX5	K14E	K14D	**K5D**	KGLD
32b	K736	K737	KDC4	KDC5	KX4	KX5	K15E	K15D	**K6D**	KGLD
33b	K736	K737	KDC4	KDC5	KX4	KX5	K16E	K16D	**K7D**	KGLD
34b	K736	K737	KDC4	KDC5	KX4	KX5	K17E	K17D	**K8D**	KGLD
35b	K736	K737	KDC4	KDC5	KX4	KX5	K18E	K18D	**K9D**	KGLD
36b	K737	K738	KDC5	KDC6	KX5	KX6	K10F	K10E	**K1E**	KGLE
37b	K737	K738	KDC5	KDC6	KX5	KX6	K11F	K11E	**K2E**	KGLE
38b	K737	K738	KDC5	KDC6	KX5	KX6	K12F	K12E	**K3E**	KGLE
39b	K737	K738	KDC5	KDC6	KX5	KX6	K13F	K13E	**K4E**	KGLE
40b	K737	K738	KDC5	KDC6	KX5	KX6	K14F	K14E	**K5E**	KGLE
41b	K737	K738	KDC5	KDC6	KX5	KX6	K15F	K15E	**K6E**	KGLE
42b	K737	K738	KDC5	KDC6	KX5	KX6	K16F	K16E	**K7E**	KGLE
43b	K737	K738	KDC5	KDC6	KX5	KX6	K17F	K17E	**K8E**	KGLE
44b	K737	K738	KDC5	KDC6	KX5	KX6	K18F	K18E	**K9E**	KGLE
45b	K738	K739	KDC6	KDC7	KX6	KX7	K10G	K10F	**K1F**	KGLF
46b	K738	K739	KDC6	KDC7	KX6	KX7	K11G	K11F	**K2F**	KGLF
47b	K738	K739	KDC6	KDC7	KX6	KX7	K12G	K12F	**K3F**	KGLF
48b	K738	K739	KDC6	KDC7	KX6	KX7	K13G	K13F	**K4F**	KGLF
49b	K738	K739	KDC6	KDC7	KX6	KX7	K14G	K14F	**K5F**	KGLF
50b	K738	K739	KDC6	KDC7	KX6	KX7	K15G	K15F	**K6F**	KGLF
51b	K738	K739	KDC6	KDC7	KX6	KX7	K16G	K16F	**K7F**	KGLF
52b	K738	K739	KDC6	KDC7	KX6	KX7	K17G	K17F	**K8F**	KGLF
53b	K738	K739	KDC6	KDC7	KX6	KX7	K18G	K18F	**K9F**	KGLF
54b	K739	K740	KDC7	KDC8	KX7	KX8	K10H	K10G	**K1G**	KGLG
55b	K739	K740	KDC7	KDC8	KX7	KX8	K11H	K11G	**K2G**	KGLG
56b	K739	K740	KDC7	KDC8	KX7	KX8	K12H	K12G	**K3G**	KGLG
57b	K739	K740	KDC7	KDC8	KX7	KX8	K13H	K13G	**K4G**	KGLG
58b	K739	K740	KDC7	KDC8	KX7	KX8	K14H	K14G	**K5G**	KGLG

Table 5-95

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
59b	K739	K740	KDC7	KDC8	KX7	KX8	K15H	K15G	**K6G**	KGLG
60b	K739	K740	KDC7	KDC8	KX7	KX8	K16H	K16G	**K7G**	KGLG
61b	K739	K740	KDC7	KDC8	KX7	KX8	K17H	K17G	**K8G**	KGLG
62b	K739	K740	KDC7	KDC8	KX7	KX8	K18H	K18G	**K9G**	KGLG
63b	K740	K733	KDC8	KDC1	KX8	KX1	K10A	K10H	**K1H**	KGLH
64b	K740	K733	KDC8	KDC1	KX8	KX1	K11A	K11H	**K2H**	KGLH
65b	K740	K733	KDC8	KDC1	KX8	KX1	K12A	K12H	**K3H**	KGLH
66b	K740	K733	KDC8	KDC1	KX8	KX1	K13A	K13H	**K4H**	KGLH
67b	K740	K733	KDC8	KDC1	KX8	KX1	K14A	K14H	**K5H**	KGLH
68b	K740	K733	KDC8	KDC1	KX8	KX1	K15A	K15H	**K6H**	KGLH
69b	K740	K733	KDC8	KDC1	KX8	KX1	K16A	K16H	**K7H**	KGLH
70b	K740	K733	KDC8	KDC1	KX8	KX1	K17A	K17H	**K8H**	KGLH
71b	K740	K733	KDC8	KDC1	KX8	KX1	K18A	K18H	**K9H**	KGLH

Figure 5-37 T3975



Test 3976

Test Ground Relays can be Closed

Requires: Pin Verification Fixture

This test verifies KGD relays can be closed. A test failure is caused when the relay being tested fails to closed. The relays being tested are shown in bold, by subtest, in the table below.

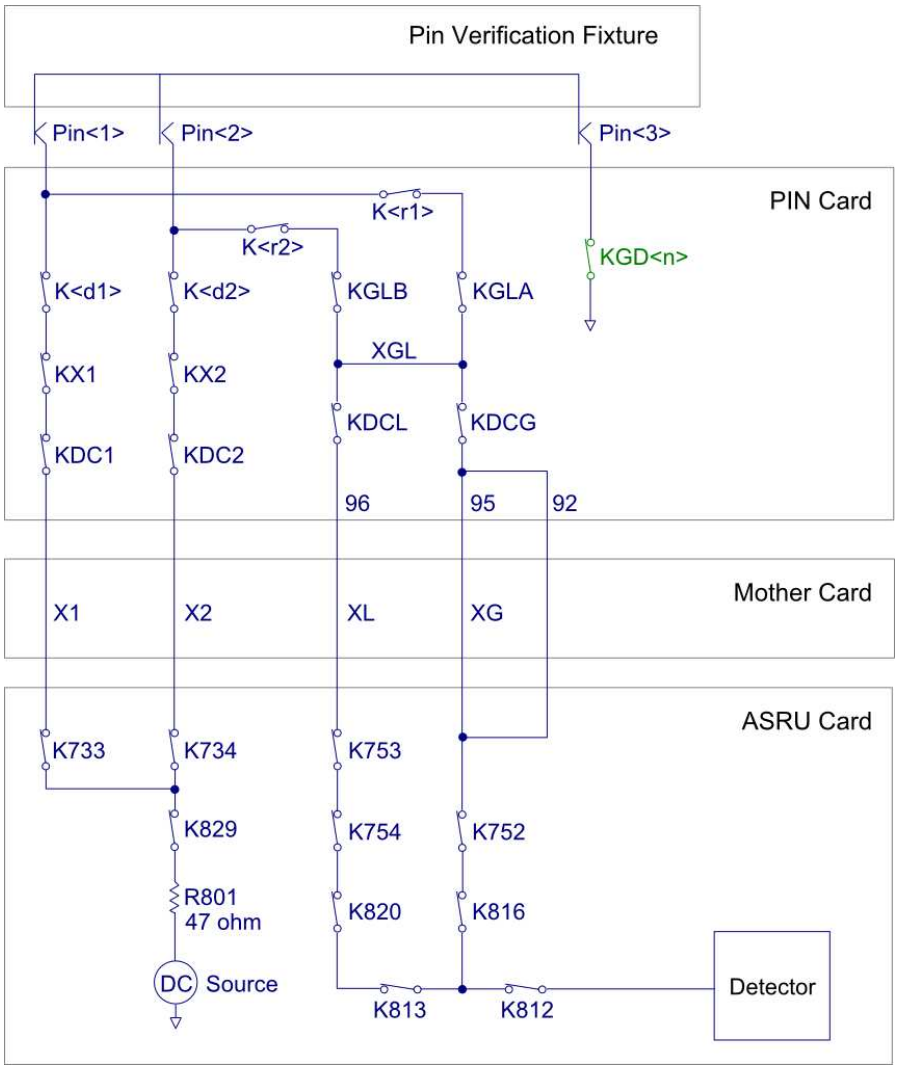
All subtests check the ground relays and their fixture interface (MINT) pins via a path through the Pin Verification Fixture. This test can fail due to dirty fixture interface (MINT) pins.

Figure 5-38 shows the measurement path.

Table 5-96

Subtest	K<r1>	K<d1>	Pin<1>	K<r2>	K<d2>	Pin<2>	Pin<3>	KGD<n>
Page A								
0a	K1A	K10A	1	K1B	K10B	2	19	**KGD1**
1a	K2A	K11A	3	K2B	K11B	4	20	**KGD2**
2a	K3A	K12A	5	K3B	K12B	6	39	**KGD3**
3a	K4A	K13A	7	K4B	K13B	8	40	**KGD4**
4a	K5A	K14A	9	K5B	K14B	10	59	**KGD5**
5a	K6A	K15A	11	K6B	K15B	12	60	**KGD6**
Page B								
0b	K1A	K10A	1	K1B	K10B	2	19	**KGD1**
1b	K2A	K11A	3	K2B	K11B	4	20	**KGD2**
2b	K3A	K12A	5	K3B	K12B	6	39	**KGD3**
3b	K4A	K13A	7	K4B	K13B	8	40	**KGD4**
4b	K5A	K14A	9	K5B	K14B	10	59	**KGD5**
5b	K6A	K15A	11	K6B	K15B	12	60	**KGD6**

Figure 5-38 T3976



Relay with Fixture: Tests 3981-3992

Test 3981

Test Receiver to X-Bus Connect Relays can be Opened

Requires: Pin Verification Fixture

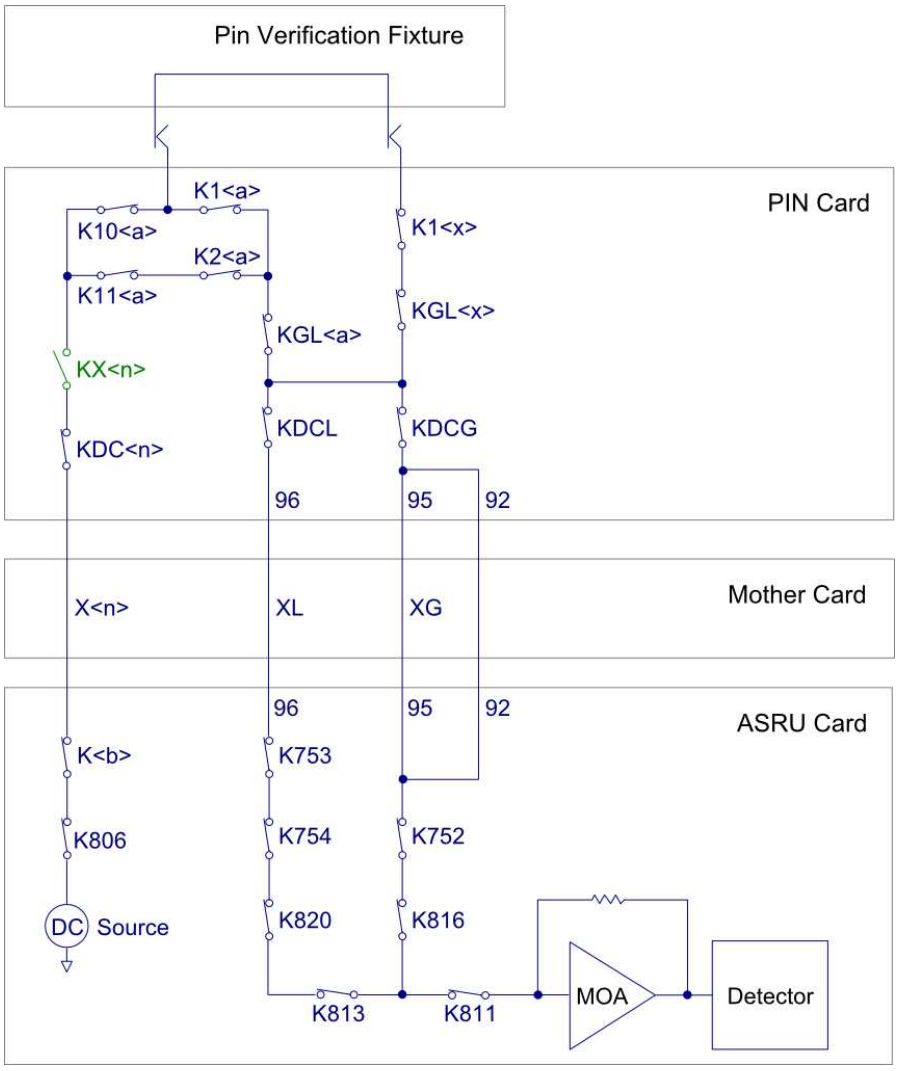
This test verifies KX relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below. Figure 5-39 shows the measurement path.

Test 3310 tests the same relays but does not contain the redundant path through the Pin Verification Fixture.

Table 5-97

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	K1<x>	KGL<a>	KGL<x>
Page A											
0a	K733	X1	KDC1	**KX1**	K1A	K2A	K10A	K11A	K1B	KGLA	KGLB
1a	K734	X2	KDC2	**KX2**	K1B	K2B	K10B	K11B	K1C	KGLB	KGLC
2a	K735	X3	KDC3	**KX3**	K1C	K2C	K10C	K11C	K1D	KGLC	KGLD
3a	K736	X4	KDC4	**KX4**	K1D	K2D	K10D	K11D	K1E	KGLD	KGLE
4a	K737	X5	KDC5	**KX5**	K1E	K2E	K10E	K11E	K1F	KGLE	KGLF
5a	K738	X6	KDC6	**KX6**	K1F	K2F	K10F	K11F	K1G	KGLF	KGLG
6a	K739	X7	KDC7	**KX7**	K1G	K2G	K10G	K11G	K1H	KGLG	KGLH
7a	K740	X8	KDC8	**KX8**	K1H	K2H	K10H	K11H	K1A	KGLH	KGLA
Page B											
0b	K733	X1	KDC1	**KX1**	K1A	K2A	K10A	K11A	K1B	KGLA	KGLB
1b	K734	X2	KDC2	**KX2**	K1B	K2B	K10B	K11B	K1C	KGLB	KGLC
2b	K735	X3	KDC3	**KX3**	K1C	K2C	K10C	K11C	K1D	KGLC	KGLD
3b	K736	X4	KDC4	**KX4**	K1D	K2D	K10D	K11D	K1E	KGLD	KGLE
4b	K737	X5	KDC5	**KX5**	K1E	K2E	K10E	K11E	K1F	KGLE	KGLF
5b	K738	X6	KDC6	**KX6**	K1F	K2F	K10F	K11F	K1G	KGLF	KGLG
6b	K739	X7	KDC7	**KX7**	K1G	K2G	K10G	K11G	K1H	KGLG	KGLH
7b	K740	X8	KDC8	**KX8**	K1H	K2H	K10H	K11H	K1A	KGLH	KGLA

Figure 5-39 T3981



Test 3982

Test X-Bus Disconnect Relays can be Opened

Requires: Pin Verification Fixture

This test verifies KDC relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

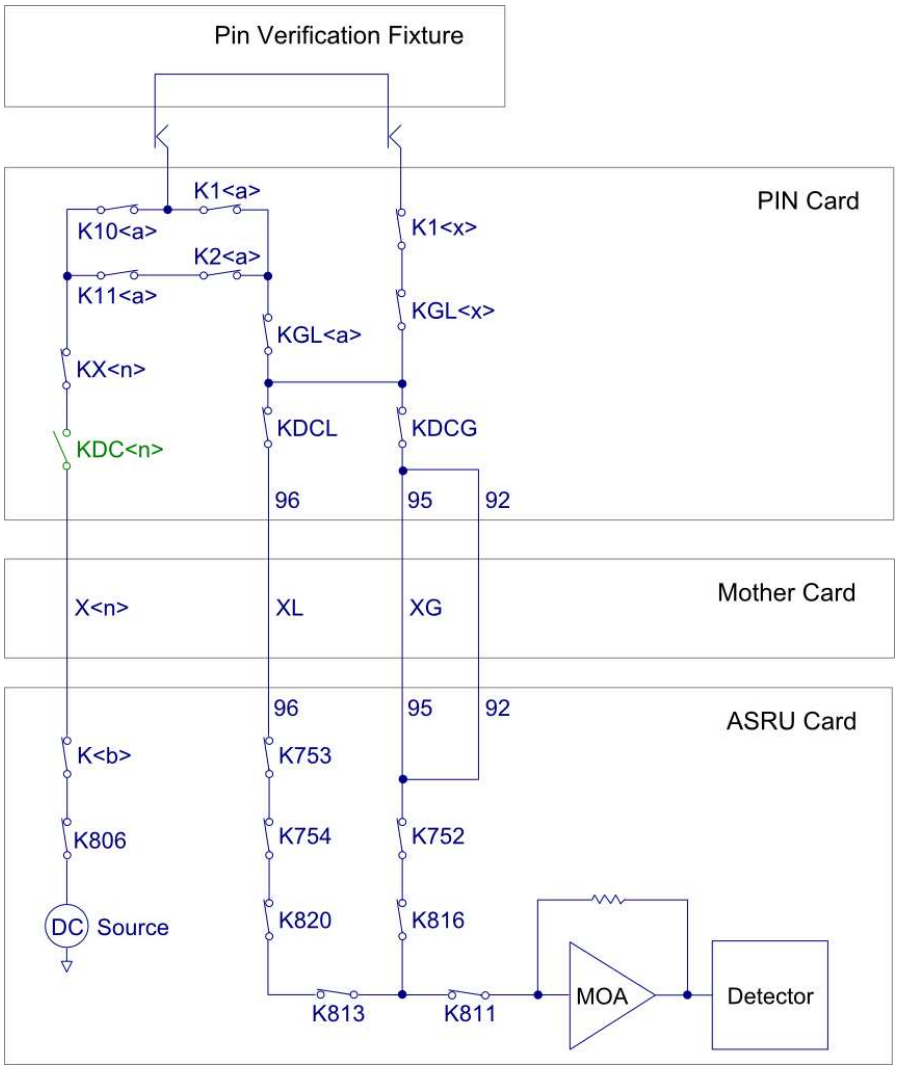
Test 3320 tests the same relays but does not contain the redundant path through the Pin Verification Fixture.

Figure 5-40 shows the measurement path.

Table 5-98

Subtest	K<b>	X<n>	KDC<n>	KX<n>	K1<a>	K2<a>	K10<a>	K11<a>	K1<x>	KGL<a>	KGL<x>
Page A											
0a	K733	X1	**KDC1**	KX1	K1A	K2A	K10A	K11A	K1B	KGLA	KGLB
1a	K734	X2	**KDC2**	KX2	K1B	K2B	K10B	K11B	K1C	KGLB	KGLC
2a	K735	X3	**KDC3**	KX3	K1C	K2C	K10C	K11C	K1D	KGLC	KGLD
3a	K736	X4	**KDC4**	KX4	K1D	K2D	K10D	K11D	K1E	KGLD	KGLE
4a	K737	X5	**KDC5**	KX5	K1E	K2E	K10E	K11E	K1F	KGLE	KGLF
5a	K738	X6	**KDC6**	KX6	K1F	K2F	K10F	K11F	K1G	KGLF	KGLG
6a	K739	X7	**KDC7**	KX7	K1G	K2G	K10G	K11G	K1H	KGLG	KGLH
7a	K740	X8	**KDC8**	KX8	K1H	K2H	K10H	K11H	K1A	KGLH	KGLA
Page B											
0b	K733	X1	**KDC1**	KX1	K1A	K2A	K10A	K11A	K1B	KGLA	KGLB
1b	K734	X2	**KDC2**	KX2	K1B	K2B	K10B	K11B	K1C	KGLB	KGLC
2b	K735	X3	**KDC3**	KX3	K1C	K2C	K10C	K11C	K1D	KGLC	KGLD
3b	K736	X4	**KDC4**	KX4	K1D	K2D	K10D	K11D	K1E	KGLD	KGLE
4b	K737	X5	**KDC5**	KX5	K1E	K2E	K10E	K11E	K1F	KGLE	KGLF
5b	K738	X6	**KDC6**	KX6	K1F	K2F	K10F	K11F	K1G	KGLF	KGLG
6b	K739	X7	**KDC7**	KX7	K1G	K2G	K10G	K11G	K1H	KGLG	KGLH
7b	K740	X8	**KDC8**	KX8	K1H	K2H	K10H	K11H	K1A	KGLH	KGLA

Figure 5-40 T3982



Test 3983

Test Driver to XGL-Bus Connect Relays can be Opened

Requires: Pin Verification Fixture

This test verifies KGL relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

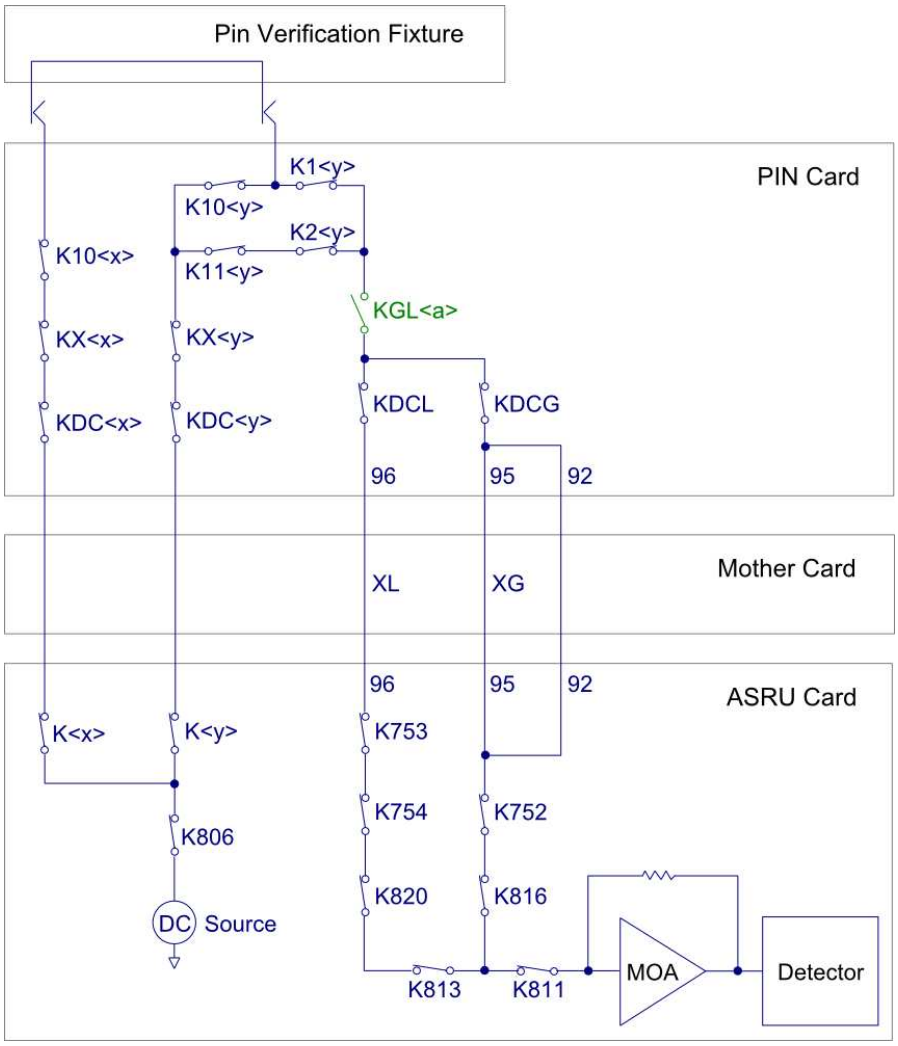
Test 3330 tests the same relays but does not contain the redundant path through the Pin Verification Fixture.

Figure 5-41 shows the measurement path.

Table 5-99

Subtest	K<x>	K<y>	KDC<x>	KDC<y>	KX<x>	KX<y>	K10<x>	K10<y>	K11<y>	K1<y>	K2<y>	KGL<a>
Page A												
0a	K734	K733	KDC2	KDC1	KX2	KX1	K10B	K10A	K11A	K1A	K2A	**KGLA**
1a	K735	K734	KDC3	KDC2	KX3	KX2	K10C	K10B	K11B	K1B	K2B	**KGLB**
2a	K736	K735	KDC4	KDC3	KX4	KX3	K10D	K10C	K11C	K1C	K2C	**KGLC**
3a	K737	K736	KDC5	KDC4	KX5	KX4	K10E	K10D	K11D	K1D	K2D	**KGLD**
4a	K738	K737	KDC6	KDC5	KX6	KX5	K10F	K10E	K11E	K1E	K2E	**KGLE**
5a	K739	K738	KDC7	KDC6	KX7	KX6	K10G	K10F	K11F	K1F	K2F	**KGLF**
6a	K740	K739	KDC8	KDC7	KX8	KX7	K10H	K10G	K11G	K1G	K2G	**KGLG**
7a	K733	K740	KDC1	KDC8	KX1	KX8	K10A	K10H	K11H	K1H	K2H	**KGLH**
Page B												
0b	K734	K733	KDC2	KDC1	KX2	KX1	K10B	K10A	K11A	K1A	K2A	**KGLA**
1b	K735	K734	KDC3	KDC2	KX3	KX2	K10C	K10B	K11B	K1B	K2B	**KGLB**
2b	K736	K735	KDC4	KDC3	KX4	KX3	K10D	K10C	K11C	K1C	K2C	**KGLC**
3b	K737	K736	KDC5	KDC4	KX5	KX4	K10E	K10D	K11D	K1D	K2D	**KGLD**
4b	K738	K737	KDC6	KDC5	KX6	KX5	K10F	K10E	K11E	K1E	K2E	**KGLE**
5b	K739	K738	KDC7	KDC6	KX7	KX6	K10G	K10F	K11F	K1F	K2F	**KGLF**
6b	K740	K739	KDC8	KDC7	KX8	KX7	K10H	K10G	K11G	K1G	K2G	**KGLG**
7b	K733	K740	KDC1	KDC8	KX1	KX8	K10A	K10H	K11H	K1H	K2H	**KGLH**

Figure 5-41 T3983



Test 3985

Test Receiver to Fixture Interface (MINT) Pin (MUX) Relays can be Opened

Requires: Pin Verification Fixture

This test verifies that the K10A-H relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3350 tests the same relays but does not contain the redundant path through the Pin Verification Fixture.

Figure 5-42 shows the measurement path.

Table 5-100

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
Page A								
0a	K733	KDC1	KX1	**K10A**	K1A	K1B	KGLA	KGLB
1a	K733	KDC1	KX1	**K11A**	K2A	K2B	KGLA	KGLB
2a	K733	KDC1	KX1	**K12A**	K3A	K3B	KGLA	KGLB
3a	K733	KDC1	KX1	**K13A**	K4A	K4B	KGLA	KGLB
4a	K733	KDC1	KX1	**K14A**	K5A	K5B	KGLA	KGLB
5a	K733	KDC1	KX1	**K15A**	K6A	K6B	KGLA	KGLB
6a	K733	KDC1	KX1	**K16A**	K7A	K7B	KGLA	KGLB
7a	K733	KDC1	KX1	**K17A**	K8A	K8B	KGLA	KGLB
8a	K733	KDC1	KX1	**K18A**	K9A	K9B	KGLA	KGLB
9a	K734	KDC2	KX2	**K10B**	K1B	K1C	KGLB	KGLC
10a	K734	KDC2	KX2	**K11B**	K2B	K2C	KGLB	KGLC
11a	K734	KDC2	KX2	**K12B**	K3B	K3C	KGLB	KGLC
12a	K734	KDC2	KX2	**K13B**	K4B	K4C	KGLB	KGLC
13a	K734	KDC2	KX2	**K14B**	K5B	K5C	KGLB	KGLC
14a	K734	KDC2	KX2	**K15B**	K6B	K6C	KGLB	KGLC
15a	K734	KDC2	KX2	**K16B**	K7B	K7C	KGLB	KGLC
16a	K734	KDC2	KX2	**K17B**	K8B	K8C	KGLB	KGLC
17a	K734	KDC2	KX2	**K18B**	K9B	K9C	KGLB	KGLC
18a	K735	KDC3	KX3	**K10C**	K1C	K1D	KGLC	KGLD
19a	K735	KDC3	KX3	**K11C**	K2C	K2D	KGLC	KGLD

Table 5-100

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
20a	K735	KDC3	KX3	**K12C**	K3C	K3D	KGLC	KGLD
21a	K735	KDC3	KX3	**K13C**	K4C	K4D	KGLC	KGLD
22a	K735	KDC3	KX3	**K14C**	K5C	K5D	KGLC	KGLD
23a	K735	KDC3	KX3	**K15C**	K6C	K6D	KGLC	KGLD
24a	K735	KDC3	KX3	**K16C**	K7C	K7D	KGLC	KGLD
25a	K735	KDC3	KX3	**K17C**	K8C	K8D	KGLC	KGLD
26a	K735	KDC3	KX3	**K18C**	K9C	K9D	KGLC	KGLD
27a	K736	KDC4	KX4	**K10D**	K1D	K1E	KGLD	KGLE
28a	K736	KDC4	KX4	**K11D**	K2D	K2E	KGLD	KGLE
29a	K736	KDC4	KX4	**K12D**	K3D	K3E	KGLD	KGLE
30a	K736	KDC4	KX4	**K13D**	K4D	K4E	KGLD	KGLE
31a	K736	KDC4	KX4	**K14D**	K5D	K5E	KGLD	KGLE
32a	K736	KDC4	KX4	**K15D**	K6D	K6E	KGLD	KGLE
33a	K736	KDC4	KX4	**K16D**	K7D	K7E	KGLD	KGLE
34a	K736	KDC4	KX4	**K17D**	K8D	K8E	KGLD	KGLE
35a	K736	KDC4	KX4	**K18D**	K9D	K9E	KGLD	KGLE
36a	K737	KDC5	KX5	**K10E**	K1E	K1F	KGLE	KGLF
37a	K737	KDC5	KX5	**K11E**	K2E	K2F	KGLE	KGLF
38a	K737	KDC5	KX5	**K12E**	K3E	K3F	KGLE	KGLF
39a	K737	KDC5	KX5	**K13E**	K4E	K4F	KGLE	KGLF
40a	K737	KDC5	KX5	**K14E**	K5E	K5F	KGLE	KGLF
41a	K737	KDC5	KX5	**K15E**	K6E	K6F	KGLE	KGLF
42a	K737	KDC5	KX5	**K16E**	K7E	K7F	KGLE	KGLF
43a	K737	KDC5	KX5	**K17E**	K8E	K8F	KGLE	KGLF
44a	K737	KDC5	KX5	**K18E**	K9E	K9F	KGLE	KGLF
45a	K738	KDC6	KX6	**K10F**	K1F	K1G	KGLF	KGLG
46a	K738	KDC6	KX6	**K11F**	K2F	K2G	KGLF	KGLG
47a	K738	KDC6	KX6	**K12F**	K3F	K3G	KGLF	KGLG
48a	K738	KDC6	KX6	**K13F**	K4F	K4G	KGLF	KGLG
49a	K738	KDC6	KX6	**K14F**	K5F	K5G	KGLF	KGLG

Table 5-100

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
50a	K738	KDC6	KX6	**K15F**	K6F	K6G	KGLF	KGLG
51a	K738	KDC6	KX6	**K16F**	K7F	K7G	KGLF	KGLG
52a	K738	KDC6	KX6	**K17F**	K8F	K8G	KGLF	KGLG
53a	K738	KDC6	KX6	**K18F**	K9F	K9G	KGLF	KGLG
54a	K739	KDC7	KX7	**K10G**	K1G	K1H	KGLG	KGLH
55a	K739	KDC7	KX7	**K11G**	K2G	K2H	KGLG	KGLH
56a	K739	KDC7	KX7	**K12G**	K3G	K3H	KGLG	KGLH
57a	K739	KDC7	KX7	**K13G**	K4G	K4H	KGLG	KGLH
58a	K739	KDC7	KX7	**K14G**	K5G	K5H	KGLG	KGLH
59a	K739	KDC7	KX7	**K15G**	K6G	K6H	KGLG	KGLH
60a	K739	KDC7	KX7	**K16G**	K7G	K7H	KGLG	KGLH
61a	K739	KDC7	KX7	**K17G**	K8G	K8H	KGLG	KGLH
62a	K739	KDC7	KX7	**K18G**	K9G	K9H	KGLG	KGLH
63a	K740	KDC8	KX8	**K10H**	K1H	K1A	KGLH	KGLA
64a	K740	KDC8	KX8	**K11H**	K2H	K2A	KGLH	KGLA
65a	K740	KDC8	KX8	**K12H**	K3H	K3A	KGLH	KGLA
66a	K740	KDC8	KX8	**K13H**	K4H	K4A	KGLH	KGLA
67a	K740	KDC8	KX8	**K14H**	K5H	K5A	KGLH	KGLA
68a	K740	KDC8	KX8	**K15H**	K6H	K6A	KGLH	KGLA
69a	K740	KDC8	KX8	**K16H**	K7H	K7A	KGLH	KGLA
70a	K740	KDC8	KX8	**K17H**	K8H	K8A	KGLH	KGLA
71a	K740	KDC8	KX8	**K18H**	K9H	K9A	KGLH	KGLA
Page B								
0b	K733	KDC1	KX1	**K10A**	K1A	K1B	KGLA	KGLB
1b	K733	KDC1	KX1	**K11A**	K2A	K2B	KGLA	KGLB
2b	K733	KDC1	KX1	**K12A**	K3A	K3B	KGLA	KGLB
3b	K733	KDC1	KX1	**K13A**	K4A	K4B	KGLA	KGLB
4b	K733	KDC1	KX1	**K14A**	K5A	K5B	KGLA	KGLB
5b	K733	KDC1	KX1	**K15A**	K6A	K6B	KGLA	KGLB
6b	K733	KDC1	KX1	**K16A**	K7A	K7B	KGLA	KGLB

Table 5-100

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
7b	K733	KDC1	KX1	**K17A**	K8A	K8B	KGLA	KGLB
8b	K733	KDC1	KX1	**K18A**	K9A	K9B	KGLA	KGLB
9b	K734	KDC2	KX2	**K10B**	K1B	K1C	KGLB	KGLC
10b	K734	KDC2	KX2	**K11B**	K2B	K2C	KGLB	KGLC
11b	K734	KDC2	KX2	**K12B**	K3B	K3C	KGLB	KGLC
12b	K734	KDC2	KX2	**K13B**	K4B	K4C	KGLB	KGLC
13b	K734	KDC2	KX2	**K14B**	K5B	K5C	KGLB	KGLC
14b	K734	KDC2	KX2	**K15B**	K6B	K6C	KGLB	KGLC
15b	K734	KDC2	KX2	**K16B**	K7B	K7C	KGLB	KGLC
16b	K734	KDC2	KX2	**K17B**	K8B	K8C	KGLB	KGLC
17b	K734	KDC2	KX2	**K18B**	K9B	K9C	KGLB	KGLC
18b	K735	KDC3	KX3	**K10C**	K1C	K1D	KGLC	KGLD
19b	K735	KDC3	KX3	**K11C**	K2C	K2D	KGLC	KGLD
20b	K735	KDC3	KX3	**K12C**	K3C	K3D	KGLC	KGLD
21b	K735	KDC3	KX3	**K13C**	K4C	K4D	KGLC	KGLD
22b	K735	KDC3	KX3	**K14C**	K5C	K5D	KGLC	KGLD
23b	K735	KDC3	KX3	**K15C**	K6C	K6D	KGLC	KGLD
24b	K735	KDC3	KX3	**K16C**	K7C	K7D	KGLC	KGLD
25b	K735	KDC3	KX3	**K17C**	K8C	K8D	KGLC	KGLD
26b	K735	KDC3	KX3	**K18C**	K9C	K9D	KGLC	KGLD
27b	K736	KDC4	KX4	**K10D**	K1D	K1E	KGLD	KGLE
28b	K736	KDC4	KX4	**K11D**	K2D	K2E	KGLD	KGLE
29b	K736	KDC4	KX4	**K12D**	K3D	K3E	KGLD	KGLE
30b	K736	KDC4	KX4	**K13D**	K4D	K4E	KGLD	KGLE
31b	K736	KDC4	KX4	**K14D**	K5D	K5E	KGLD	KGLE
32b	K736	KDC4	KX4	**K15D**	K6D	K6E	KGLD	KGLE
33b	K736	KDC4	KX4	**K16D**	K7D	K7E	KGLD	KGLE
34b	K736	KDC4	KX4	**K17D**	K8D	K8E	KGLD	KGLE
35b	K736	KDC4	KX4	**K18D**	K9D	K9E	KGLD	KGLE
36b	K737	KDC5	KX5	**K10E**	K1E	K1F	KGLE	KGLF

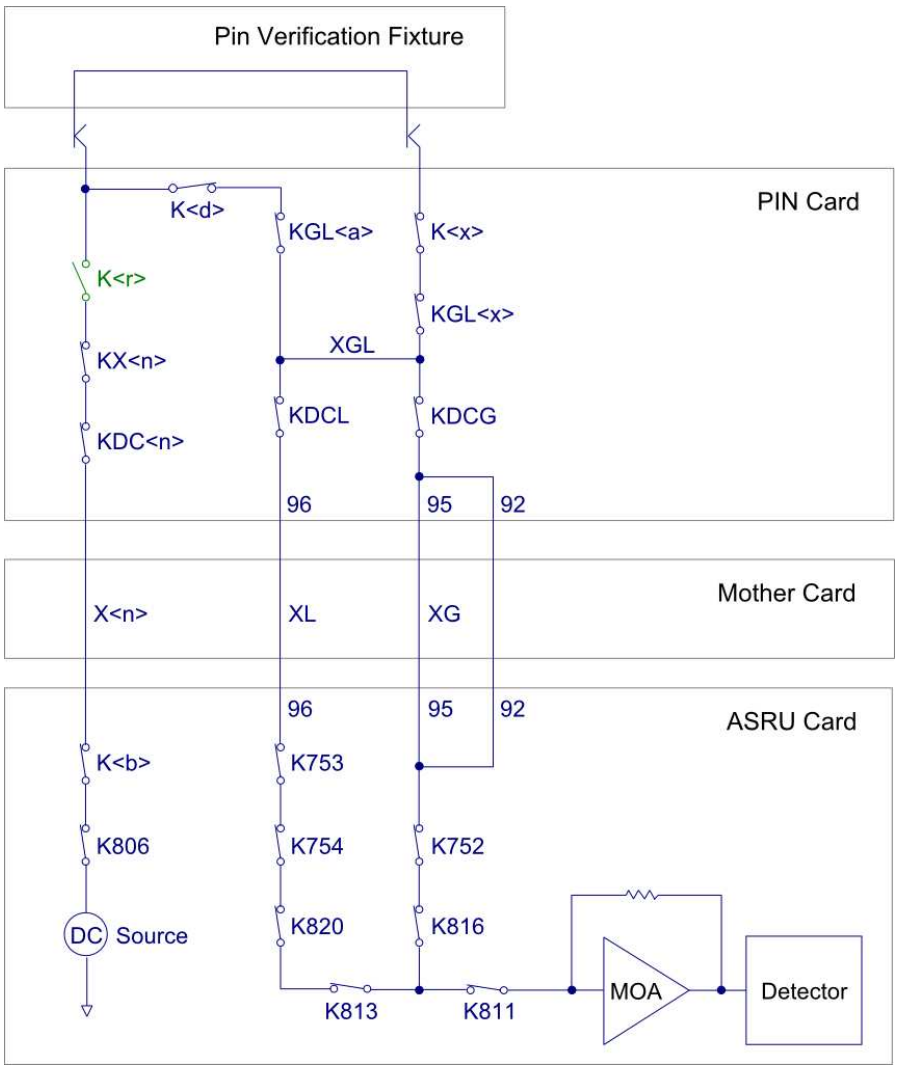
Table 5-100

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
37b	K737	KDC5	KX5	**K11E**	K2E	K2F	KGLE	KGLF
38b	K737	KDC5	KX5	**K12E**	K3E	K3F	KGLE	KGLF
39b	K737	KDC5	KX5	**K13E**	K4E	K4F	KGLE	KGLF
40b	K737	KDC5	KX5	**K14E**	K5E	K5F	KGLE	KGLF
41b	K737	KDC5	KX5	**K15E**	K6E	K6F	KGLE	KGLF
42b	K737	KDC5	KX5	**K16E**	K7E	K7F	KGLE	KGLF
43b	K737	KDC5	KX5	**K17E**	K8E	K8F	KGLE	KGLF
44b	K737	KDC5	KX5	**K18E**	K9E	K9F	KGLE	KGLF
45b	K738	KDC6	KX6	**K10F**	K1F	K1G	KGLF	KGLG
46b	K738	KDC6	KX6	**K11F**	K2F	K2G	KGLF	KGLG
47b	K738	KDC6	KX6	**K12F**	K3F	K3G	KGLF	KGLG
48b	K738	KDC6	KX6	**K13F**	K4F	K4G	KGLF	KGLG
49b	K738	KDC6	KX6	**K14F**	K5F	K5G	KGLF	KGLG
50b	K738	KDC6	KX6	**K15F**	K6F	K6G	KGLF	KGLG
51b	K738	KDC6	KX6	**K16F**	K7F	K7G	KGLF	KGLG
52b	K738	KDC6	KX6	**K17F**	K8F	K8G	KGLF	KGLG
53b	K738	KDC6	KX6	**K18F**	K9F	K9G	KGLF	KGLG
54b	K739	KDC7	KX7	**K10G**	K1G	K1H	KGLG	KGLH
55b	K739	KDC7	KX7	**K11G**	K2G	K2H	KGLG	KGLH
56b	K739	KDC7	KX7	**K12G**	K3G	K3H	KGLG	KGLH
57b	K739	KDC7	KX7	**K13G**	K4G	K4H	KGLG	KGLH
58b	K739	KDC7	KX7	**K14G**	K5G	K5H	KGLG	KGLH
59b	K739	KDC7	KX7	**K15G**	K6G	K6H	KGLG	KGLH
60b	K739	KDC7	KX7	**K16G**	K7G	K7H	KGLG	KGLH
61b	K739	KDC7	KX7	**K17G**	K8G	K8H	KGLG	KGLH
62b	K739	KDC7	KX7	**K18G**	K9G	K9H	KGLG	KGLH
63b	K740	KDC8	KX8	**K10H**	K1H	K1A	KGLH	KGLA
64b	K740	KDC8	KX8	**K11H**	K2H	K2A	KGLH	KGLA
65b	K740	KDC8	KX8	**K12H**	K3H	K3A	KGLH	KGLA
66b	K740	KDC8	KX8	**K13H**	K4H	K4A	KGLH	KGLA

Table 5-100

Subtest	K<b>	KDC<n>	KX<n>	K<r>	K<d>	K<x>	KGL<a>	KGL<x>
67b	K740	KDC8	KX8	**K14H**	K5H	K5A	KGLH	KGLA
68b	K740	KDC8	KX8	**K15H**	K6H	K6A	KGLH	KGLA
69b	K740	KDC8	KX8	**K16H**	K7H	K7A	KGLH	KGLA
70b	K740	KDC8	KX8	**K17H**	K8H	K8A	KGLH	KGLA
71b	K740	KDC8	KX8	**K18H**	K9H	K9A	KGLH	KGLA

Figure 5-42 T3985



Test 3986

Test Driver Fixture Interface (MINT) Pin (MUX) Relays can be Opened

Requires: Pin Verification Fixture

This test verifies that the K1A-H relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Test 3360 tests the same relays but does not contain the redundant path through the Pin Verification Fixture.

Figure 5-43 shows the measurement path.

Table 5-101

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
Page A										
0a	K733	K734	KDC1	KDC2	KX1	KX2	K10B	K10A	**K1A**	KGLA
1a	K733	K734	KDC1	KDC2	KX1	KX2	K11B	K11A	**K2A**	KGLA
2a	K733	K734	KDC1	KDC2	KX1	KX2	K12B	K12A	**K3A**	KGLA
3a	K733	K734	KDC1	KDC2	KX1	KX2	K13B	K13A	**K4A**	KGLA
4a	K733	K734	KDC1	KDC2	KX1	KX2	K14B	K14A	**K5A**	KGLA
5a	K733	K734	KDC1	KDC2	KX1	KX2	K15B	K15A	**K6A**	KGLA
6a	K733	K734	KDC1	KDC2	KX1	KX2	K16B	K16A	**K7A**	KGLA
7a	K733	K734	KDC1	KDC2	KX1	KX2	K17B	K17A	**K8A**	KGLA
8a	K733	K734	KDC1	KDC2	KX1	KX2	K18B	K18A	**K9A**	KGLA
9a	K734	K735	KDC2	KDC3	KX2	KX3	K10C	K10B	**K1B**	KGLB
10a	K734	K735	KDC2	KDC3	KX2	KX3	K11C	K11B	**K2B**	KGLB
11a	K734	K735	KDC2	KDC3	KX2	KX3	K12C	K12B	**K3B**	KGLB
12a	K734	K735	KDC2	KDC3	KX2	KX3	K13C	K13B	**K4B**	KGLB
13a	K734	K735	KDC2	KDC3	KX2	KX3	K14C	K14B	**K5B**	KGLB
14a	K734	K735	KDC2	KDC3	KX2	KX3	K15C	K15B	**K6B**	KGLB
15a	K734	K735	KDC2	KDC3	KX2	KX3	K16C	K16B	**K7B**	KGLB
16a	K734	K735	KDC2	KDC3	KX2	KX3	K17C	K17B	**K8B**	KGLB
17a	K734	K735	KDC2	KDC3	KX2	KX3	K18C	K18B	**K9B**	KGLB
18a	K735	K736	KDC3	KDC4	KX3	KX4	K10D	K10C	**K1C**	KGLC
19a	K735	K736	KDC3	KDC4	KX3	KX4	K11D	K11C	**K2C**	KGLC

Table 5-101

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
20a	K735	K736	KDC3	KDC4	KX3	KX4	K12D	K12C	**K3C**	KGLC
21a	K735	K736	KDC3	KDC4	KX3	KX4	K13D	K13C	**K4C**	KGLC
22a	K735	K736	KDC3	KDC4	KX3	KX4	K14D	K14C	**K5C**	KGLC
23a	K735	K736	KDC3	KDC4	KX3	KX4	K15D	K15C	**K6C**	KGLC
24a	K735	K736	KDC3	KDC4	KX3	KX4	K16D	K16C	**K7C**	KGLC
25a	K735	K736	KDC3	KDC4	KX3	KX4	K17D	K17C	**K8C**	KGLC
26a	K735	K736	KDC3	KDC4	KX3	KX4	K18D	K18C	**K9C**	KGLC
27a	K736	K737	KDC4	KDC5	KX4	KX5	K10E	K10D	**K1D**	KGLD
28a	K736	K737	KDC4	KDC5	KX4	KX5	K11E	K11D	**K2D**	KGLD
29a	K736	K737	KDC4	KDC5	KX4	KX5	K12E	K12D	**K3D**	KGLD
30a	K736	K737	KDC4	KDC5	KX4	KX5	K13E	K13D	**K4D**	KGLD
31a	K736	K737	KDC4	KDC5	KX4	KX5	K14E	K14D	**K5D**	KGLD
32a	K736	K737	KDC4	KDC5	KX4	KX5	K15E	K15D	**K6D**	KGLD
33a	K736	K737	KDC4	KDC5	KX4	KX5	K16E	K16D	**K7D**	KGLD
34a	K736	K737	KDC4	KDC5	KX4	KX5	K17E	K17D	**K8D**	KGLD
35a	K736	K737	KDC4	KDC5	KX4	KX5	K18E	K18D	**K9D**	KGLD
36a	K737	K738	KDC5	KDC6	KX5	KX6	K10F	K10E	**K1E**	KGLE
37a	K737	K738	KDC5	KDC6	KX5	KX6	K11F	K11E	**K2E**	KGLE
38a	K737	K738	KDC5	KDC6	KX5	KX6	K12F	K12E	**K3E**	KGLE
39a	K737	K738	KDC5	KDC6	KX5	KX6	K13F	K13E	**K4E**	KGLE
40a	K737	K738	KDC5	KDC6	KX5	KX6	K14F	K14E	**K5E**	KGLE
41a	K737	K738	KDC5	KDC6	KX5	KX6	K15F	K15E	**K6E**	KGLE
42a	K737	K738	KDC5	KDC6	KX5	KX6	K16F	K16E	**K7E**	KGLE
43a	K737	K738	KDC5	KDC6	KX5	KX6	K17F	K17E	**K8E**	KGLE
44a	K737	K738	KDC5	KDC6	KX5	KX6	K18F	K18E	**K9E**	KGLE
45a	K738	K739	KDC6	KDC7	KX6	KX7	K10G	K10F	**K1F**	KGLF
46a	K738	K739	KDC6	KDC7	KX6	KX7	K11G	K11F	**K2F**	KGLF
47a	K738	K739	KDC6	KDC7	KX6	KX7	K12G	K12F	**K3F**	KGLF
48a	K738	K739	KDC6	KDC7	KX6	KX7	K13G	K13F	**K4F**	KGLF
49a	K738	K739	KDC6	KDC7	KX6	KX7	K14G	K14F	**K5F**	KGLF

Table 5-101

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
50a	K738	K739	KDC6	KDC7	KX6	KX7	K15G	K15F	**K6F**	KGLF
51a	K738	K739	KDC6	KDC7	KX6	KX7	K16G	K16F	**K7F**	KGLF
52a	K738	K739	KDC6	KDC7	KX6	KX7	K17G	K17F	**K8F**	KGLF
53a	K738	K739	KDC6	KDC7	KX6	KX7	K18G	K18F	**K9F**	KGLF
54a	K739	K740	KDC7	KDC8	KX7	KX8	K10H	K10G	**K1G**	KGLG
55a	K739	K740	KDC7	KDC8	KX7	KX8	K11H	K11G	**K2G**	KGLG
56a	K739	K740	KDC7	KDC8	KX7	KX8	K12H	K12G	**K3G**	KGLG
57a	K739	K740	KDC7	KDC8	KX7	KX8	K13H	K13G	**K4G**	KGLG
58a	K739	K740	KDC7	KDC8	KX7	KX8	K14H	K14G	**K5G**	KGLG
59a	K739	K740	KDC7	KDC8	KX7	KX8	K15H	K15G	**K6G**	KGLG
60a	K739	K740	KDC7	KDC8	KX7	KX8	K16H	K16G	**K7G**	KGLG
61a	K739	K740	KDC7	KDC8	KX7	KX8	K17H	K17G	**K8G**	KGLG
62a	K739	K740	KDC7	KDC8	KX7	KX8	K18H	K18G	**K9G**	KGLG
63a	K740	K733	KDC8	KDC1	KX8	KX1	K10A	K10H	**K1H**	KGLH
64a	K740	K733	KDC8	KDC1	KX8	KX1	K11A	K11H	**K2H**	KGLH
65a	K740	K733	KDC8	KDC1	KX8	KX1	K12A	K12H	**K3H**	KGLH
66a	K740	K733	KDC8	KDC1	KX8	KX1	K13A	K13H	**K4H**	KGLH
67a	K740	K733	KDC8	KDC1	KX8	KX1	K14A	K14H	**K5H**	KGLH
68a	K740	K733	KDC8	KDC1	KX8	KX1	K15A	K15H	**K6H**	KGLH
69a	K740	K733	KDC8	KDC1	KX8	KX1	K16A	K16H	**K7H**	KGLH
70a	K740	K733	KDC8	KDC1	KX8	KX1	K17A	K17H	**K8H**	KGLH
71a	K740	K733	KDC8	KDC1	KX8	KX1	K18A	K18H	**K9H**	KGLH
Page B										
0b	K733	K734	KDC1	KDC2	KX1	KX2	K10B	K10A	**K1A**	KGLA
1b	K733	K734	KDC1	KDC2	KX1	KX2	K11B	K11A	**K2A**	KGLA
2b	K733	K734	KDC1	KDC2	KX1	KX2	K12B	K12A	**K3A**	KGLA
3b	K733	K734	KDC1	KDC2	KX1	KX2	K13B	K13A	**K4A**	KGLA
4b	K733	K734	KDC1	KDC2	KX1	KX2	K14B	K14A	**K5A**	KGLA
5b	K733	K734	KDC1	KDC2	KX1	KX2	K15B	K15A	**K6A**	KGLA
6b	K733	K734	KDC1	KDC2	KX1	KX2	K16B	K16A	**K7A**	KGLA

Table 5-101

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
7b	K733	K734	KDC1	KDC2	KX1	KX2	K17B	K17A	**K8A**	KGLA
8b	K733	K734	KDC1	KDC2	KX1	KX2	K18B	K18A	**K9A**	KGLA
9b	K734	K735	KDC2	KDC3	KX2	KX3	K10C	K10B	**K1B**	KGLB
10b	K734	K735	KDC2	KDC3	KX2	KX3	K11C	K11B	**K2B**	KGLB
11b	K734	K735	KDC2	KDC3	KX2	KX3	K12C	K12B	**K3B**	KGLB
12b	K734	K735	KDC2	KDC3	KX2	KX3	K13C	K13B	**K4B**	KGLB
13b	K734	K735	KDC2	KDC3	KX2	KX3	K14C	K14B	**K5B**	KGLB
14b	K734	K735	KDC2	KDC3	KX2	KX3	K15C	K15B	**K6B**	KGLB
15b	K734	K735	KDC2	KDC3	KX2	KX3	K16C	K16B	**K7B**	KGLB
16b	K734	K735	KDC2	KDC3	KX2	KX3	K17C	K17B	**K8B**	KGLB
17b	K734	K735	KDC2	KDC3	KX2	KX3	K18C	K18B	**K9B**	KGLB
18b	K735	K736	KDC3	KDC4	KX3	KX4	K10D	K10C	**K1C**	KGLC
19b	K735	K736	KDC3	KDC4	KX3	KX4	K11D	K11C	**K2C**	KGLC
20b	K735	K736	KDC3	KDC4	KX3	KX4	K12D	K12C	**K3C**	KGLC
21b	K735	K736	KDC3	KDC4	KX3	KX4	K13D	K13C	**K4C**	KGLC
22b	K735	K736	KDC3	KDC4	KX3	KX4	K14D	K14C	**K5C**	KGLC
23b	K735	K736	KDC3	KDC4	KX3	KX4	K15D	K15C	**K6C**	KGLC
24b	K735	K736	KDC3	KDC4	KX3	KX4	K16D	K16C	**K7C**	KGLC
25b	K735	K736	KDC3	KDC4	KX3	KX4	K17D	K17C	**K8C**	KGLC
26b	K735	K736	KDC3	KDC4	KX3	KX4	K18D	K18C	**K9C**	KGLC
27b	K736	K737	KDC4	KDC5	KX4	KX5	K10E	K10D	**K1D**	KGLD
28b	K736	K737	KDC4	KDC5	KX4	KX5	K11E	K11D	**K2D**	KGLD
29b	K736	K737	KDC4	KDC5	KX4	KX5	K12E	K12D	**K3D**	KGLD
30b	K736	K737	KDC4	KDC5	KX4	KX5	K13E	K13D	**K4D**	KGLD
31b	K736	K737	KDC4	KDC5	KX4	KX5	K14E	K14D	**K5D**	KGLD
32b	K736	K737	KDC4	KDC5	KX4	KX5	K15E	K15D	**K6D**	KGLD
33b	K736	K737	KDC4	KDC5	KX4	KX5	K16E	K16D	**K7D**	KGLD
34b	K736	K737	KDC4	KDC5	KX4	KX5	K17E	K17D	**K8D**	KGLD
35b	K736	K737	KDC4	KDC5	KX4	KX5	K18E	K18D	**K9D**	KGLD
36b	K737	K738	KDC5	KDC6	KX5	KX6	K10F	K10E	**K1E**	KGLE

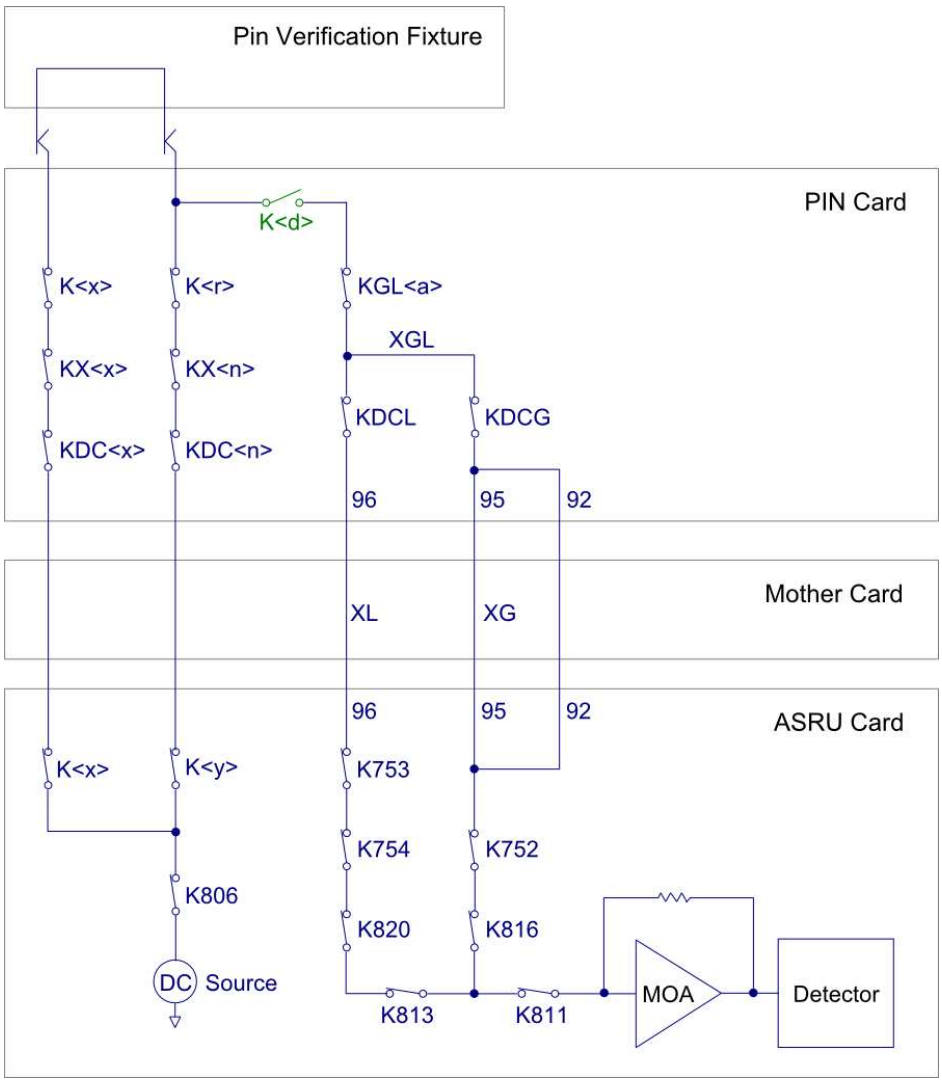
Table 5-101

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
37b	K737	K738	KDC5	KDC6	KX5	KX6	K11F	K11E	**K2E**	KGLE
38b	K737	K738	KDC5	KDC6	KX5	KX6	K12F	K12E	**K3E**	KGLE
39b	K737	K738	KDC5	KDC6	KX5	KX6	K13F	K13E	**K4E**	KGLE
40b	K737	K738	KDC5	KDC6	KX5	KX6	K14F	K14E	**K5E**	KGLE
41b	K737	K738	KDC5	KDC6	KX5	KX6	K15F	K15E	**K6E**	KGLE
42b	K737	K738	KDC5	KDC6	KX5	KX6	K16F	K16E	**K7E**	KGLE
43b	K737	K738	KDC5	KDC6	KX5	KX6	K17F	K17E	**K8E**	KGLE
44b	K737	K738	KDC5	KDC6	KX5	KX6	K18F	K18E	**K9E**	KGLE
45b	K738	K739	KDC6	KDC7	KX6	KX7	K10G	K10F	**K1F**	KGLF
46b	K738	K739	KDC6	KDC7	KX6	KX7	K11G	K11F	**K2F**	KGLF
47b	K738	K739	KDC6	KDC7	KX6	KX7	K12G	K12F	**K3F**	KGLF
48b	K738	K739	KDC6	KDC7	KX6	KX7	K13G	K13F	**K4F**	KGLF
49b	K738	K739	KDC6	KDC7	KX6	KX7	K14G	K14F	**K5F**	KGLF
50b	K738	K739	KDC6	KDC7	KX6	KX7	K15G	K15F	**K6F**	KGLF
51b	K738	K739	KDC6	KDC7	KX6	KX7	K16G	K16F	**K7F**	KGLF
52b	K738	K739	KDC6	KDC7	KX6	KX7	K17G	K17F	**K8F**	KGLF
53b	K738	K739	KDC6	KDC7	KX6	KX7	K18G	K18F	**K9F**	KGLF
54b	K739	K740	KDC7	KDC8	KX7	KX8	K10H	K10G	**K1G**	KGLG
55b	K739	K740	KDC7	KDC8	KX7	KX8	K11H	K11G	**K2G**	KGLG
56b	K739	K740	KDC7	KDC8	KX7	KX8	K12H	K12G	**K3G**	KGLG
57b	K739	K740	KDC7	KDC8	KX7	KX8	K13H	K13G	**K4G**	KGLG
58b	K739	K740	KDC7	KDC8	KX7	KX8	K14H	K14G	**K5G**	KGLG
59b	K739	K740	KDC7	KDC8	KX7	KX8	K15H	K15G	**K6G**	KGLG
60b	K739	K740	KDC7	KDC8	KX7	KX8	K16H	K16G	**K7G**	KGLG
61b	K739	K740	KDC7	KDC8	KX7	KX8	K17H	K17G	**K8G**	KGLG
62b	K739	K740	KDC7	KDC8	KX7	KX8	K18H	K18G	**K9G**	KGLG
63b	K740	K733	KDC8	KDC1	KX8	KX1	K10A	K10H	**K1H**	KGLH
64b	K740	K733	KDC8	KDC1	KX8	KX1	K11A	K11H	**K2H**	KGLH
65b	K740	K733	KDC8	KDC1	KX8	KX1	K12A	K12H	**K3H**	KGLH
66b	K740	K733	KDC8	KDC1	KX8	KX1	K13A	K13H	**K4H**	KGLH

Table 5-101

Subtest	K<b>	K<c>	KDC<n>	KDC<x>	KX<n>	KX<x>	K<x>	K<r>	K<d>	KGL<a>
67b	K740	K733	KDC8	KDC1	KX8	KX1	K14A	K14H	**K5H**	KGLH
68b	K740	K733	KDC8	KDC1	KX8	KX1	K15A	K15H	**K6H**	KGLH
69b	K740	K733	KDC8	KDC1	KX8	KX1	K16A	K16H	**K7H**	KGLH
70b	K740	K733	KDC8	KDC1	KX8	KX1	K17A	K17H	**K8H**	KGLH
71b	K740	K733	KDC8	KDC1	KX8	KX1	K18A	K18H	**K9H**	KGLH

Figure 5-43 T3986



Test 3987

Test Ground to Fixture Interface (MINT) Pin Relays can be Opened

Requires: Pin Verification Fixture

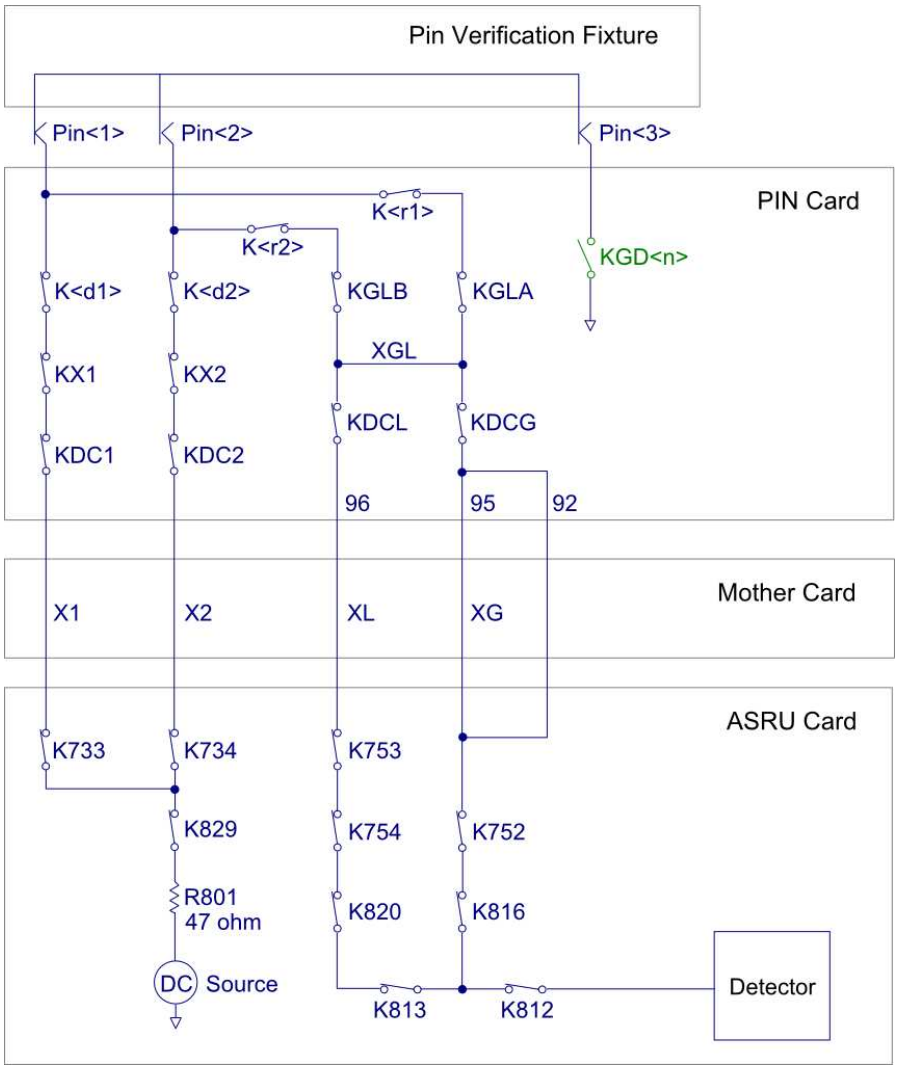
This test verifies KGD relays can be opened. A test failure is caused when the relay being tested fails to open. The relays being tested are shown in bold, by subtest, in the table below.

Figure 5-44 shows the measurement path.

Table 5-102

Subtest	K<r1>	K<d1>	Pin<1>	K<r2>	K<d2>	Pin<2>	Pin<3>	KGD<n>
Page A								
0a	K1A	K10A	1	K1B	K10B	2	19	**KGD1**
1a	K2A	K11A	3	K2B	K11B	4	20	**KGD2**
2a	K3A	K12A	5	K3B	K12B	6	39	**KGD3**
3a	K4A	K13A	7	K4B	K13B	8	40	**KGD4**
4a	K5A	K14A	9	K5B	K14B	10	59	**KGD5**
5a	K6A	K15A	11	K6B	K15B	12	60	**KGD6**
Page B								
0b	K1A	K10A	1	K1B	K10B	2	19	**KGD1**
1b	K2A	K11A	3	K2B	K11B	4	20	**KGD2**
2b	K3A	K12A	5	K3B	K12B	6	39	**KGD3**
3b	K4A	K13A	7	K4B	K13B	8	40	**KGD4**
4b	K5A	K14A	9	K5B	K14B	10	59	**KGD5**
5b	K6A	K15A	11	K6B	K15B	12	60	**KGD6**

Figure 5-44 T3987



Test 3991

Verify Fixture Interface (MINT) Pins

Requires: Pin Verification Fixture

This test verifies the fixture interface (MINT) pins. It is the only test that explicitly tests the pins.

Table 5-103

Subtest	Pin	Subtest	Pin	Subtest	Pin
Side A					
0a	62a	24a	14a	48a	47a
1a	64a	25a	16a	49a	49a
2a	66a	26a	18a	50a	51a
3a	68a	27a	21a	51a	53a
4a	70a	28a	23a	52a	55a
5a	72a	29a	25a	53a	57a
6a	74a	30a	27a	54a	42a
7a	76a	31a	29a	55a	44a
8a	78a	32a	31a	56a	46a
9a	1a	33a	33a	57a	48a
10a	3a	34a	35a	58a	50a
11a	5a	35a	37a	59a	52a
12a	7a	36a	22a	60a	54a
13a	9a	37a	24a	61a	56a
14a	11a	38a	26a	62a	58a
15a	13a	39a	28a	63a	61a
16a	15a	40a	30a	64a	63a
17a	17a	41a	32a	65a	65a
18a	2a	42a	34a	66a	67a
19a	4a	43a	36a	67a	69a
20a	6a	44a	38a	68a	71a
21a	8a	45a	41a	69a	73a
22a	10a	46a	43a	70a	75a

Table 5-103

Subtest	Pin	Subtest	Pin	Subtest	Pin
23a	12a	47a	45a	71a	77a
Side B					
0b	62b	24b	14b	48b	47b
1b	64b	25b	16b	49b	49b
2b	66b	26b	18b	50b	51b
3b	68b	27b	21b	51b	53b
4b	70b	28b	23b	52b	55b
5b	72b	29b	25b	53b	57b
6b	74b	30b	27b	54b	42b
7b	76b	31b	29b	55b	44b
8b	78b	32b	31b	56b	46b
9b	1b	33b	33b	57b	48b
10b	3b	34b	35b	58b	50b
11b	5b	35b	37b	59b	52b
12b	7b	36b	22b	60b	54b
13b	9b	37b	24b	61b	56b
14b	11b	38b	26b	62b	58b
15b	13b	39b	28b	63b	61b
16b	15b	40b	30b	64b	63b
17b	17b	41b	32b	65b	65b
18b	2b	42b	34b	66b	67b
19b	4b	43b	36b	67b	69b
20b	6b	44b	38b	68b	71b
21b	8b	45b	41b	69b	73b
22b	10b	46b	43b	70b	75b
23b	12b	47b	45b	71b	77b

Test 3992

Verify No Short Between Fixture Interface (MINT) Pins

This test verifies that there are no shorts between adjacent MINT pins. It makes a resistance measurement between adjacent pairs of pins and passes if the result is greater than 10 kohms.

It cannot detect a short between KGD (digital ground) pins, but it can detect a short between KGD and adjacent hybrid pins.

The test is run without the pin verification fixture. If a fixture is present, it is released.

NOTE Overriding the pin verification fixture requirement on this test will cause false failures since the pin verification fixture purposely shorts MINT pins together.

An error message would resemble the following:

```
Test 3992, Subtest 75, Module 3, Slot 2b FAILED.
Short detected between MINT pins 77 and 78
  Low Limit:          1.00000E+04
  Result Received:    2.06013E+00 Ohms
  High Limit:         1.00000E+30
```