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Reconfigurable Hardware Components in the Context of Cloud-Architectures

Los Angeles // 26. July 2018

Introduction and motivation

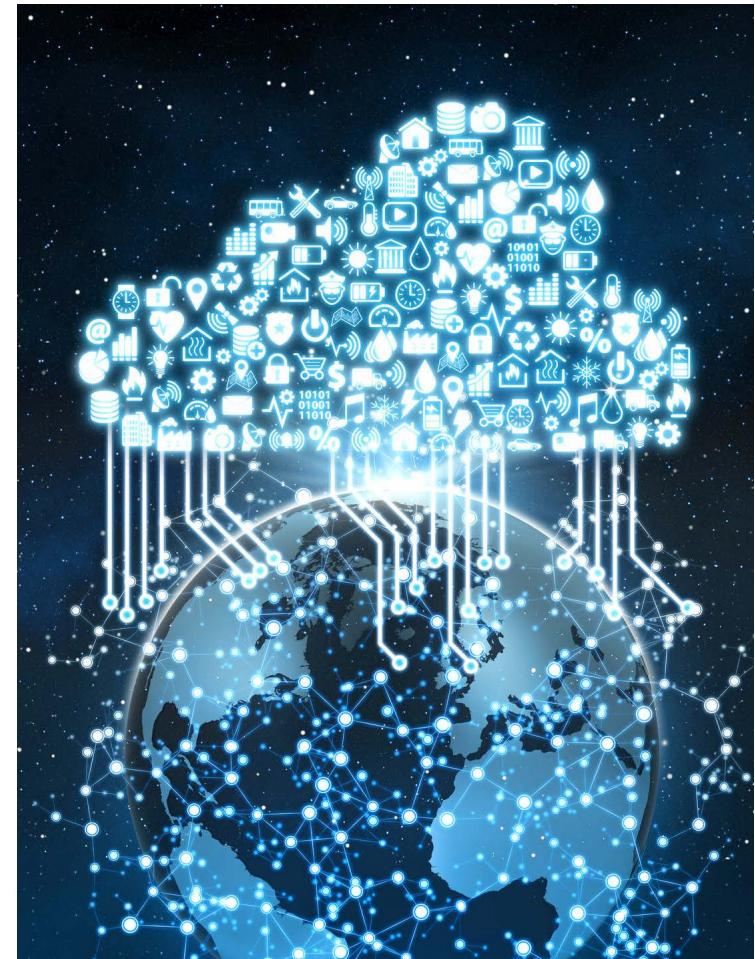
The Coming Data Avalanche — And How we'll Handle it [Rog16]

Potentials and problems of cloud computing

- By 2020, cloud providers will sell more computing power than in-house data center manufacturers — Gartner 2018 [Man18].
- Growth rates of cloud computing of up to 30% worldwide in 2016 lead to a steady concentration of computing resources — IDC [IDC16].
- The energy needs of US data centers grew by approximately 24% between 2010 and 2014 — DoE [DoE16].

An approach to reduce the data centres energy consumption

- Amazon [Ama17a], IBM [IBM15a] and Microsoft [Put+14] - the world's leading data center operators - deploy Field Programmable Gate Arrays (FPGAs) at the application level in various cloud services.
- Reconfigurable hardware for the acceleration of applications is a key technology for many companies — Forbes [Rog16].



[Rog16] Bruce Rogers. „The Coming Data Avalanche – And how we'll handle it“. In: *Forbes Insights*. 2016.

Introduction and motivation

Why we should deploy FPGAs in the Cloud?

Advantages of using FPGAs

- Reduce the **energy consumption** of a data center and thereby reduce operating costs by outsourcing calculations to energy efficient hardware.
- **Accelerate** compute-intensive services with dedicated low-latency, high-bandwidth hardware.
- Increased **security** (encryption, authentication, ...) through processing or anonymization on easier-to-protect special hardware.

Special features and challenges

- Integration of special hardware into a resource management requires corresponding new **administrative structures** and an analysis of the different application possibilities.
- Abstraction of real hardware through **virtualization** to increase flexibility and increase utilization.



Amazon Web Services, Inc. [Ama18]

Structure

Introduction and motivation

Literature review and classification

Requirements analysis and stakeholder

System architecture of the cloud — RC3E

- Requirements
- System architecture

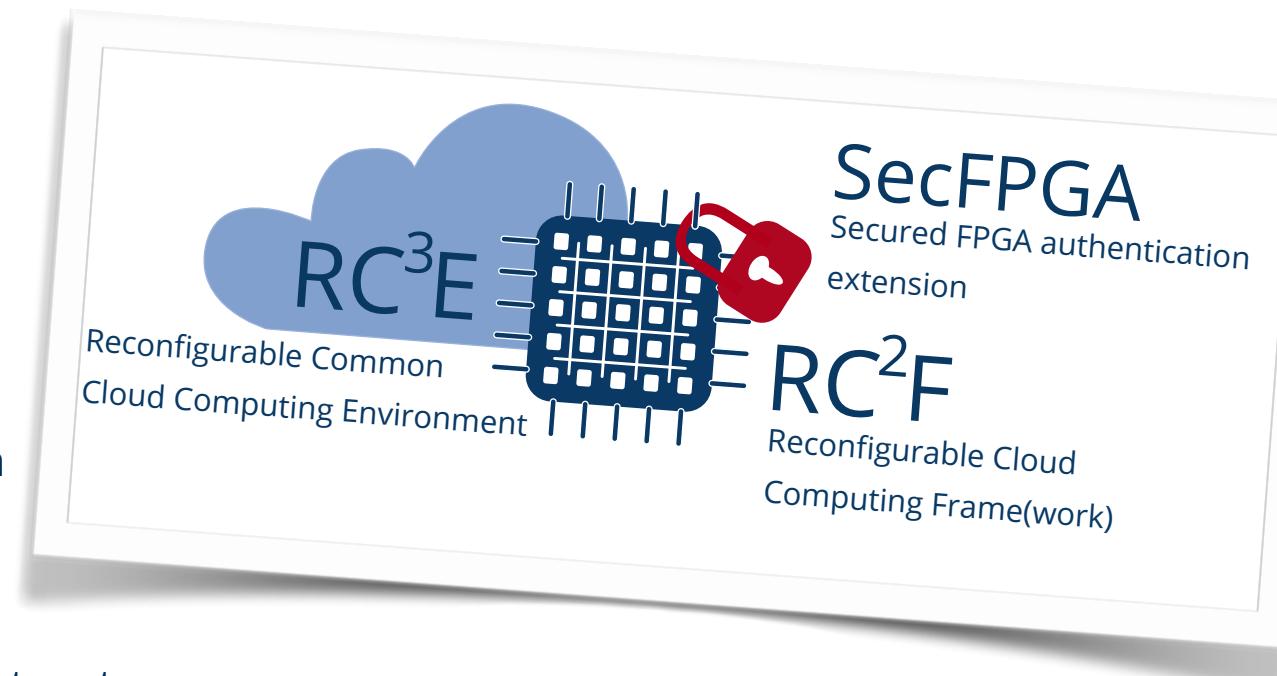
Virtualization of the FPGAs — RC2F

- Infrastructure and virtualization
- Design process and integration into a host-system

Results of the prototypical implementation

- Required FPGA-ressources
- Behaviour simulation of the resource management system

Final considerations



Literature review and classification

Literature review and classification

(a) FPGAs in the context of cloud-computing

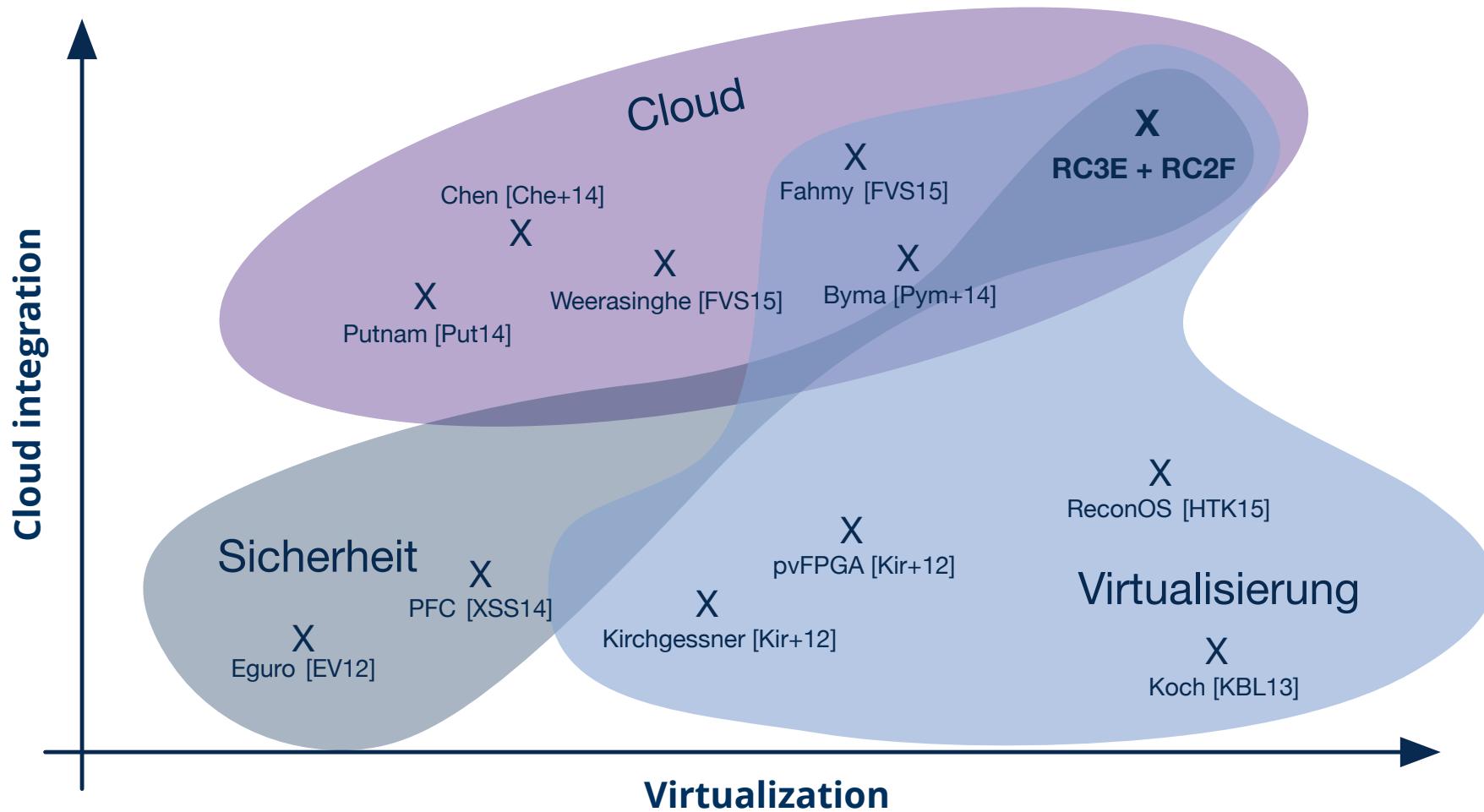
1998	...	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	
												Pogliani [Pog+16]	Geng [GWS+17]	
												Proano [PCC16]	Varela [VW17]	
										Weerasinghe [Wee+15]	Kachris [Kac+16b]	Hong [HKK+17]		
									Grigoras [Gri+14]	Fahmy [FVS15]	Asiatici [Asi+16]	He [HWL17]		
									Byma [Bym+14]	Gazzano [Don+15]	Chow [Cho16]	Tarafdar [TEL+17]		
									Chen [Che+14]	IBM [IBM15]	Knodel [KLS16]	Orellana [Ore17]		
						Madhavapeddy [MS11]	Yin [Y+12]	Knodel [KS13]	Knodel [Kno14]	Ghasemi [Gha15]	Orellana [OCC16]	Zha [ZL17]		
					Shan [Sha+10]	Mondol [Mon11]	Eguro [EV12]	Kochberger [Koc+13]	Putnam [Put+14]	Ovtcharov [Ovt+15]	Kachris [Kac+16a]	Jadhav [JGA+17]		
							Lim [Lim+13]	Xu [XSS14]	Pöppelmann [Pöp+15]	Gao [GS16]	Proano [PCC17]			

Literature review and classification

(b) virtualization of FPGAs

1998	...	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
										Byma [Bym+14]	Weerasinghe [Wee+15]	Kidane [KB16]	Sindhu [SAF17]
										Chen [Che+14]	Gazzano [Don+15]	Chow [Cho16]	Tarafdar [TEL+17]
								Zuma [BL12]	Koch [KBL13]	Nguyen [NK14]	Fahmy [FVS15]	Asiatici [Asi+16]	Zhao [TZ17]
				So [SB08]			Yu [Yu+11]	Gonzalez [Gon+12]	Cheng [Che+13]	Agne [Agn+14]	Knodel [KS15]	Knodel [KLS16]	Chen [CMN17]
Fornaciari [FP98a]		Peck [Pec+06]		EI-Araby [EG08]			Figuli [Fig+11]	Kirchgessner [Kir+12]	Wang [WBP13]	Eckert [Eck14]	Happe [HTK15]	Knodel [KGS16]	Knodel [KGS17]

Literature review and classification



CLOUD

Alibaba gets Xilinx FPGA for its F3 cloud

BY PARAS NEHRAMIC ON 11 MAY 2018

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<https://fudzilla.com/news/memory-and-storage/46283-alibaba-gets-xilinx-fpga-for-its-f3-cloud>

WIRED

CADE METZ BUSINESS 09.26.16 07:00 PM

MICROSOFT BETS ITS FUTURE ON A REPROGRAMMABLE COMPUTER CHIP

<https://www.wired.com/2016/09/microsoft-bets-future-chip-reprogram-fly/>

Facebook has a new job posting calling for chip designers

Matthew Lynley @matthewlynley Apr 19, 2018

<https://techcrunch.com/2018/04/18/facebook-has-a-new-job-posting-calling-for-chip-designers/>

Microsoft takes step towards delivering FPGAs as a service

2018
Launches preview of FPGA-powered Project Brainwave

<https://www.computerworld.com.au/article/640970/microsoft-takes-step-towards-delivering-fpgas>



Amazon And Xilinx Deliver New FPGA Solutions

SEP 27, 2017 6:08:48 AM 8,423 0

Forbes

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<https://www.forbes.com/sites/moorinsights/2017/09/27/amazon-and-xilinx-deliver-new-fpga-solutions/#3f880862370a>

FPGAs and the New Era of Cloud-based ‘Hardware Microservices’

8 Jun 2017 6:00am, by Mary Branscombe

<https://thenewstack.io/developers-fpgas-cloud/>

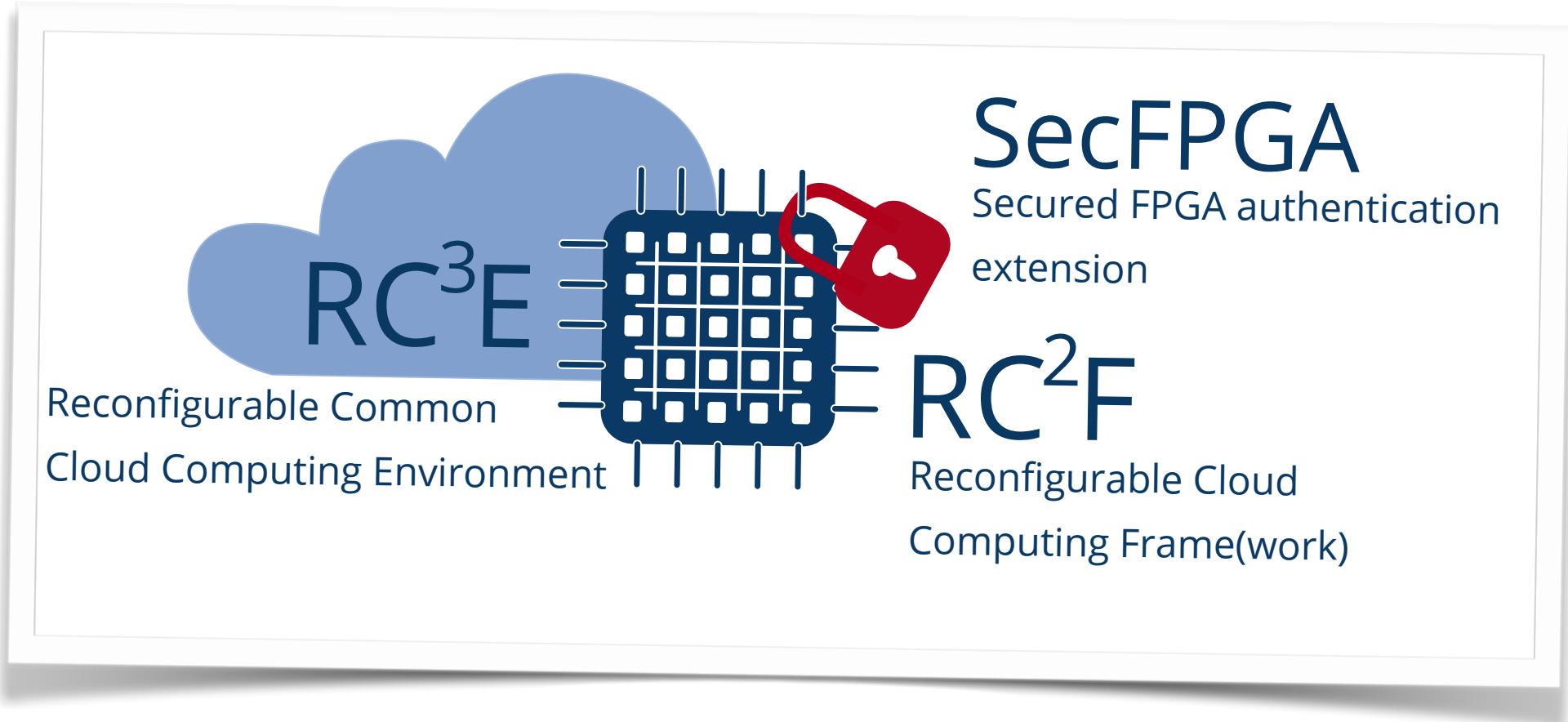
I. Requirements and stakeholder analysis

II. System architecture of the cloud — RC3E

III. Virtualization of the FPGAs — RC2F

Requirements and stakeholder analysis

Overall system partitioning and architecture — RC3E + RC2F (+SecFPGA)



Requirements and stakeholder analysis

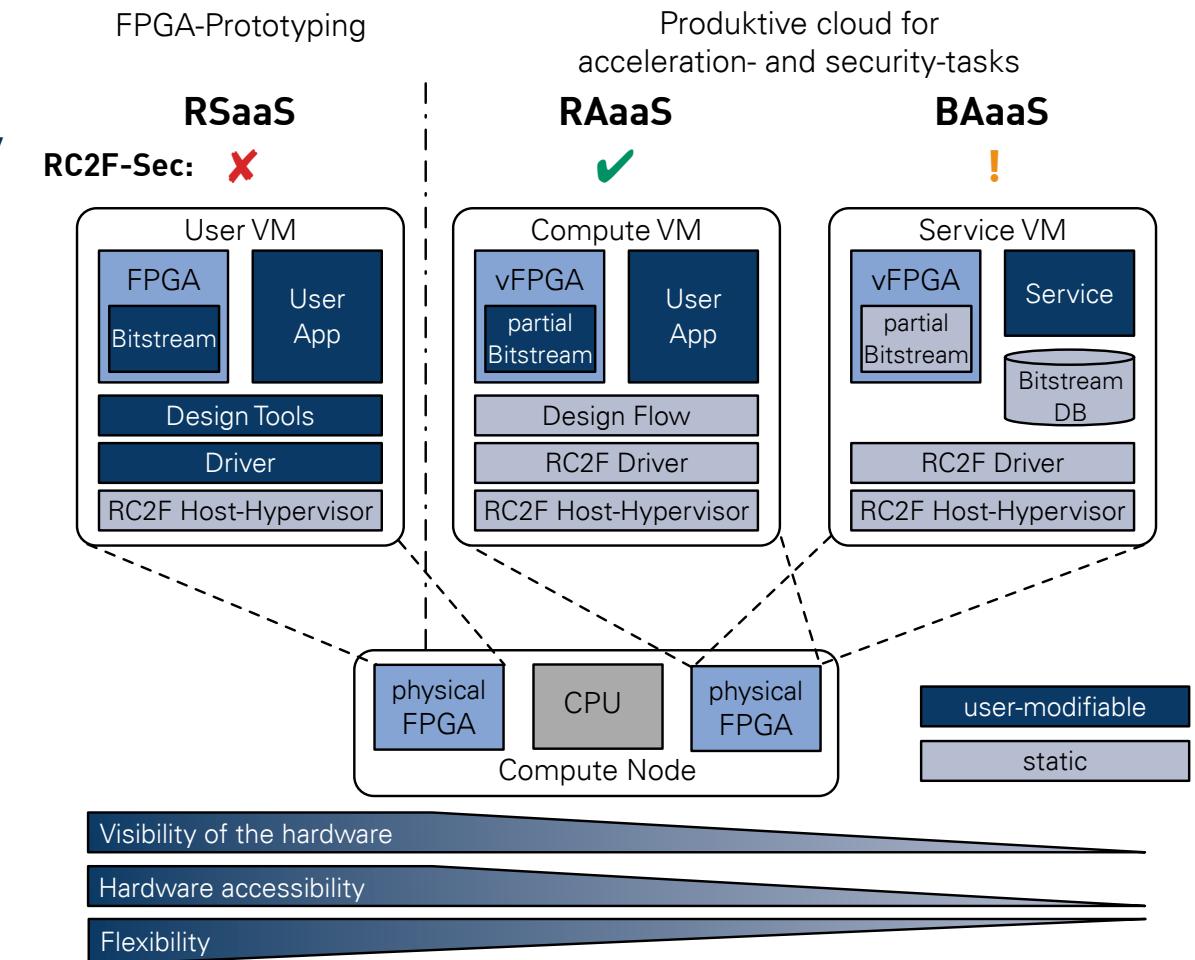
Provision, security and service models

Approach

- The user groups require a different level of visibility and virtualization.
- With division into service models, this abstraction can be integrated into resource management.

Service-Models

- I. Reconfigurable Silicon as a Service (RSaaS).
- II. Reconfigurable Accelerator as a Service (RAaaS).
- III. Background Acceleration as a Service (BAaaS).

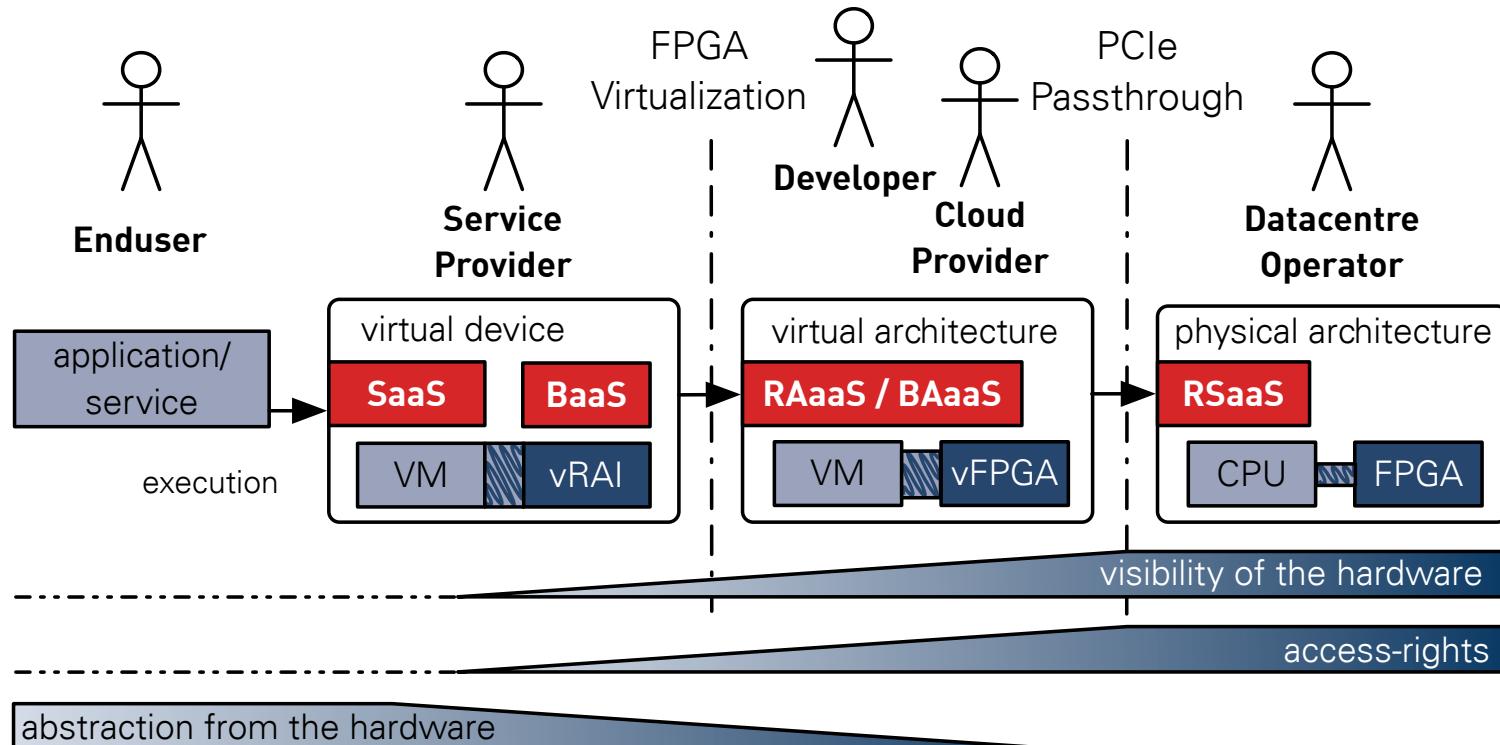


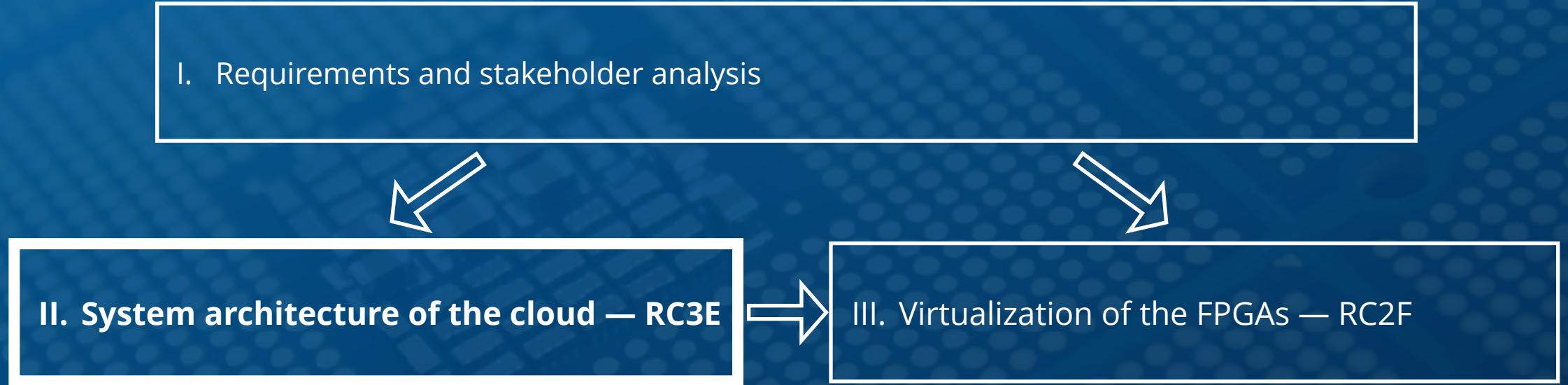
Requirements and stakeholder analysis

The role of users in the context of FPGAs in the cloud

Objectives

- Flexible deployment for different **groups of people** with different needs.
- The FPGA is **not visible** to the enduser and only *virtual* resources are used by the service providers.





II. System architecture of the cloud — RC3E

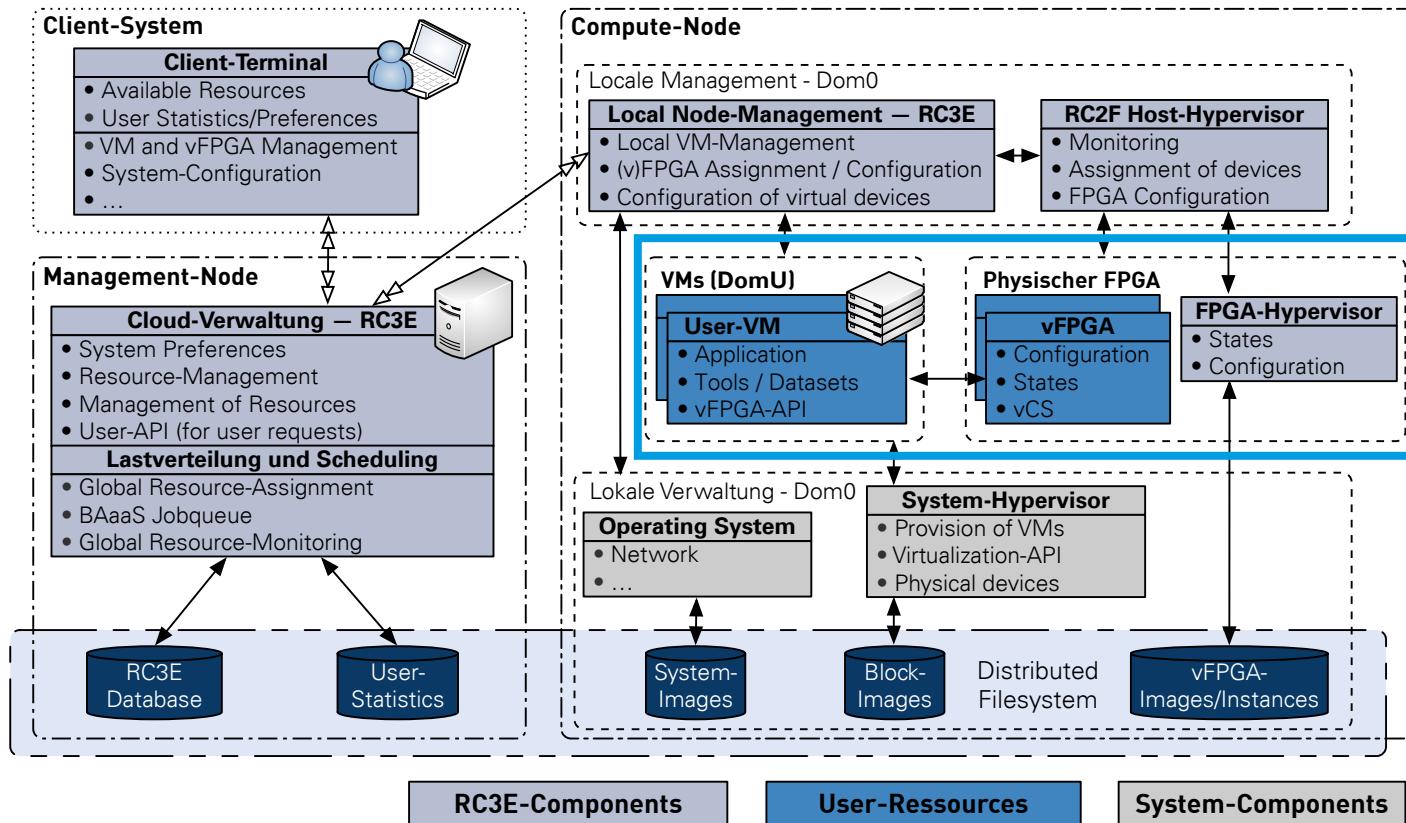
Architecture of the RC3E prototype

View of the hardware architecture

- The cloud consists of nodes with one CPU each and (two) PCIe-coupled FPGAs.
- Each physical FPGA can contain multiple virtual FPGAs.

Extension of the software architecture

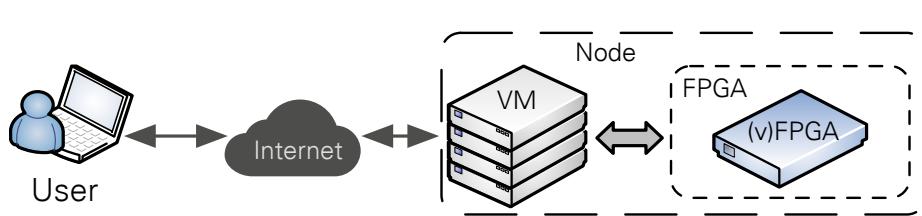
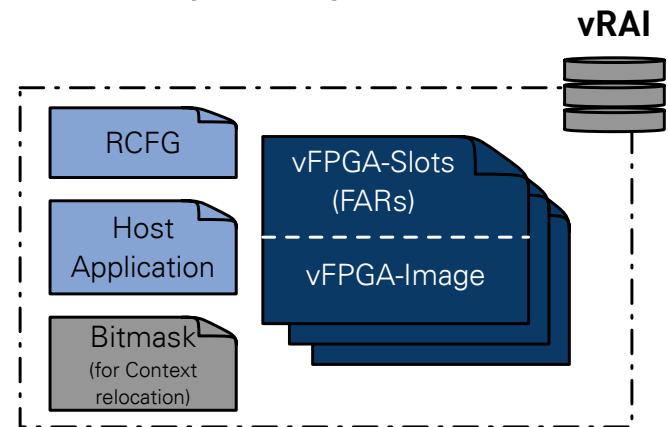
- Manage resources (vFPGA and VMs) across all cloud nodes according to service models.
- Required components:
 - local node-management
 - RC2F host-hypervisor
 - FPGA-hypervisor (located on the FPGA)



II. System architecture of the cloud — RC3E

Encapsulation in packages (vRAIs) and description of virtual resources (RCFG)

- All necessary files for a background accelerator are encapsulated in virtual Reconfigurable Acceleration Images (vRAIs).
- The vFPGA itself is described in the form of a **Reconfigurable (Device) Configuration (RCFG)**.
- A simple VM with hardware accelerator can be easily described:



```
service = 'ba'  
name = ['vfpga-kmeans']  
vm = ['vm1-pvm']  
  
vfpga = [1]  
size = [4]  
memory = [4000]  
  
boot= ['idle']  
design = ['kmeans-quad.vrai']
```

#Service Model BAaaS
#vFPGA/User Design Name
#VM-Instance Name

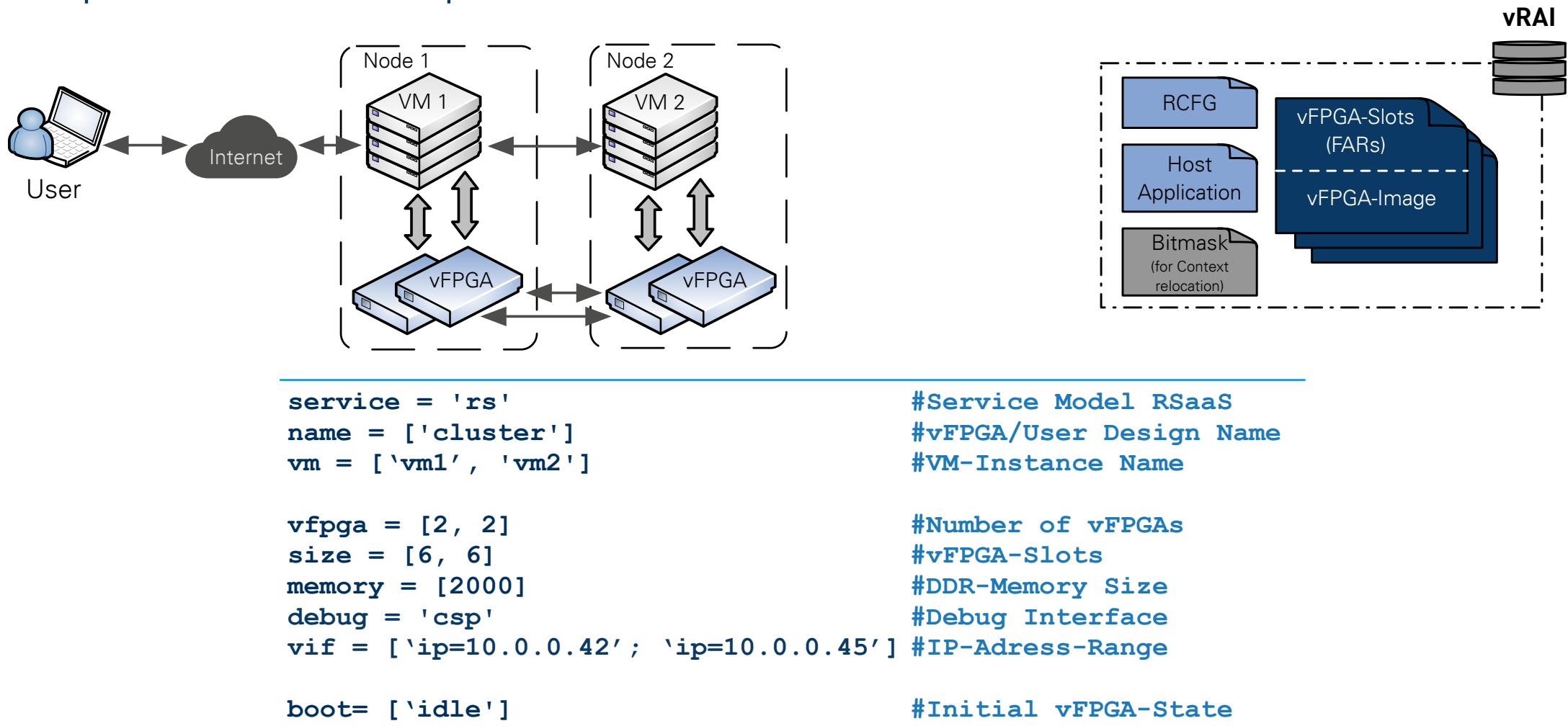
#Number of vFPGAs
#vFPGA-Slots
#DDR-Memory Size

#Initial vFPGA-State
#Initial Design

Example of a RCFG for a vFPGA in model BAaaS.

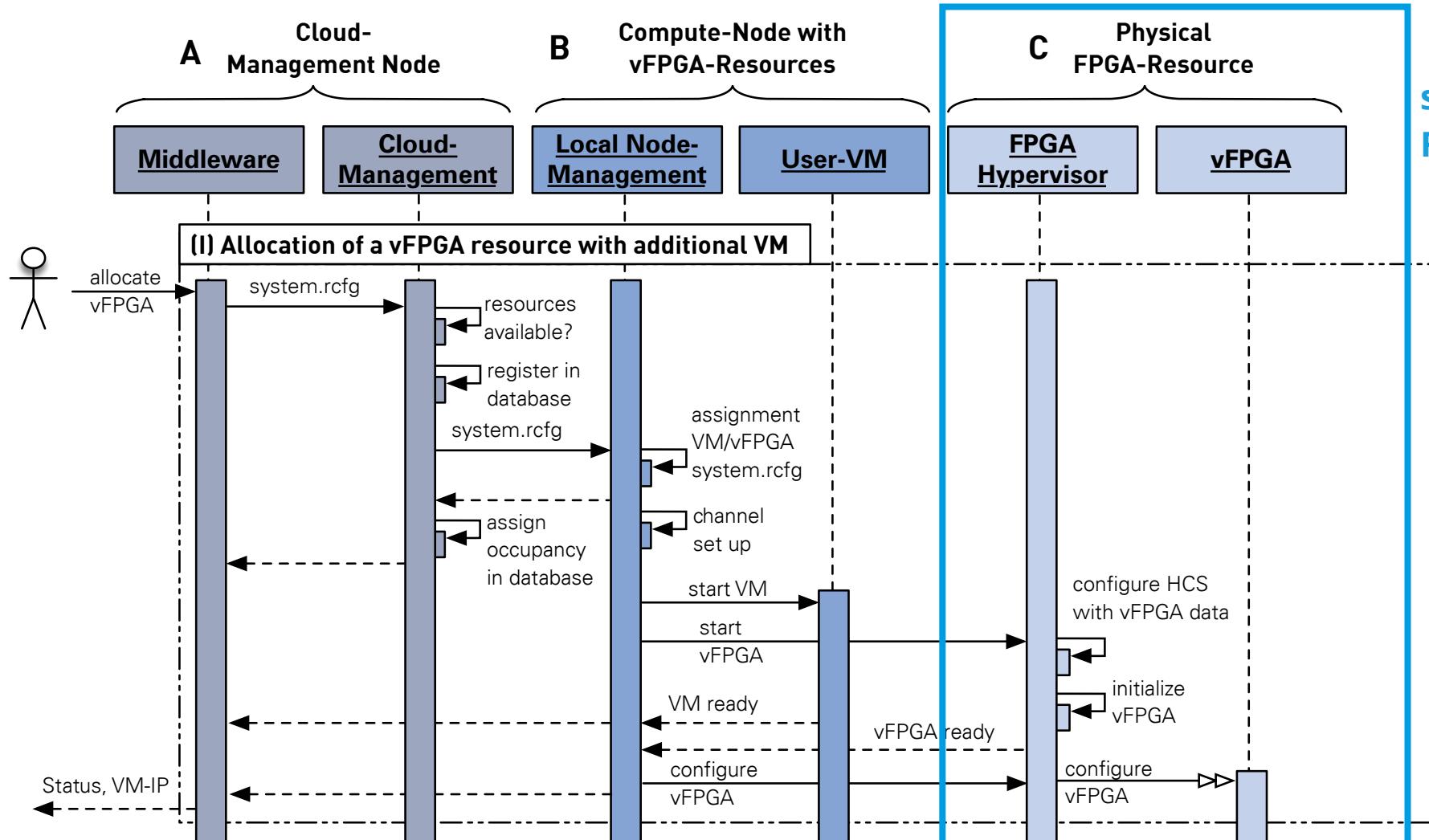
II. System architecture of the cloud — RC3E

Description of a more complex virtual resource in a RCFG

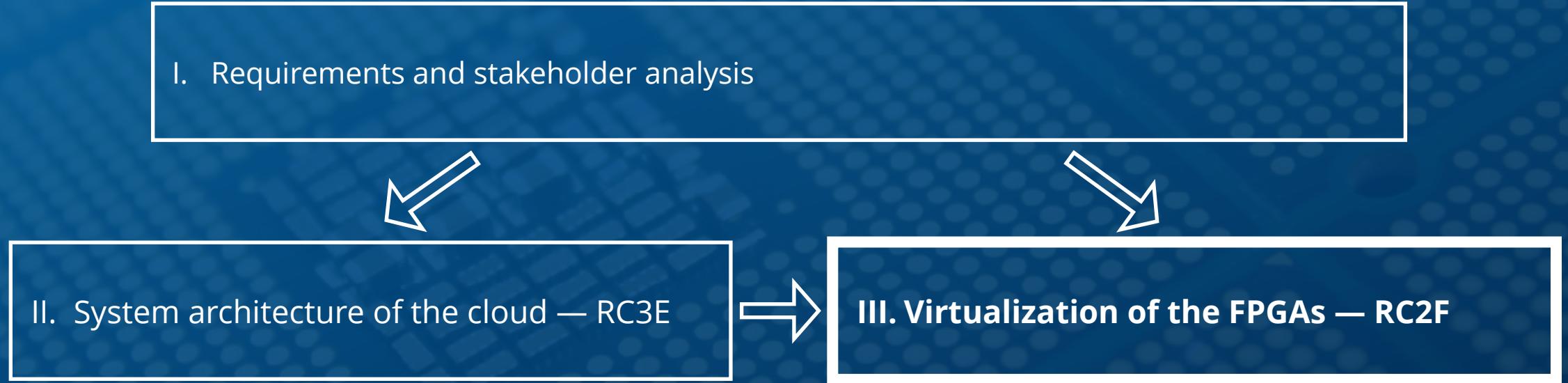


II. System architecture of the cloud — RC3E

Interactions across the individual components within the RC3E



starting point for
RC2F virtualization



III. Virtualization of the FPGAs — RC2F

Transfer of the classic virtualization to the reconfigurable hardware

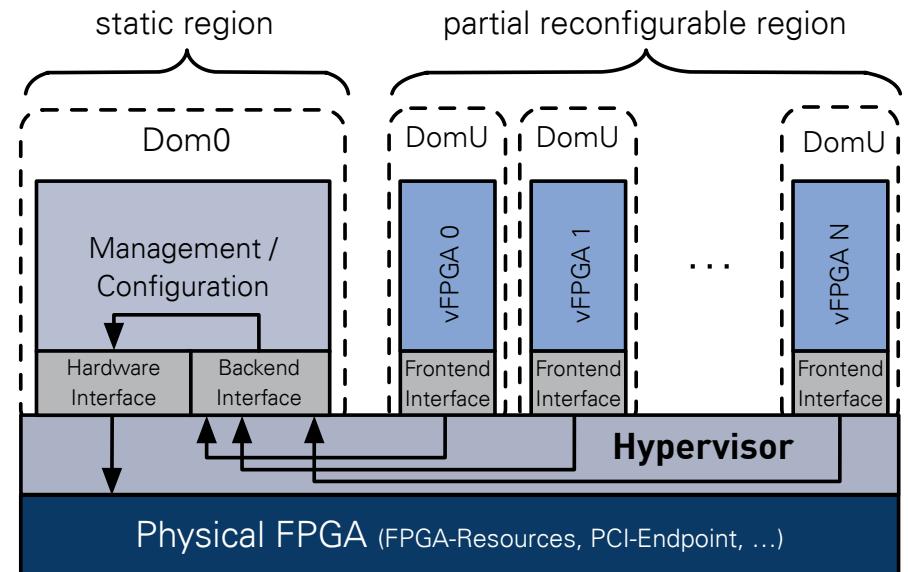
Concept for the virtualization of FPGAs (approach based on classical System-VMs):

- The user core is located directly (bare-metal) on the FPGA-resources within a dynamically reconfigurable region, the virtual FPGA (vFPGA).
- The static part of the FPGA contains management structures and the physical interfaces.
- The concept is equivalent to traditional virtual machines:

Native Typ 1 System-/Bare-Metal-Virtualization with same ISA

Interface-Virtualization:

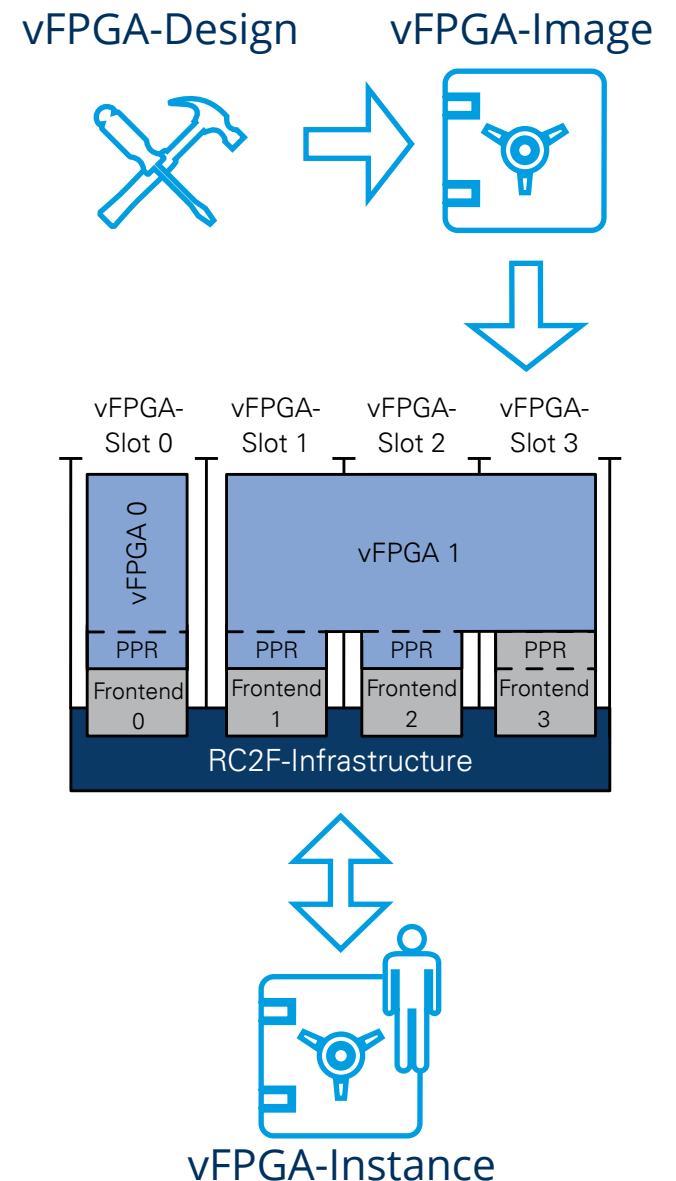
- External devices are accessed through **paravirtualization** within the FPGA hypervisor (VMM).
- The interfaces of the vFPGAs are the **frontends**, which are connected to the **backend** in the static region.



III. Virtualization of the FPGAs — RC2F

Definitions and terms

- A **vFPGA** is perceived by the user as a stand-alone resource with a dynamic number of hardware resources (slices, LUTs, registers, etc.).
- A vFPGA is mapped to **vFPGA-Slots** — smallest possible physical regions with a fixed number of hardware resources.
- A **vFPGA-Design** is the hardware design within a vFPGA.
- A partial Bitstream is called **vFPGA-Image** and
- if this is assigned to a user this becomes a **vFPGA-Instance**.



Distinctions in the term “Hypervisor”:

- The management structure for the vFPGAs on their host system is called the **RC2F Host-Hypervisor**.
- The **FPGA-Hypervisor** is the management structure on the FPGA (Dom0).

III. Virtualization of the FPGAs — RC2F

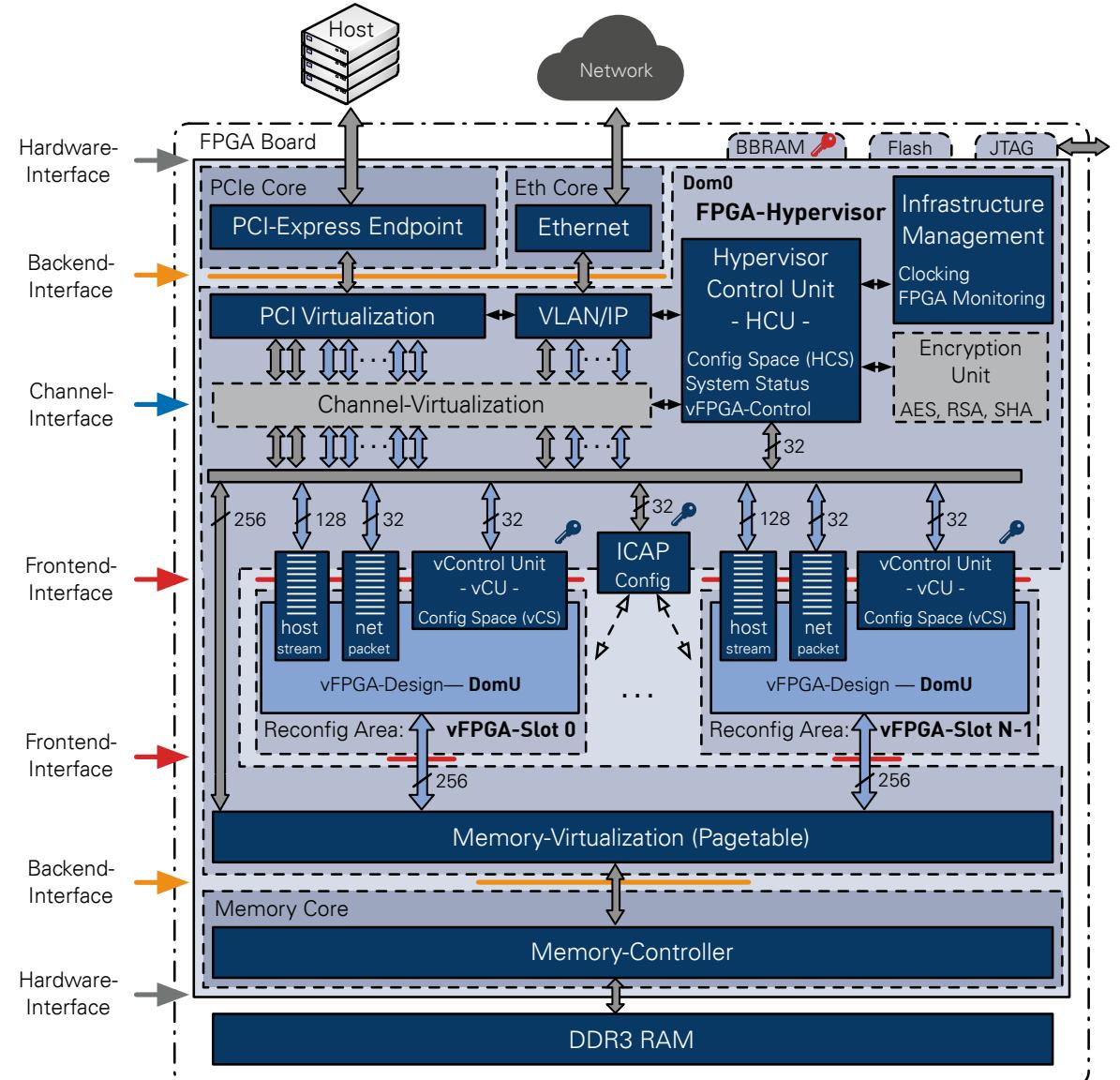
Architecture for deploying virtualized FPGAs

Provision of vFPGAs on the physical FPGA-device:

- Multiple vFPGAs within vFPGA slots.
- The ICAP is used for dynamic partial reconfiguration.
- Direct management of the states of the vFPGAs on the FPGA within the vControl Unit (**vCU**).

Components of the infrastructure (FPGA-Hypervisor):

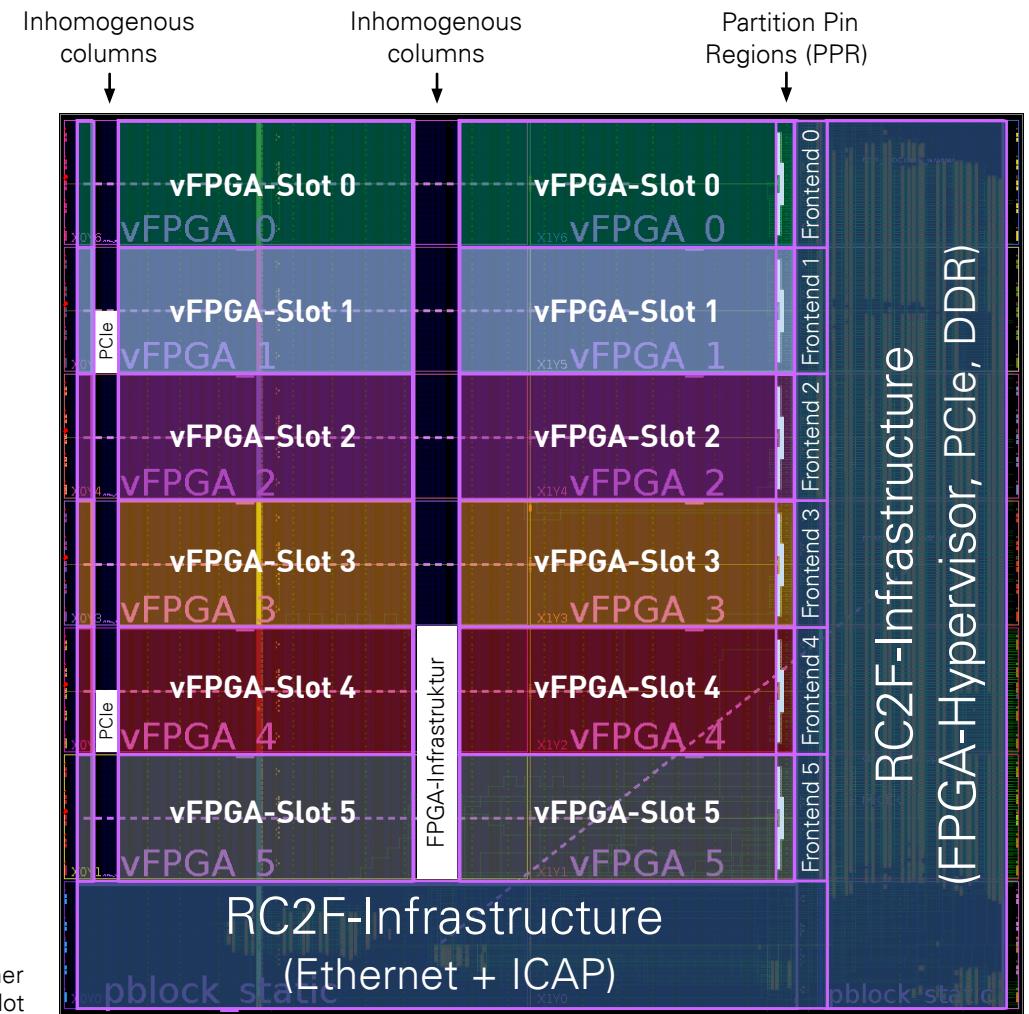
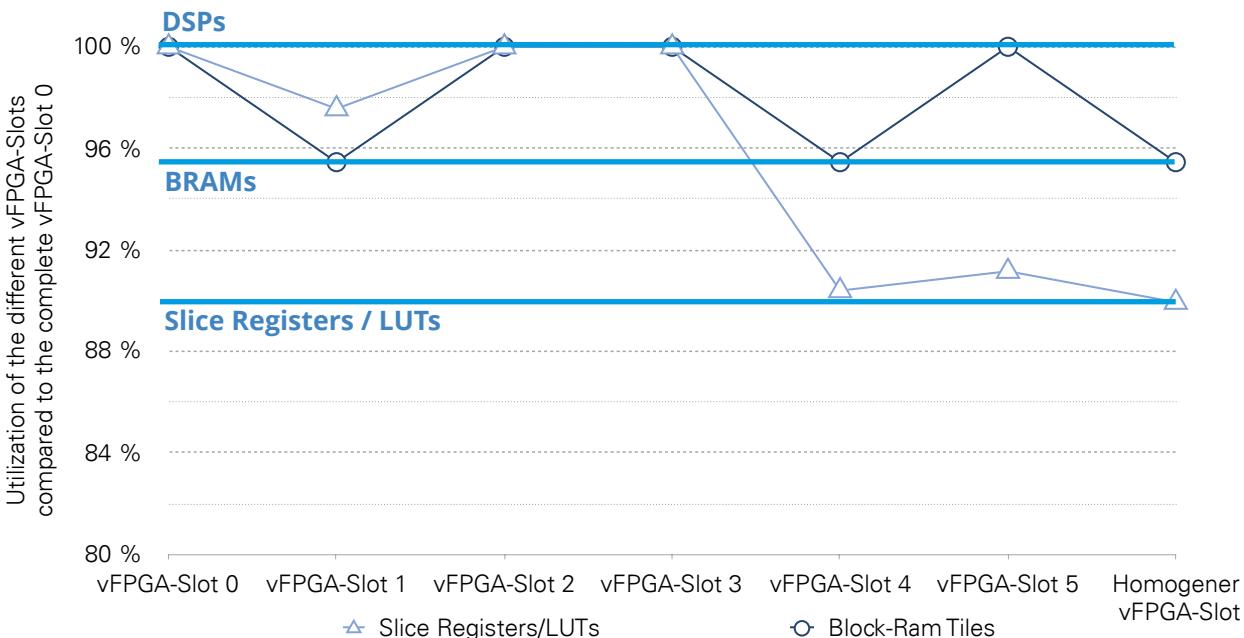
- Internal system bus used for the Paravirtualization.
- Hypervisor Control Unit (**HCU**) to monitor the physical FPGA infrastructure.
- **PCIe** and **Ethernet**-Interfaces.
- Access to **DDR3 memory** on the FPGA board via page tables.



III. Virtualization of the FPGAs — RC2F

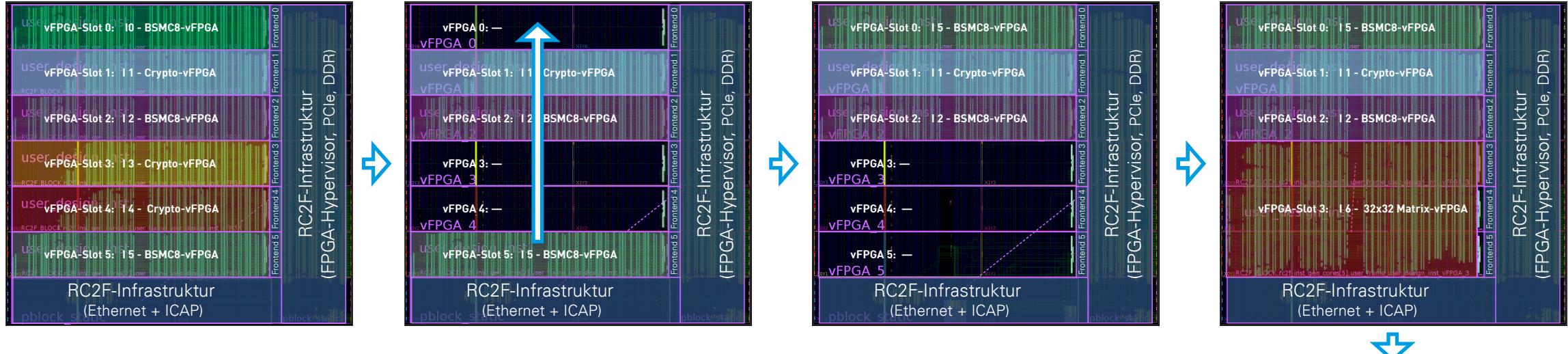
Mapping of the RC2F on homogeneous vFPGA slots (Xilinx Virtex-7 XC7VX485T)

- Establishment of vFPGA slots within the clock regions.
- Realization of **homogeneous** vFPGA slots on the physical FPGA to enable **migration** of the vFPGA-Instances.
- The distribution is dictated by the inhomogeneous FPGA architecture.



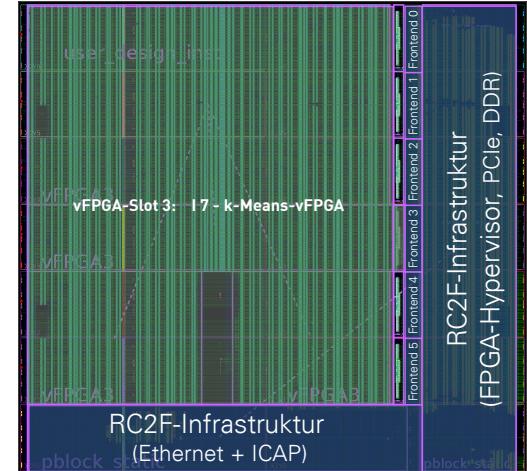
III. Virtualization of the FPGAs — RC2F

Application scenario for using migration within RC2F virtualization



Example assignment within a simple scenario

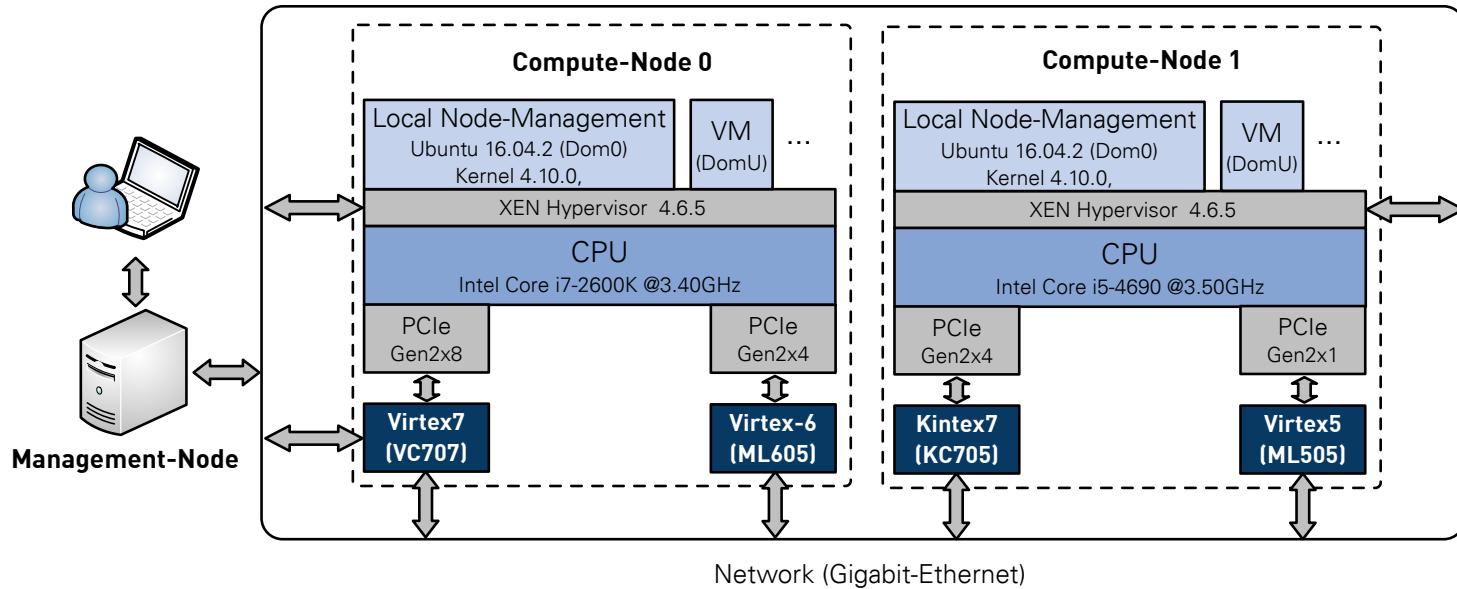
- Full utilization of the physical FPGA by six single vFPGA-Instances.
- Release of individual instances by users.
- **Migration** to provide a larger contiguous area.
- Placement of a larger vFPGA-Instance (Triple).
- Provision of the entire FPGA for a maximum size (hexa) vFPGA-Instance.



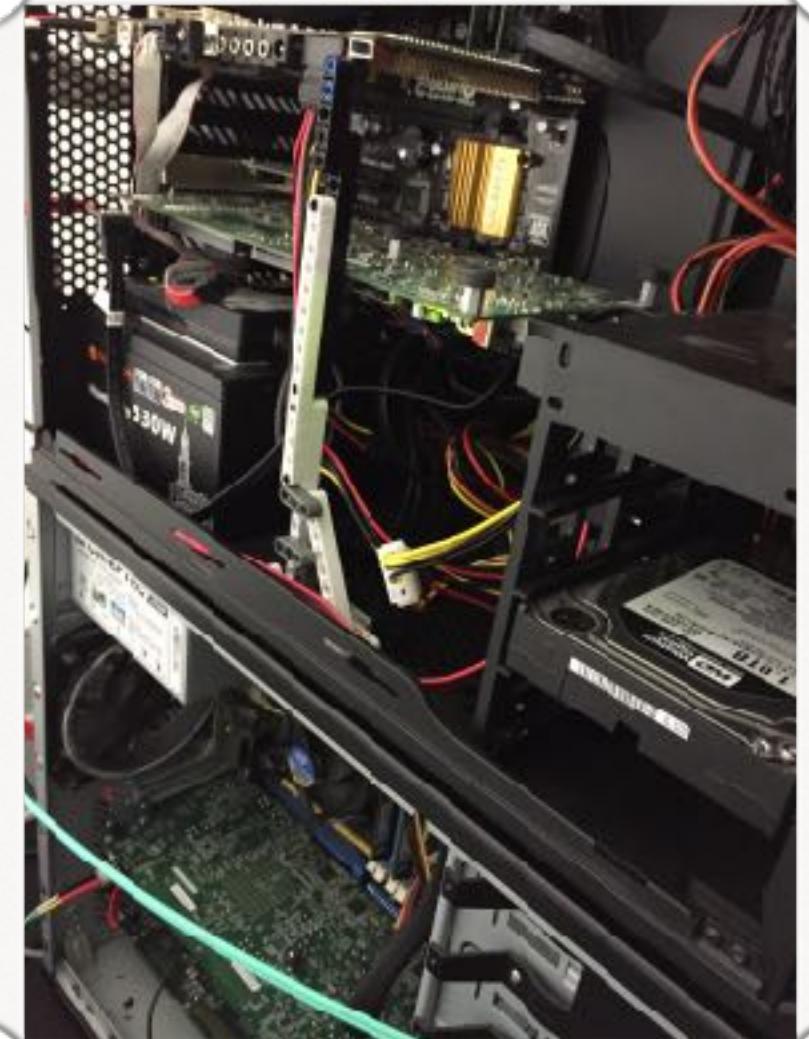
Results of the prototypical implementation of the RC3E & RC2F

Results of the prototypical implementation of the RC3E & RC2F

Hardware construction of the cloud prototype

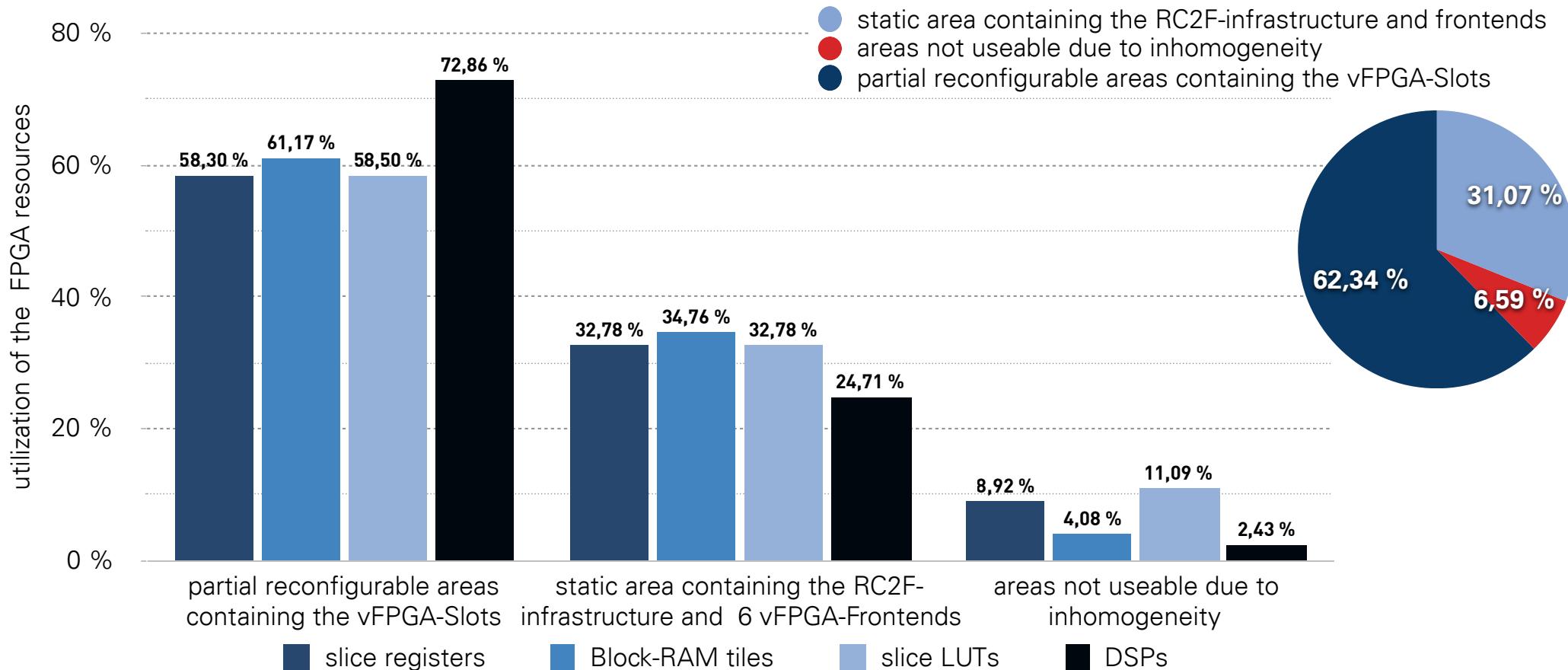


- Structure of the cloud prototype includes different FPGAs.
- Used as a system for development (RSaaS) and teaching (RAaaS).
- For the evaluation of a larger system (BAaaS) a RC3E-Simulation was realized.



Results of the prototypical implementation of the RC3E & RC2F

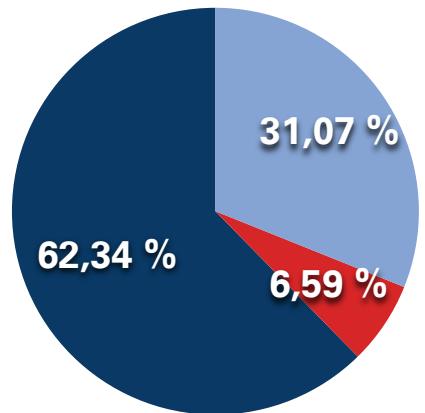
Utilization of the areas of the RC2F prototype on a Virtex-7 (XC7VX485T)



Results of the prototypical implementation of the RC3E & RC2F

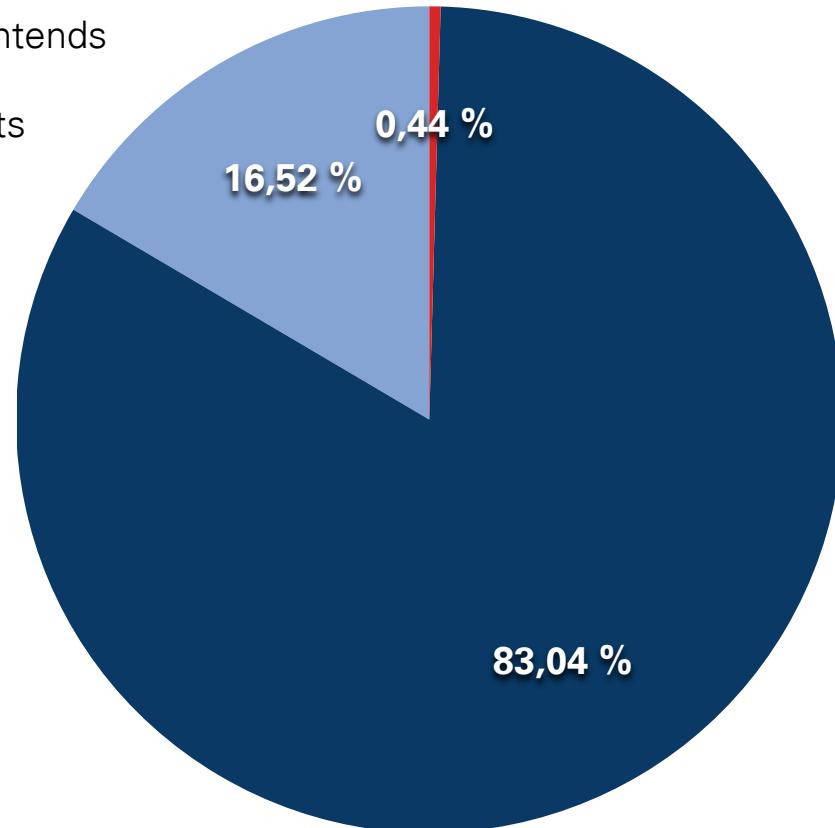
Transfer of the RC2F to a Virtex-7 UltraScale+ FPGA

- static area containing the RC2F-infrastructure and frontends
- areas not useable due to inhomogeneity
- partial reconfigurable areas containing the vFPGA-Slots



RC2F-Prototype
Virtex-7 XC7VX485T

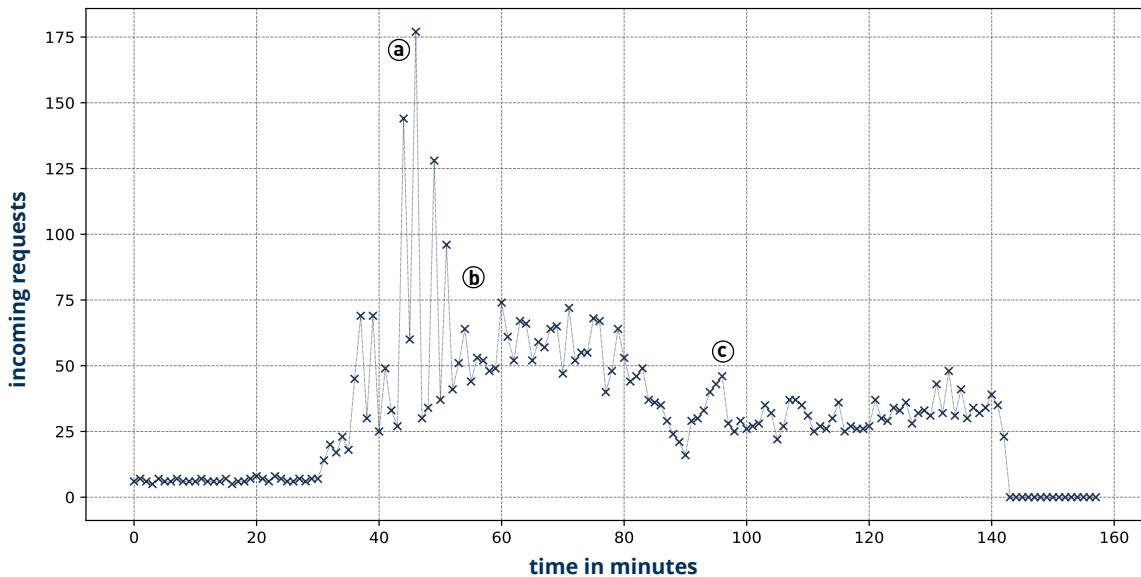
$\times 4,55$



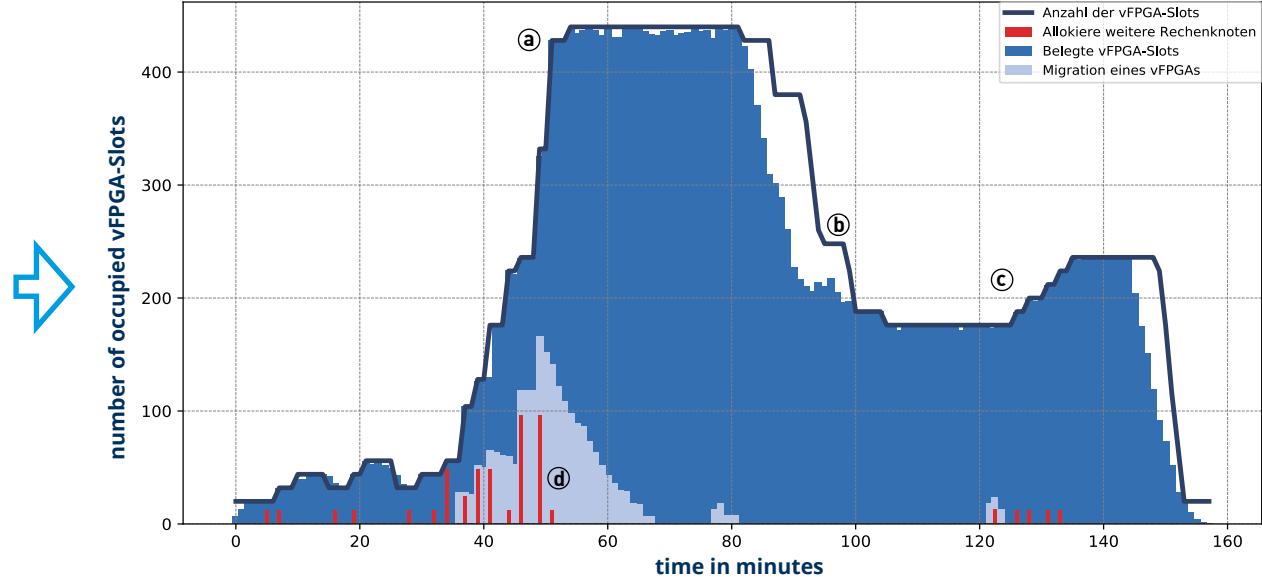
estimation for a productive cloud
Virtex-7 UltraScale+ XCVU9P

Results of the prototypical implementation of the RC3E & RC2F

Results of the RC3E simulation with a synthetic workload



Synthetic workload with 4,981 requests over 150 minutes.



Assignment of vFPGA-Slots in an simulation with additional migration to reduce defragmentation (+FPGAs +RC2F +migration).

Results of the prototypical implementation of the RC3E & RC2F

Simulation of the RC3E management system in a cloud (BAaaS)

	Scenario I (synthetic) — 4,981 requests			
	Basis (without FPGAs)	+FPGAs	+RC2F	+Migration
Compute Nodes	357	132	26	24
Utilization of the FPGAs	—	27.34 %	78.14 %	85.07 %
Energy demand (kWh)	35.37 kWh	24.53 kWh	8.64 kWh	8.13 kWh
Energy demand (%)	100 %	69.35 %	24.43 %	22.91 %

- By using two Virtex-7 FPGAs per node, the energy demand of the cloud can be reduced by **30.65 %**.
- RC2F virtualization reduces the energy demand of the cloud system to **24.43 %**.
- An additional migration of vFPGAs adds an extra **1.45 %** compared to a simple RC2F virtualization.

Final considerations, summary and outlook

Final considerations

Comparison with other works

	Host VM	Migration (vFPGAs)	Homogenous vFPGAs	Multiple User	Scalability	
					FPGA	Cluster
Kachris et al. [Kac+16b]	✓	✗	✗	✗	✗	✗
Byma et al. [Bym+14]	✗	!	✗	✓	!	✗
Fahmy et al. [FVS15]	✗	✗	✗	✓	!	✗
Gazzone et al. [Don+15]	✗	✗	✗	✓	✗	✓
Weerasinghe [Wee+15]	!	✗	✗	✓	✗	✗
Iordache et al. [Ior+16]	✓	!	✗	✗	✗	✓
Chen et al. [Che+14]	✓	!	✗	✓	✓	✗
RC3E + RC2F	✓	✓	✓	✓	✓	!

✓ realized

! limited

✗ not realized

Final considerations

Summary

I. Requirements and stakeholder analysis

- Investigation of a flexible deployment and the basic use of **virtualized FPGAs** in a Cloud.
- Analysis of possibilities use-cases of FPGAs in a cloud environment with different **service models**.
- Investigation of involved groups of people (**stakeholder**) within an FPGA cloud.



II. System architecture of the cloud — RC3E

- Embedding vFPGAs in a cloud management (**RC3E**) with the ability to migrate VM and vFPGA instances.
- Build a **configuration (.rcfg)** describing a vFPGA resource and different system configurations.
- Development of a two-stage scheduling with **migration** to increase the utilization.

III. Virtualization of the FPGAs — RC2F

- Approach to virtualization of FPGAs (**RC2F**) analogous to system virtualization.
- Concept to adapt the size of the **homogeneous** vFPGAs to the resources of the user designs.
- Realization of the **migration** of an FPGA instance.

Final considerations

Outlook: Aspects for Future FPGA Architectures

I. SoC-FPGA with a static RC2F-like Infrastructure:

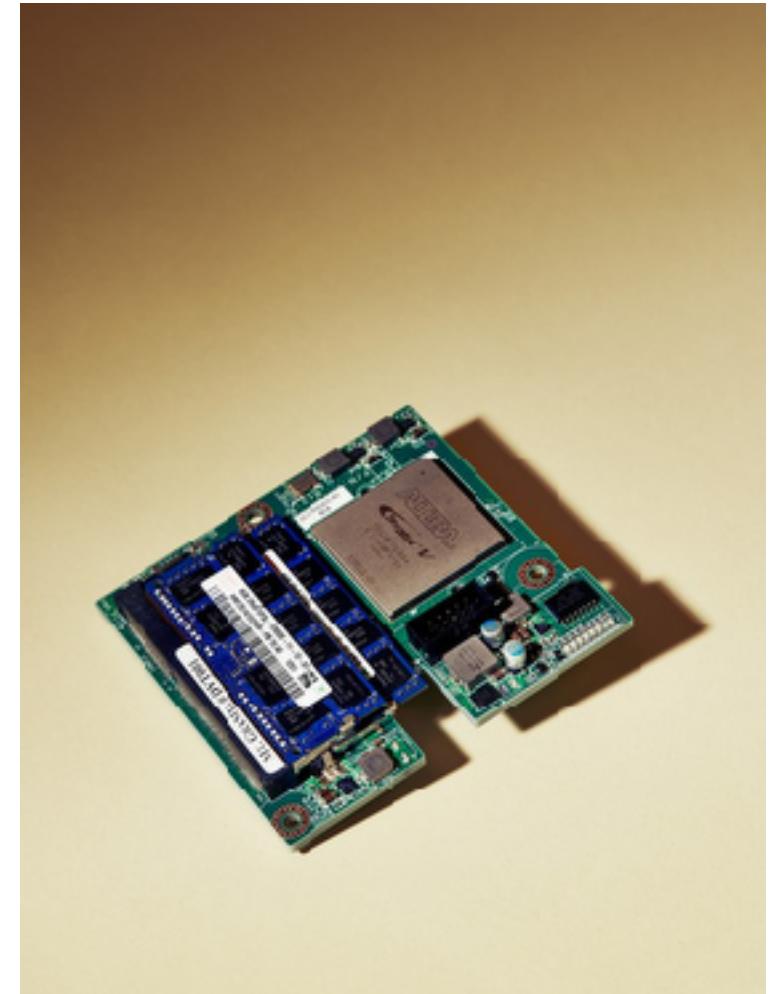
Development of a static area for the administration with all necessary interfaces to the outside world.

II. Structural changes within the FPGA architecture:

Establishment of homogeneous and areas with own clock regions on the FPGAs.

III. Implementation of a security concept:

Security concept based on a trusted authority to provide verifiable RC2F infrastructure.



<https://www.wired.com/2016/09/microsoft-bets-future-chip-reprogram-fly/>



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