Solution of Digital Logic Theory Assignment 4

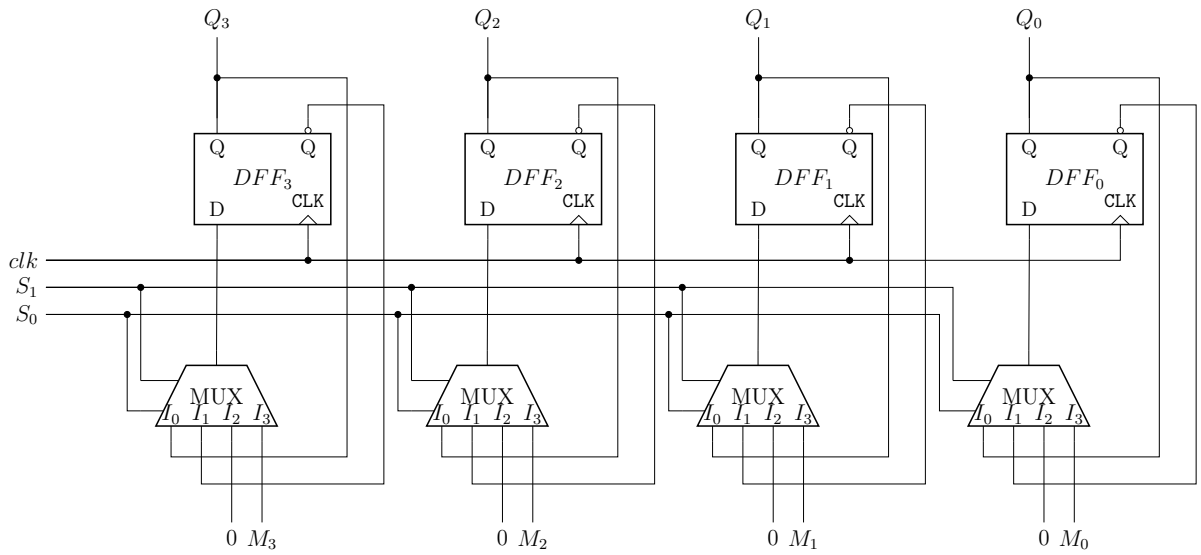
Edited from the submission of an anonymous brilliant student

1.

Function Table:

S_1	S_0	D_3	D_2	D_1	D_0	Operation
0	0	Q_3	Q_2	Q_1	Q_0	No Change
0	1	Q_3'	Q_2'	Q_1'	Q_0'	Complement the four outputs
1	0	0	0	0	0	Clear register to 0
1	1	M_3	M_2	M_1	M_0	Load parallel data

Logic Diagram:
Assume data are passed as M_3, M_2, M_1 and M_0, where M_3 is MSB.



2.

Because there are 7 possible states, and $7 \leq 2^n - 1$ with $n = 3$, we start with 3 flip-flops.

Z	Q_2	Q_1	Q_0
0	1	0	1
1	0	1	0
1	1	0	1
1	1	1	0
1	1	1	1
0	1	1	1
1	0	1	1

However, there are identical states with different outputs. We can add another flip-flop to make the circuit work.

Z	Q_3	Q_2	Q_1	Q_0
0	1	0	1	1
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0
0	1	1	1	1
1	0	1	1	1

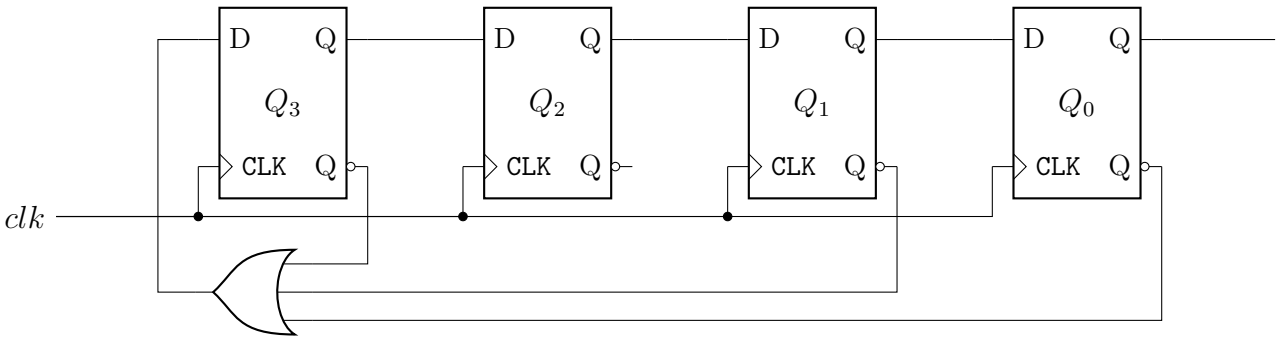
Now there are no identical states with different outputs.
Karnaugh Maps:

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	X	1	1	X
11	X	1	0	1
10	X	X	0	1

Simplified Boolean Expression:

$$Z = Q_0' + Q_1' + Q_3'$$

Logic Diagram:

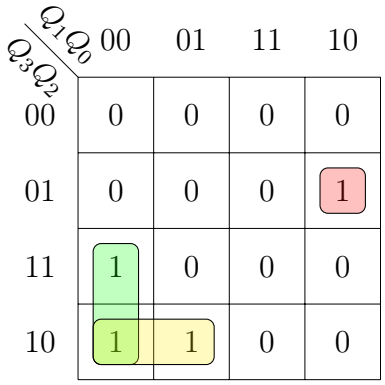


3.

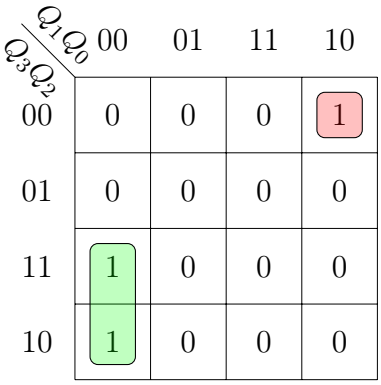
State Table:

Current State				Next State			
Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	0
1	0	0	1	1	0	0	0
1	0	1	0	0	0	1	0
1	0	1	1	0	0	1	0
1	1	0	0	1	1	0	1
1	1	0	1	0	0	1	0
1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0

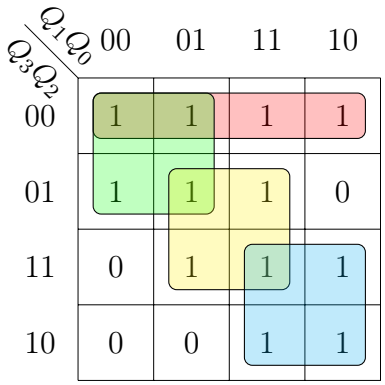
Karnaugh Maps:



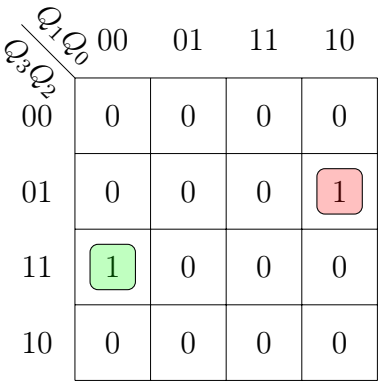
D_3



D_2



D_1

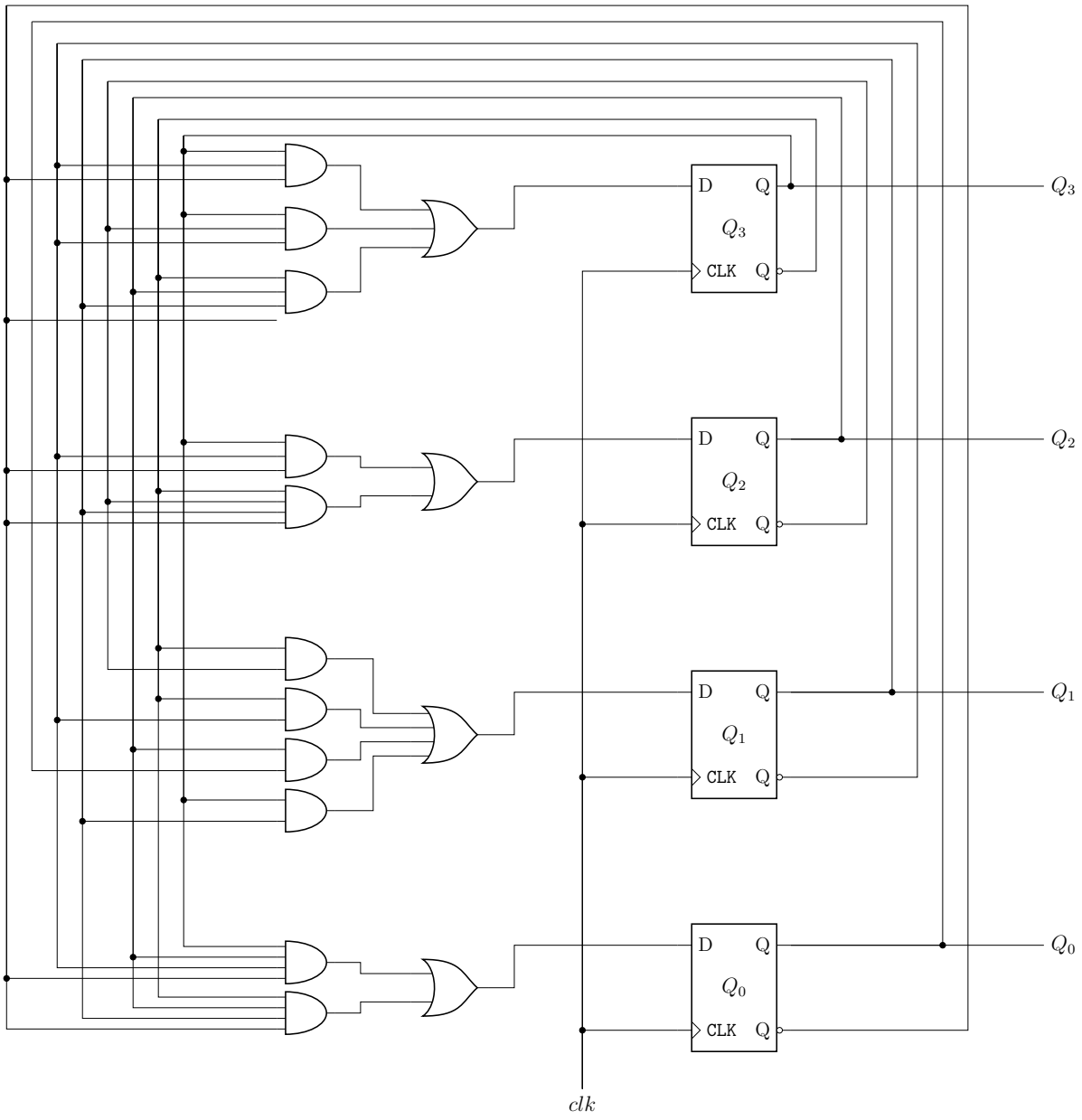


D_0

Simplified Boolean Expression:

$$
\begin{aligned}
D_3 =& Q_3Q_1'Q_0' + Q_3Q_2'Q_1' + Q_3'Q_2Q_1Q_0' \\
D_2 =& Q_3Q_1'Q_0' + Q_3'Q_2'Q_1Q_0' \\
D_1 =& Q_3'Q_2' + Q_3'Q_1' + Q_2Q_0 + Q_3Q_1 \\
D_0 =& Q_3Q_2Q_1'Q_0' + Q_3'Q_2Q_1Q_0'
\end{aligned}
$$

Logic Diagram:



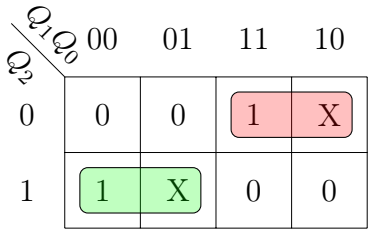
4.

With Don't Cares

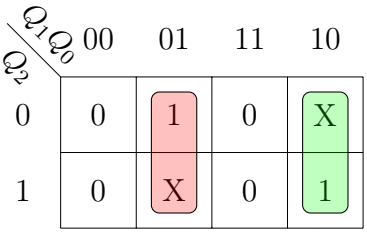
State Table with TFF Inputs:

Current State			Next State			TFF Inputs		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	x	x	x	x	x	x
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	x	x	x	x	x	x
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

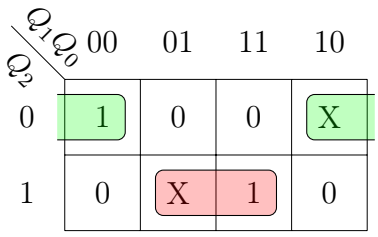
Karnaugh Maps:



T_2



T_1



T_0

Simplified Boolean Expression:

$$T_2 = Q_2'Q_1 + Q_2Q_1'$$
$$T_1 = Q_1'Q_0 + Q_1Q_0'$$
$$T_0 = Q_2'Q_0' + Q_2Q_0$$

In this case, the actual state table is:

Current State			Next State			TFF Inputs		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	1	0	1	1	1	1
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	0	1	0	1	1	1
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

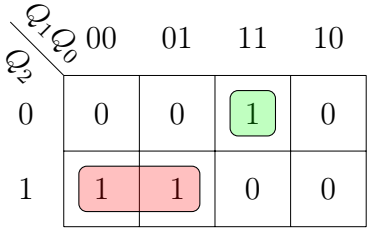
As shown in the state table, the states with don't cares form a loop. Thus, the counter may not work properly.

Unused States Redirection

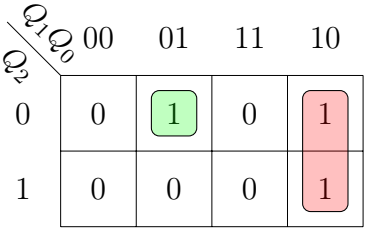
To address the problem, we can redirect all unused states to valid states. For example, we can redirect 010 and 101 to 000 at next clock pulse. **This is not the only correct answer, you can redirect unused states to any valid state as you want!**
State Table with TFF Inputs:

Current State			Next State			TFF Inputs		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	0	0	0	0	1	0
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	0	0	0	1	0	1
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

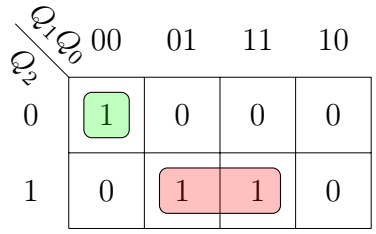
Karnaugh Maps:



T_2



T_1



T_0

Simplified Boolean Expression:

$$
\begin{aligned}
T_2 =& Q_2Q_1' + Q_2'Q_1Q_0 \\
T_1 =& Q_1Q_0' + Q_2'Q_1'Q_0 \\
T_0 =& Q_2Q_0 + Q_2'Q_1'Q_0'
\end{aligned}
$$