UDP_IP_Core:1

vcc

P

XST_VCC

MATCH_CMD

CmdToMatch(7:0)

DataToMatch(7:0)

clk

DataValid

rst

sof

CmdMatched

MATCH_RST_CODE

clk_125MHz

rst

rx_sof

input_bus(7:0)

rx_eof

FLEX_CONTROL

r_data(7:0)

r_usrdata(7:0)

clk

rst

r_eof

r_sof

r_usrvld

checksum_baseval(15:0)

l_addr(5:0)

l_data(7:0)

locked

l_wren

FLEX_CONTROL_port_map

locked

IPv4_PACKET_RECEIVER

input_bus(7:0)

clk_125Mhz

rst

rx_eof

rx_sof

usr_data_length(15:0)

usr_data_output_bus(7:0)

valid_out_usr_data

IPv4_PACKET_RECEIVER_port_map

usr_data_length(15:0)

usr_data_output_bus(7:0)

valid_out_usr_data

IPV4_PACKET_TRANSMITTER

flex_checksum_baseval(15:0)

flex_wraddr(5:0)

flex_wrdata(7:0)

transmit_data_input_bus(7:0)

transmit_data_length(15:0)

clk_125MHz

flex_wren

rst

transmit_start_enable

transmit_data_output_bus(7:0)

end_of_frame_O

source_ready

start_of_frame_O

usr_data_trans_phase_on

IPV4_PACKET_TRANSMITTER_port_map

transmit_data_output_bus(7:0)

end_of_frame_O

source_ready

start_of_frame_O

usr_data_trans_phase_on

transmit_data_input_bus(7:0)

transmit_data_length(15:0)

transmit_start_enable

UDP_IP_Core