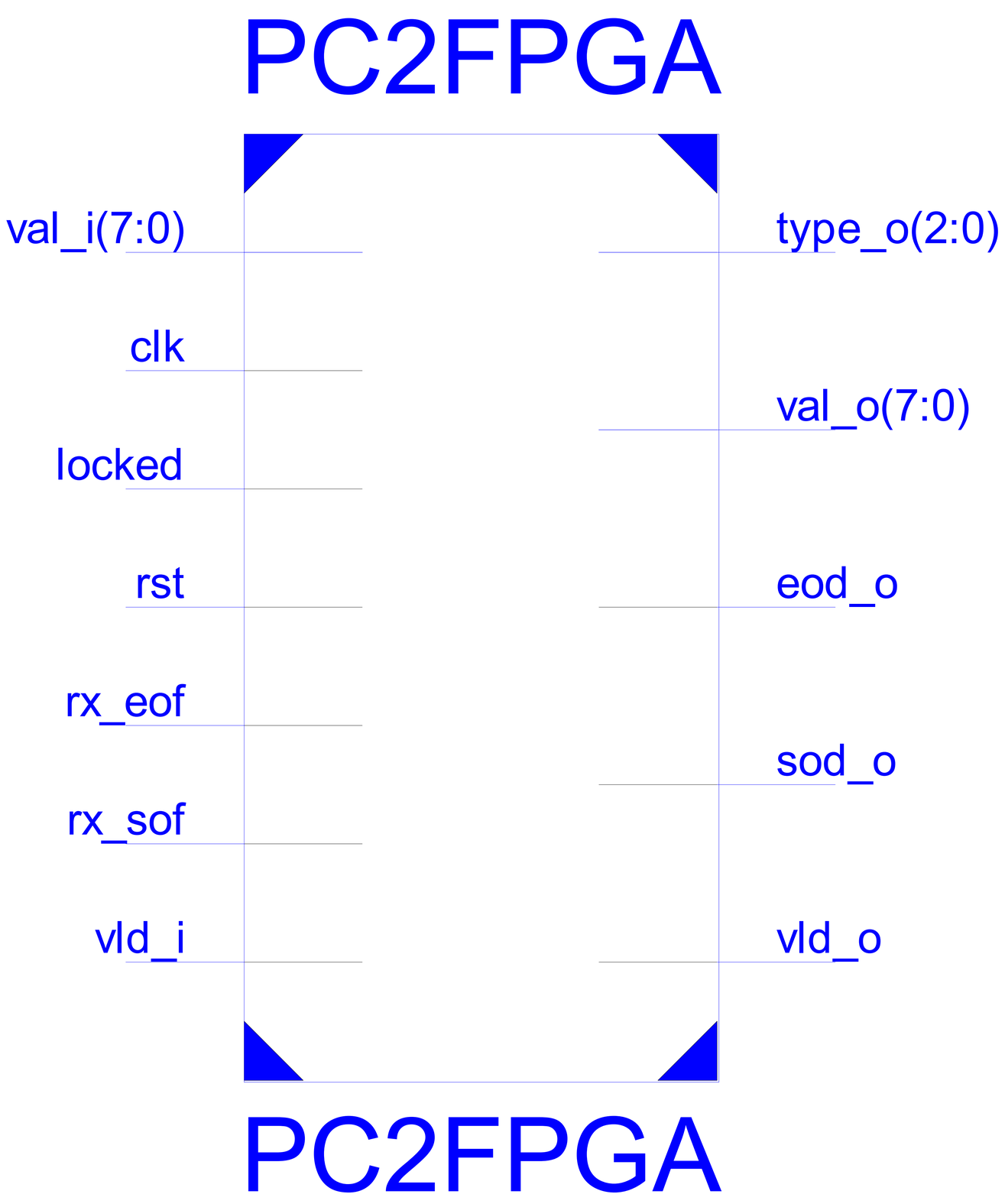
PC2FPGA
val_i(7:0)
clk
locked
rst
rx_eof
rx_sof
vld_i
type_o(2:0)
val_o(7:0)
eod_o
sod_o
vld_o
PC2FPGA