



BigBrainCPU

Aayush Patel, Yash Tyagi, Vishal Narasimhan

Advanced Features

Tournament Branch Predictor / BTB	Return Address Stack	Eviction Write Buffer	Prefetcher	L2 Cache
<ul style="list-style-type: none">• Local & Global Predictor• Global BHR/PHT• 2-bit State Counters• 32 Entries	<ul style="list-style-type: none">• 8 entry stack• RISC-V calls and returns with registers x1 and x5	<ul style="list-style-type: none">• Single buffer• Handled dirty and clean evictions	<ul style="list-style-type: none">• One Block Lookahead Prefetcher (OBL)• Added to instruction cache• Modified arbiter and cache to support prefetcher	<ul style="list-style-type: none">• 2-way set associative with 16 sets• Between arbiter and memory (cache-line adaptor)

Quantitative Results

Tournament Branch Predictor / BTB	Return Address Stack	Eviction Write Buffer	Prefetcher	L2 Cache
<p>Total Branches: 12774</p> <p>Total JALR: 3079</p> <p>BTB: 9417 (97.1%)</p> <p>Global: 323</p> <p>Local: 1862</p> <p># of Flushes: 9369 vs. 3357 (35.8%)</p>	<p>Total JALR: 2978</p> <p>RAS Correct: 1478</p> <p>Half of the JALR instructions were used to call functions</p> <p>The other half were used to return with 98.6% accuracy</p>	<p>D-Cache stall time</p> <ul style="list-style-type: none"> Before: 89182 After: 64187 <p>I-Cache hit cycles</p> <ul style="list-style-type: none"> Before: 139546 After: 114550 <p>Other metrics stayed relatively the same</p>	<p>I-Cache Misses</p> <ul style="list-style-type: none"> Before: 91 After: 78 <p>I-Cache Stall Time</p> <ul style="list-style-type: none"> Before: 5183 After: 4097 <p>I-Cache Hit Cycles</p> <ul style="list-style-type: none"> Before: 113633 After: 114550 	<p>I-Cache Stall Time</p> <ul style="list-style-type: none"> Before: 4923 After: 4087 <p>D-Cache Stall Time</p> <ul style="list-style-type: none"> Before: 123837 After: 89182 <p>I-Cache Hit Cycles</p> <ul style="list-style-type: none"> Before: 173806 After: 214868

Final Reflections

Tournament Branch Predictor / BTB	Return Address Stack	Eviction Write Buffer	Prefetcher	L2 Cache
<p>Parameterized BTB and Predictors</p> <p><i>Considerations:</i></p> <ul style="list-style-type: none"> • BTB Size • Mispredictions <p><i>Improvements:</i></p> <ul style="list-style-type: none"> • Resolve branch earlier • BHR/Predictor Size 	<p>Parameterized RAS Size</p> <p><i>Considerations:</i></p> <ul style="list-style-type: none"> • Size <p><i>Improvements:</i></p> <ul style="list-style-type: none"> • What to do when stack is full 	<p><i>Considerations:</i></p> <ul style="list-style-type: none"> • Placement in memory subsystem <p><i>Improvements:</i></p> <ul style="list-style-type: none"> • Add more line buffers 	<p><i>Considerations:</i></p> <ul style="list-style-type: none"> • Priority in memory access • Interference in regular program execution <p><i>Improvements:</i></p> <ul style="list-style-type: none"> • FSM -> More Ports • Stride Prefetching 	<p><i>Considerations:</i></p> <ul style="list-style-type: none"> • Size of L2 Cache • Line Size <p><i>Improvements:</i></p> <ul style="list-style-type: none"> • Add more ways • Make line size bigger