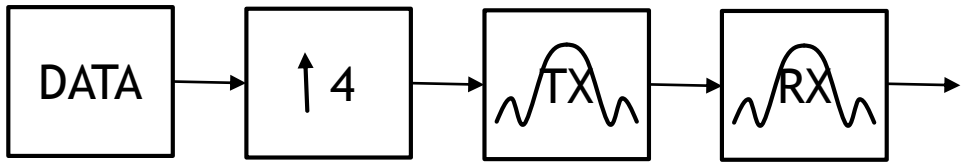
EE 465

FILTER DESIGN - 1

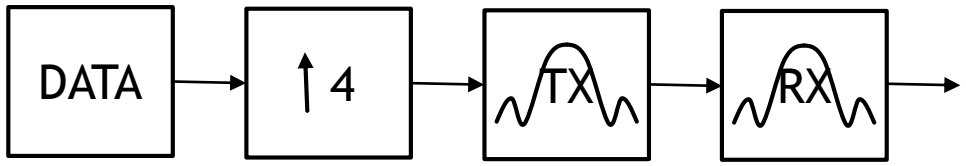
Rory Gowen

University of Saskatchewan

System Structure



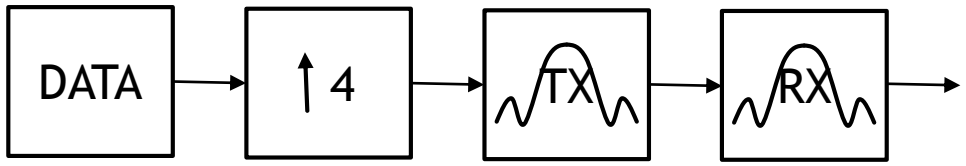
System Structure



DATA is a signal that represents a group of bits that are called a symbol

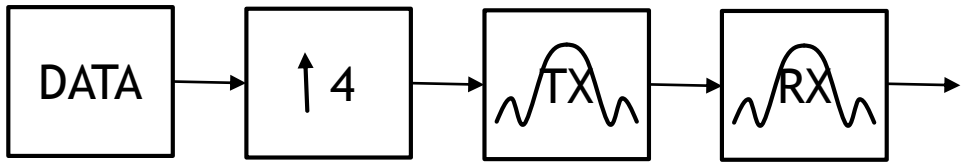
In a BPSK system there are only two digital values that can be sent, either 0 or 1.

Conditioning DATA



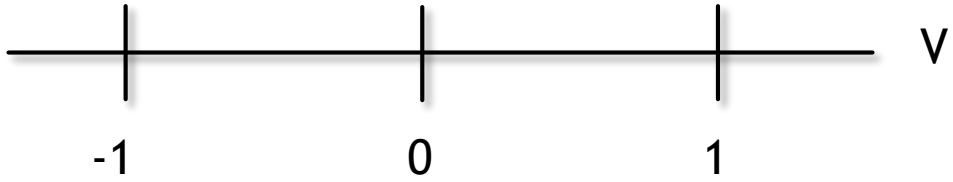
How can we transmit digital symbols through a filter that requires a 1s17 (or multi-level signal)?

Conditioning DATA

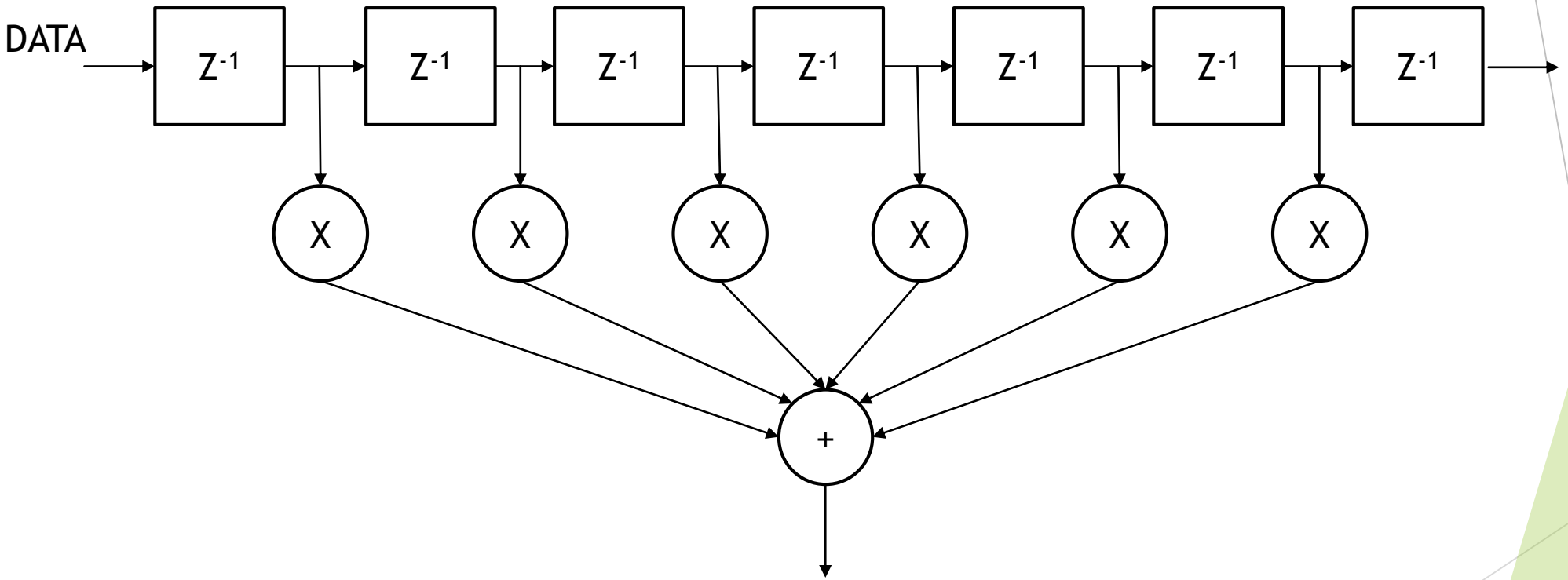


How can we transmit digital symbols through a filter that requires a 1s17 (or multi-level signal)?

Map the symbol to a voltage/multi-level value - DATA

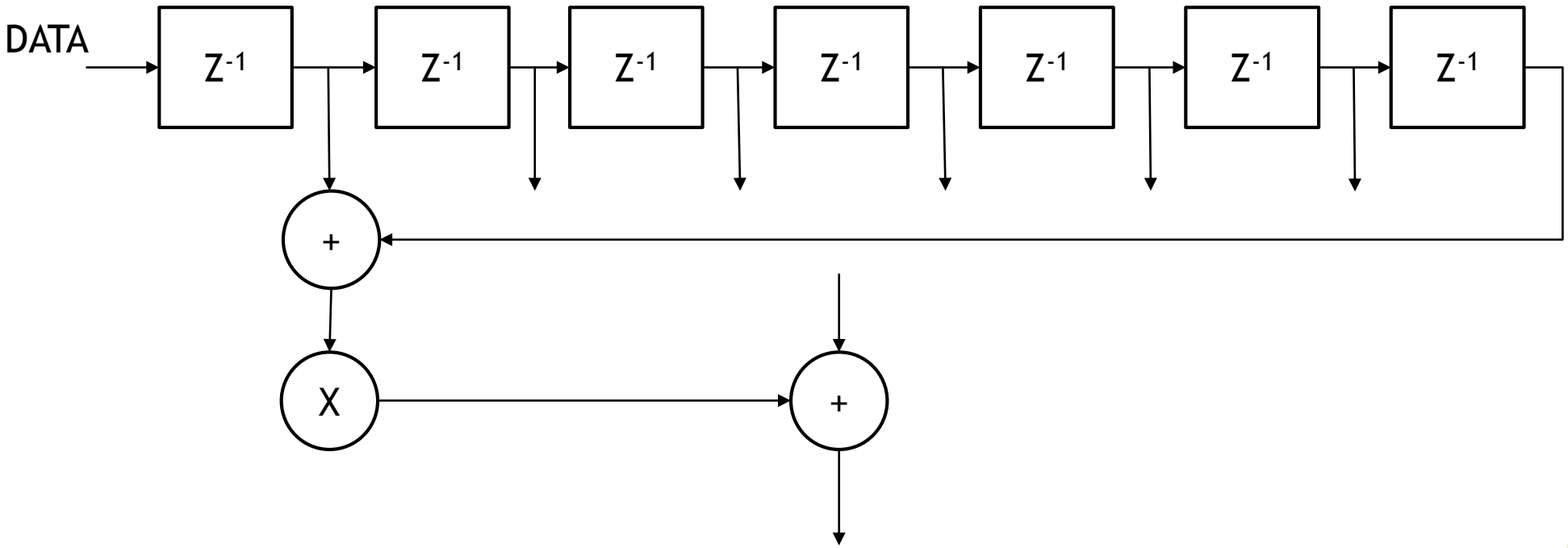


Pulse-Shaping Filter (TX and RX)

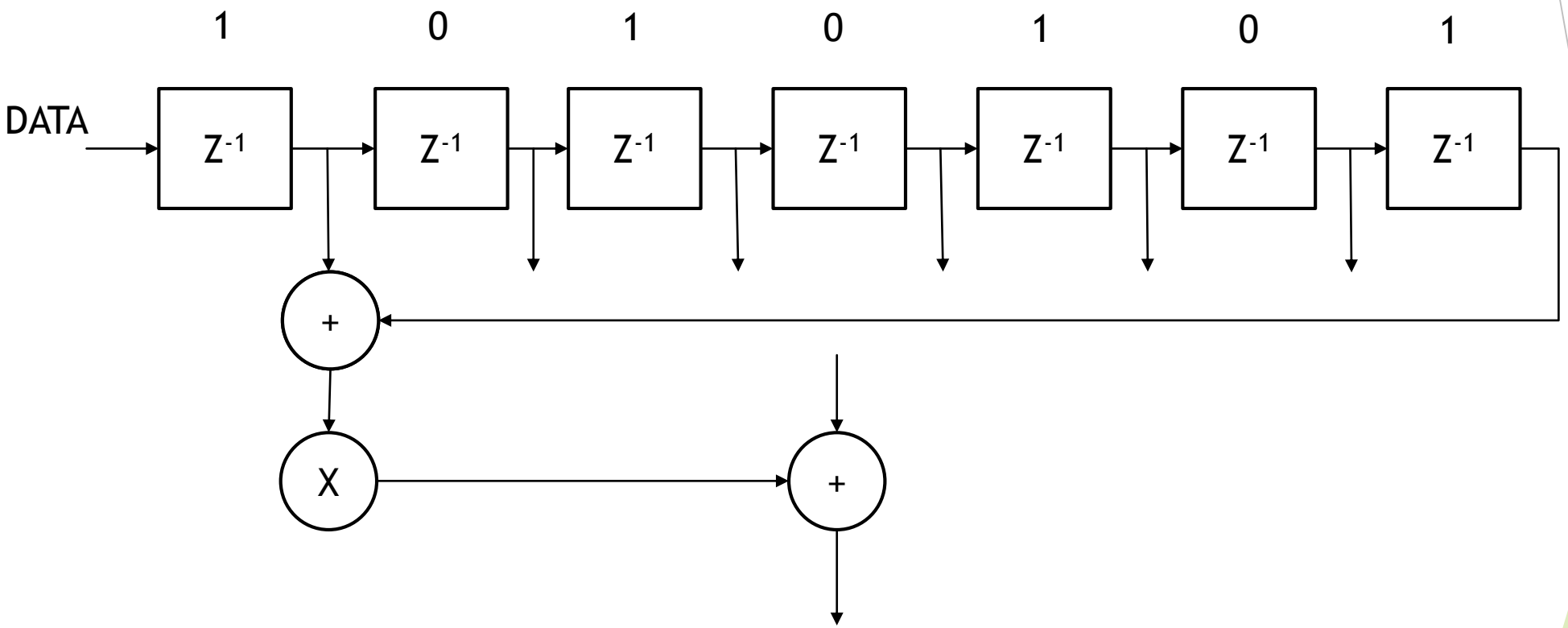


Is there a way to reduce multipliers?
Why would we want to reduce multipliers?

Pulse-Shaping Filter (Symmetry)

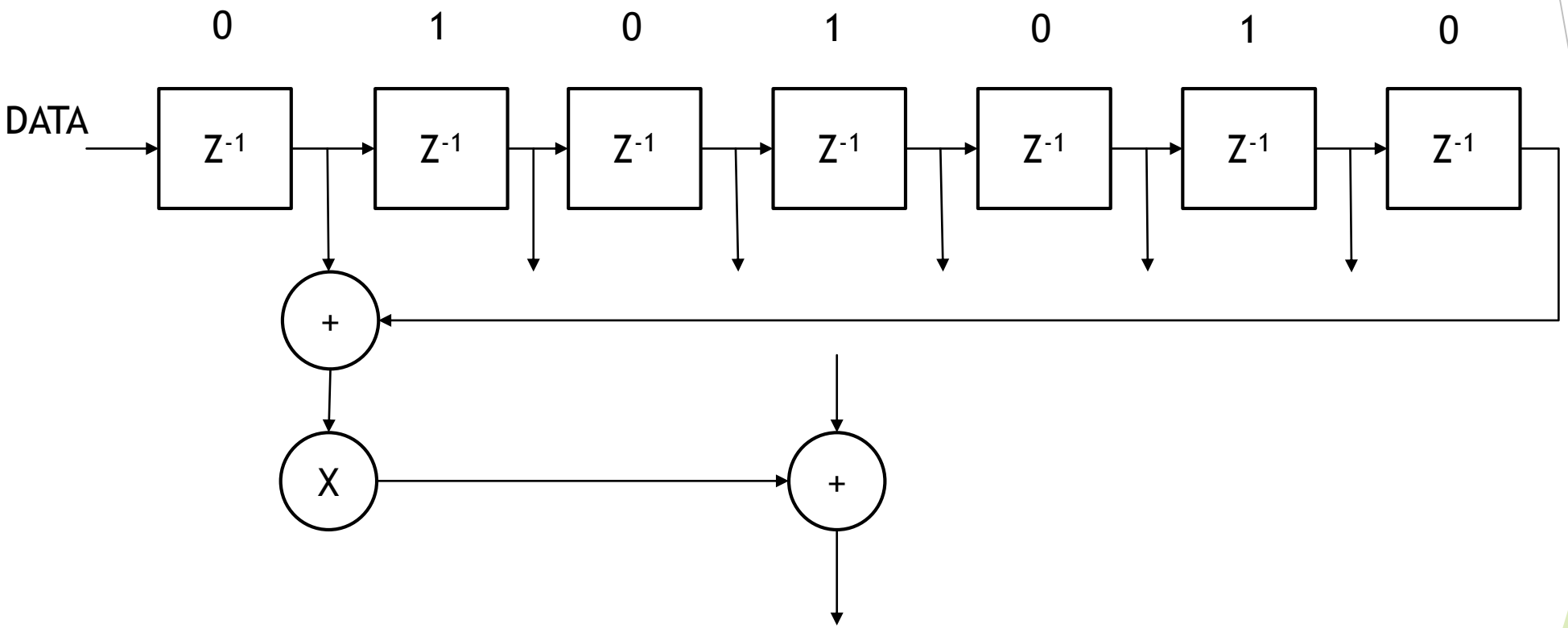


Pulse-Shaping Filter (zero-stuffing)

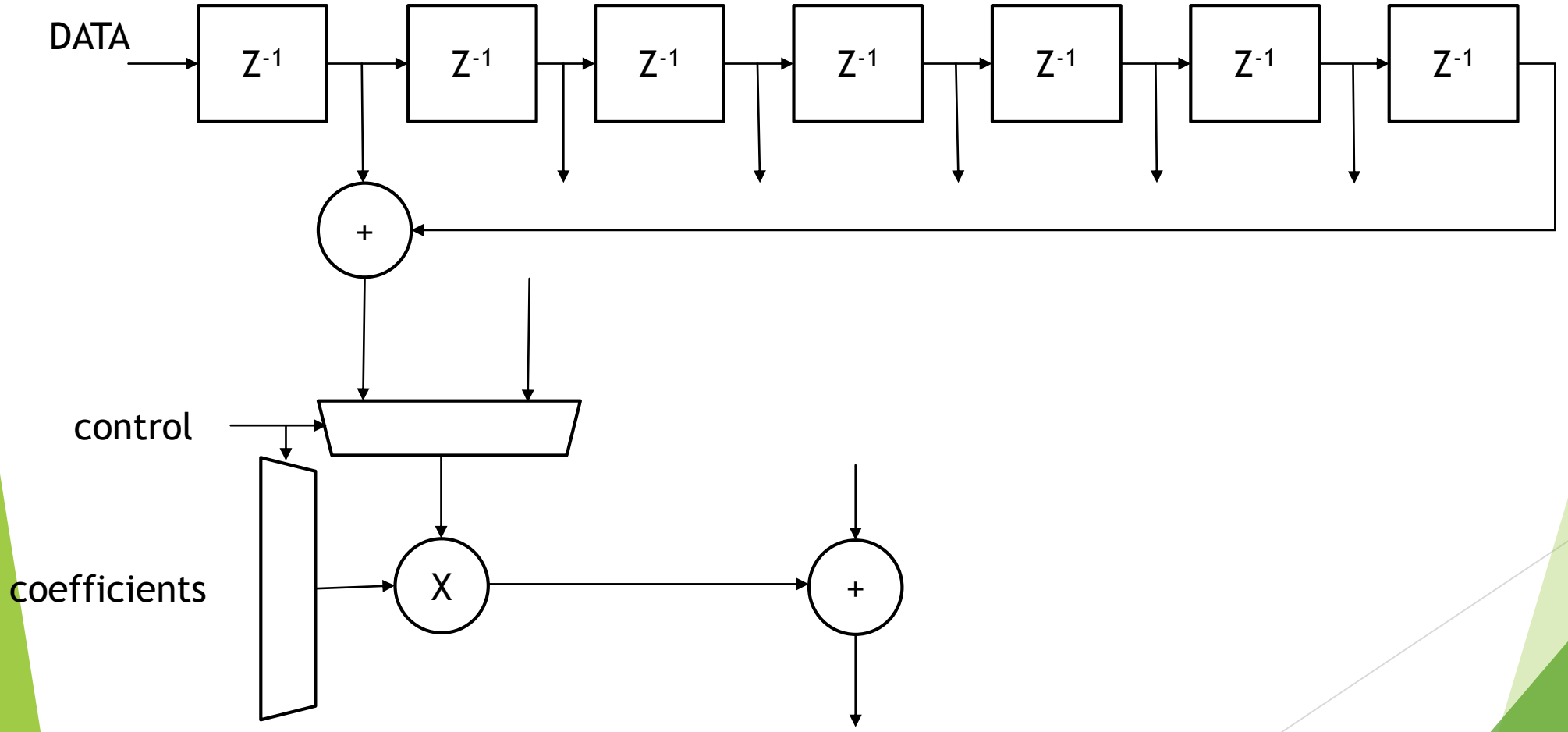


Simplified upsampling by 2, instead of 4 for illustrative purposes

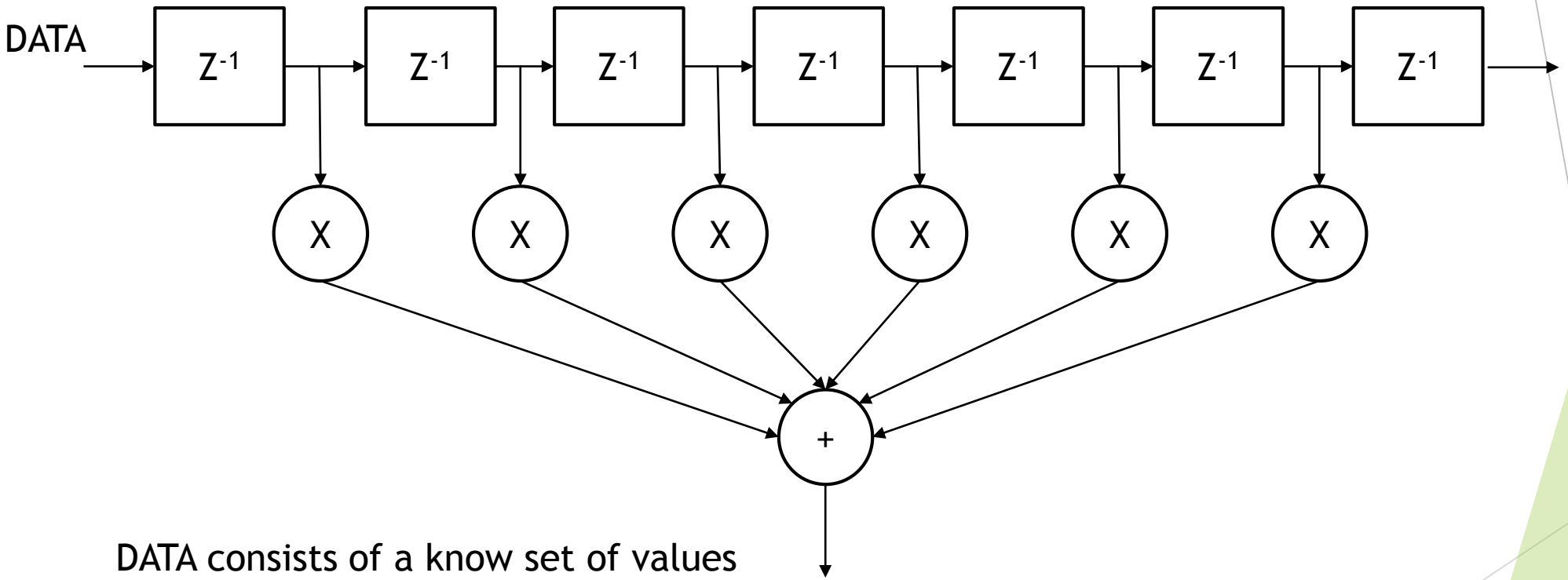
Pulse-Shaping Filter (zero-stuffing)



Pulse-Shaping Filter (zero-stuffing)

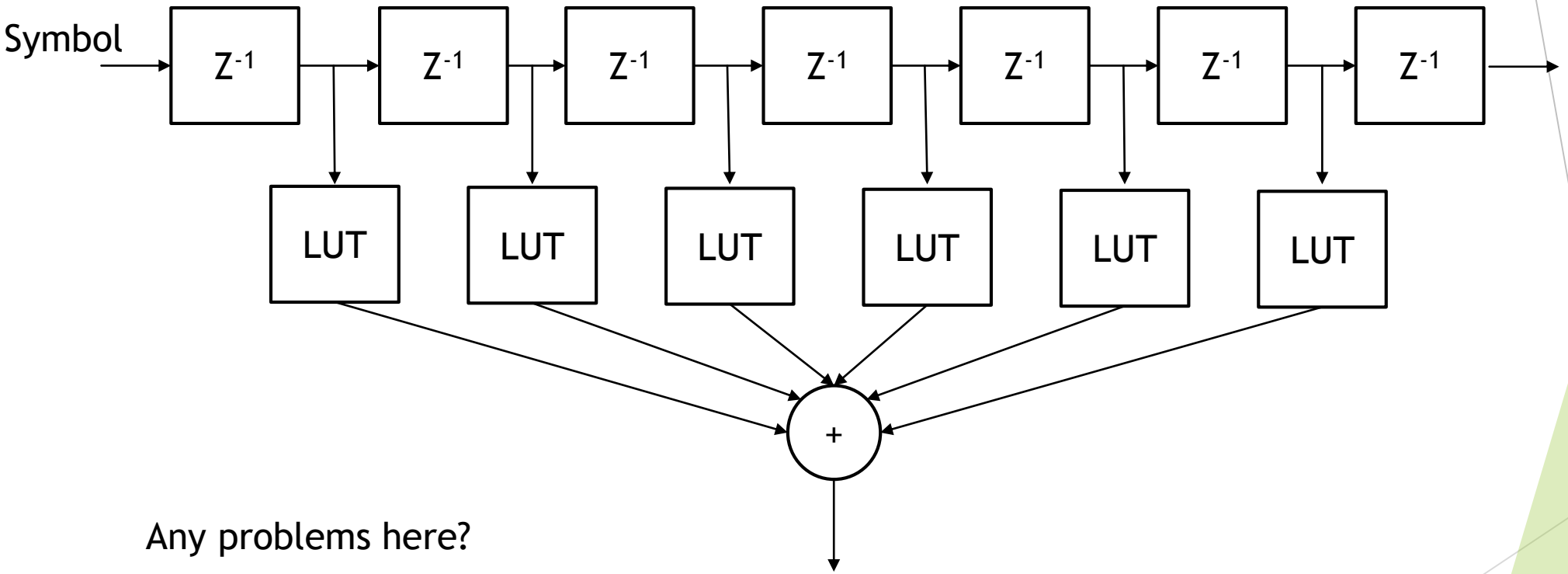


Pulse-Shaping Filter (TX)



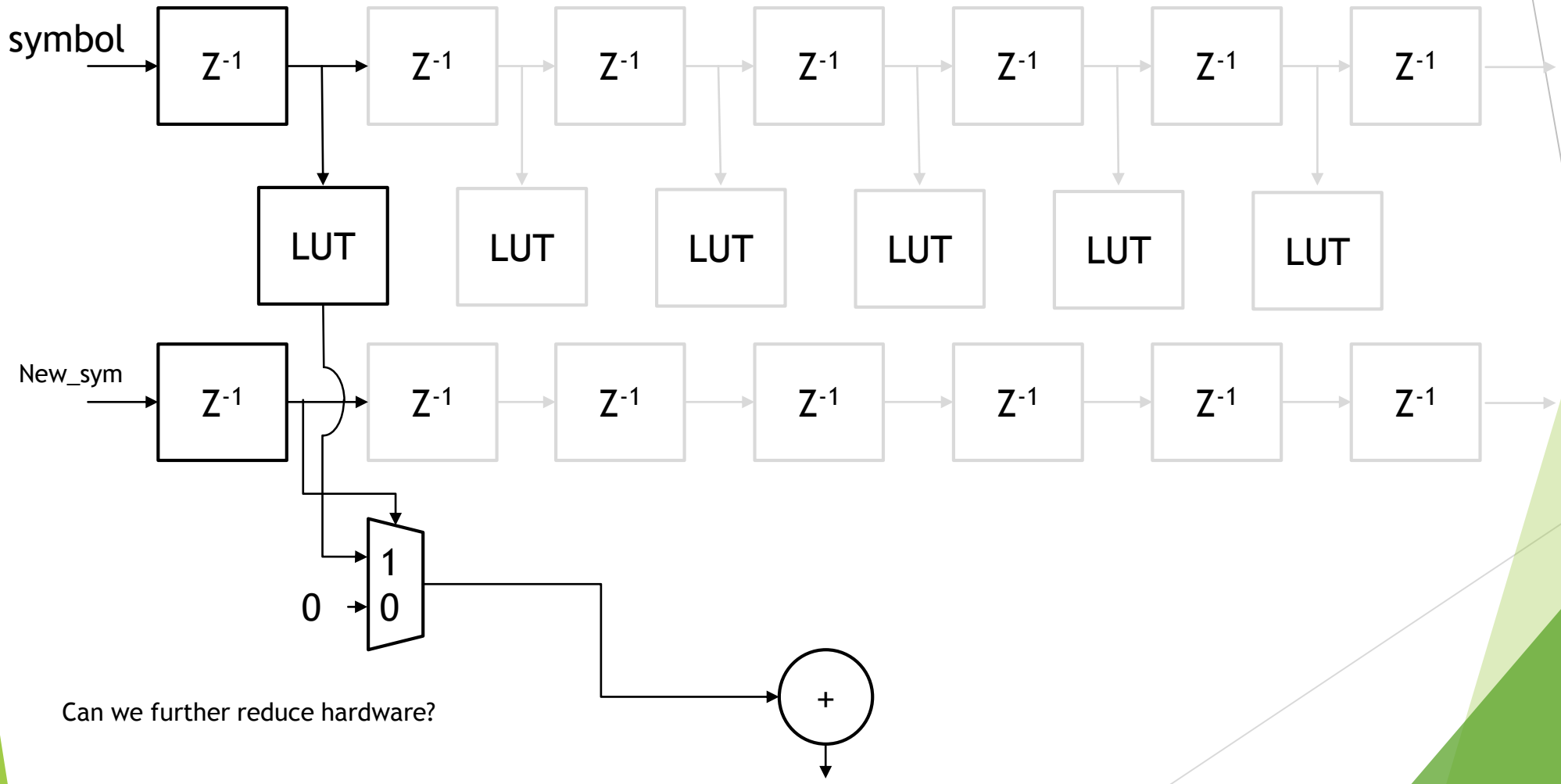
DATA consists of a know set of values
Do we need multipliers?

Pulse-Shaping Filter



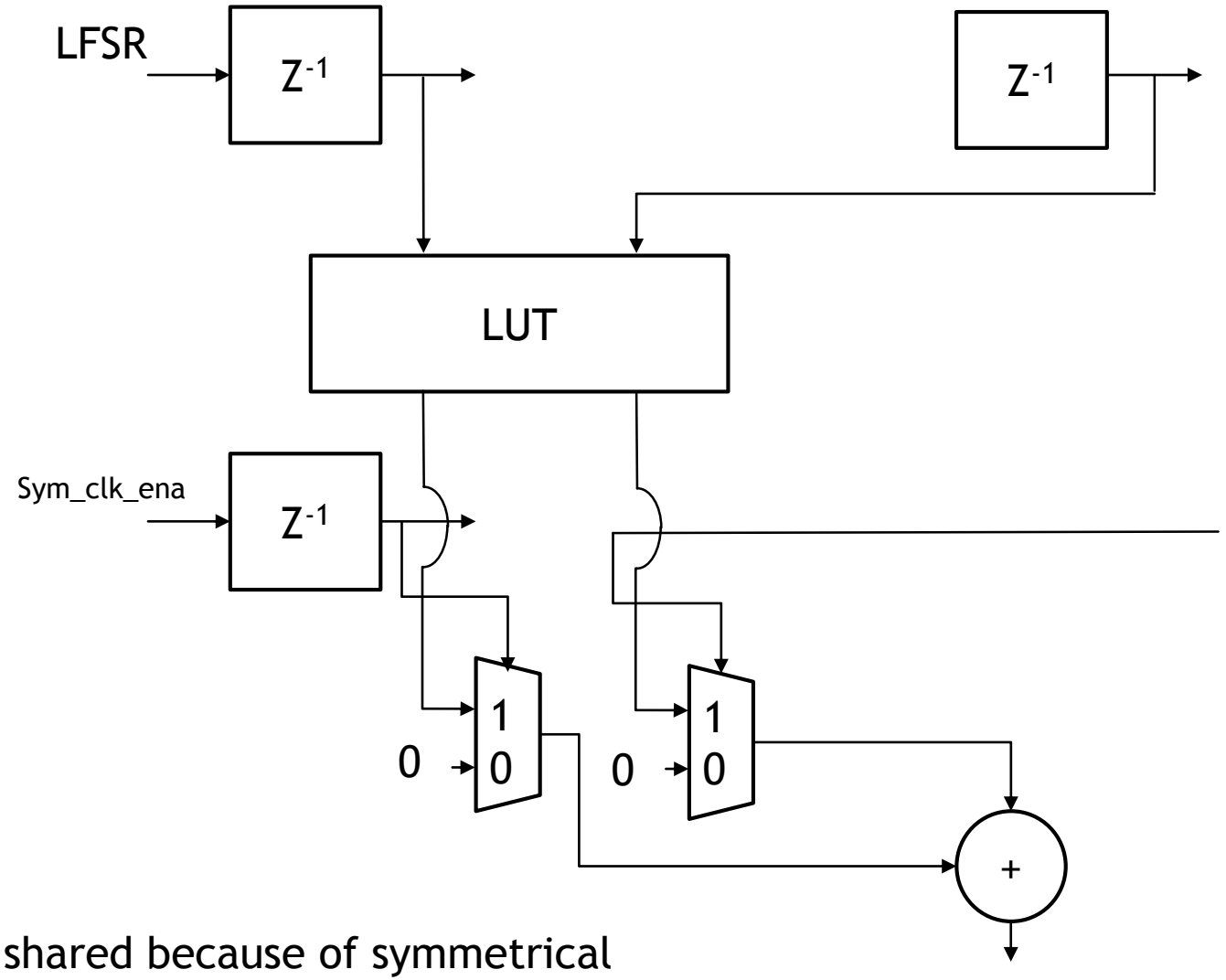
Any problems here?

Pulse-Shaping Filter



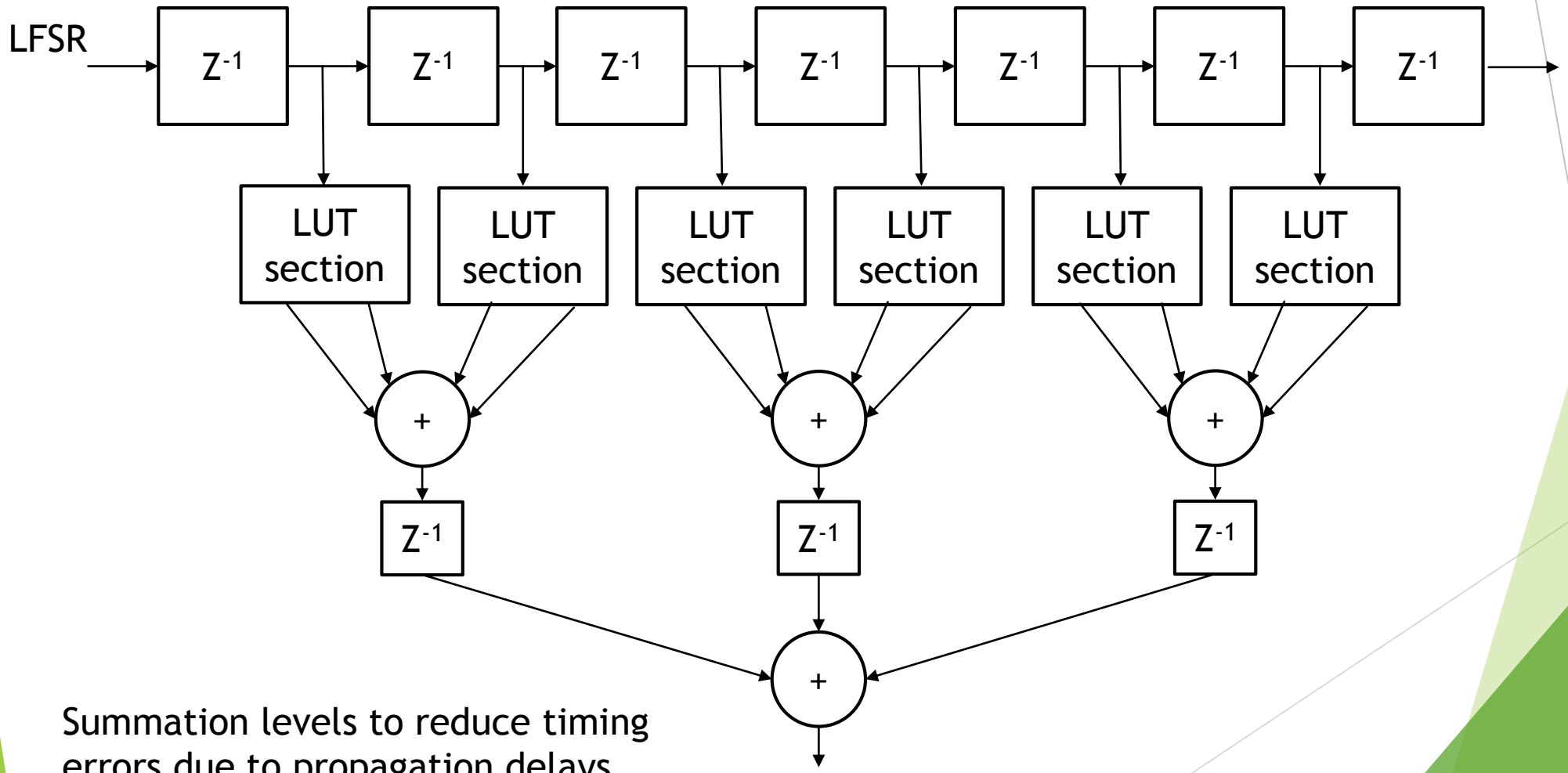
Can we further reduce hardware?

Pulse-Shaping Filter



LUTs shared because of symmetrical response

Pulse-Shaping Filter



Summation levels to reduce timing errors due to propagation delays