# Comparison of a BSIM3V3 and EKV MOSFET Model for a 0.5 $\mu$m CMOS Process and Implications for Analog Circuit Design

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***Abstract*—Design requirements for high-density detector front-ends and other high-performance analog systems routinely force designers to operate devices in moderate inversion. However, CMOS models have traditionally not handled this operating region very well. In this paper, the Berkeley Short-Channel IFGET Model (BSIM3V3) and EKV 2.6 MOSFET models are evaluated in terms of their ability to model low-voltage analog circuits. Simulation results for a standard 0.5 $\mu$m CMOS process are presented and compared to measured data. The data presented includes simulated and measured output conductance and transconductance efficiency for devices with channel lengths ranging from 0.5 $\mu$m to 33 $\mu$m. In addition, the models are compared in terms of their ability to handle the different operating regions of the MOS transistor (weak, moderate, and strong inversion). The results highlight the difficulty of obtaining a model that accurately predicts the operation of high-performance analog systems.**

***Index Terms*—Analog circuit design, BSIM3V3, CMOS modeling, EKV 2.6, inversion coefficient, transconductnce efficiency.**

## I. Introduction

In all high-performance analog signal processors, power efficiency, speed, noise, and dynamic range must be traded against one another to find an optimum device bias condition for a given application. Power efficiency is particularly important in high-density, low-noise signal processors such as detector front-ends [1], [2]. Additionally, dynamic range is greatly limited in modern submicrometer CMOS circuits because the power supply voltage scales with the technology, but threshold voltage does not [3]. Because of these constraints designers are often forced to operate critical devices in moderate inversion, where the accuracy of the model is questionable. Conversely, time-to-market and cost concerns are forcing designers to rely more-and-more on Spice for design verification, and less-and-less on prototyping and measurement. For instance, the chip reported in [4] is 20 $\mathrm{mm}^2$, contains nearly 15 000 transistors and went to full production without ever prototyping the complete system. Considering that the model will always limit the accuracy of the simulation, it is very important that a designer be aware of the capabilities and limitations of their CMOS model.

The purpose of this paper is to inform the reader about the current state of CMOS simulation models for low-voltage analog design. First, a method of characterizing MOS devices that highlights device operation over a continuum of inversion levels will be presented. Next, two popular simulation models, BSIM3V3 and EKV 2.6, will be introduced and discussed. Then simulation results of MOS devices over many decades of channel inversion, obtained using both the BSIM3V3 and EKV 2.6 models, will be shown and compared to measurement results. By comparing the results of two different MOS models with measured results it is possible to evaluate the strengths and weaknesses of each model. Finally, the implications of the results, as they apply to modeling low-voltage analog circuits, will be discussed.

## II. CMOS Process Characterization for Analog Design

Traditional methods of characterizing a semiconductor technology involve generating $I$-$V$ curves, the most common being $I_d$ versus $V_{ds}$ and $I_d$ versus $V_{gs}$. While these methods are useful for the large signal characterization of a device, it is difficult to apply them directly to the design of low-voltage CMOS circuits because they do not highlight the different operating regions of the MOS transistor. Recently, a new method of characterizing a CMOS technology, which is intended specifically for low-voltage analog circuit design, has been developed. The salient feature of this method is that it highlights device operation over the entire continuum of inversion levels, thus, the designer does not feel restricted to operate a device in only one region [5], [6]. The foundations of the new method are the concepts of transconductance efficiency and inversion coefficient.

Transconductance efficiency is defined as the ratio of the transconductance $g_m$ to drain current $I_d$. Fig. 1 shows a plot of $g_m$-efficiency versus normalized drain current, where normalized drain current is the drain current for a device with an aspect ratio of unity. In Fig. 1 the weak inversion region is where the slope of the $g_m$-efficiency is zero on a log scale, because in this region transconductance is proportional to drain current. Strong inversion is where the slope of the $g_m$-efficiency is $-1/2$, because in this region transconductance is proportional

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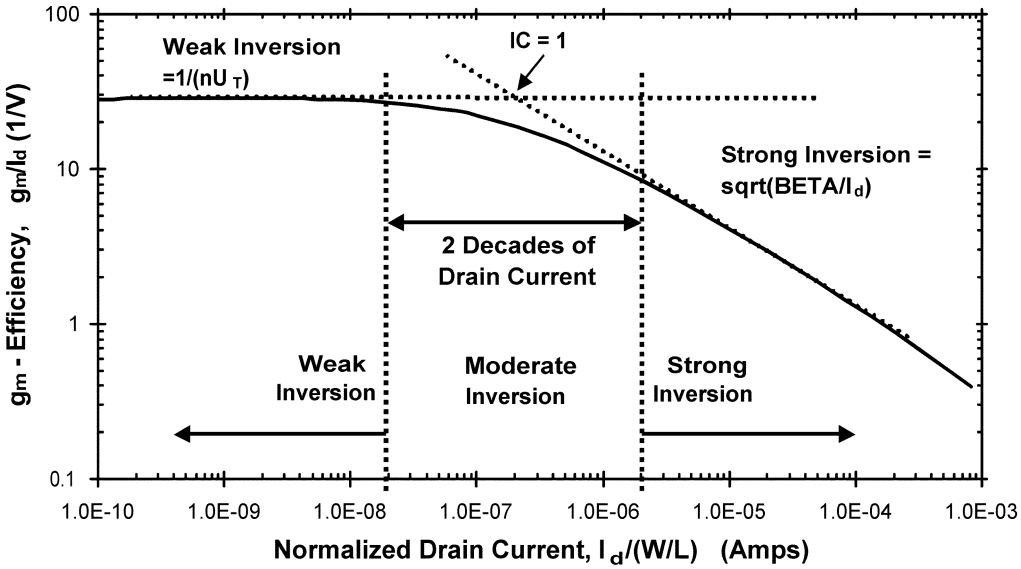


Fig. 1. MOSFET transconductance efficiency versus normalized drain current. (Note: $\mathrm{BETA} = \mu C_{\mathrm{ox}}(\mathrm{W}/\mathrm{L})$.)

to the square root of drain current, and moderate inversion is the transition region between weak and strong inversion. The center of the moderate inversion region is the intersection of the weak and strong inversion asymptotes [7], [8].

One of the most important characteristics of the $g_m$-efficiency plot is that there are roughly two decades of drain current between the weak and strong inversion regions. This is in fact a fundamental property of MOSFETs, and it has been shown to hold true for both PMOS and NMOS devices with gate lengths ranging from submicrometer to very long channels [7]. The regularity shown by MOSFET $g_m$-efficiency leads to the concept of inversion coefficient, which is a method of quantifying the inversion level of the channel. Inversion coefficient [8] is precisely defined as the normalized forward current of the MOSFET

$$IC = \frac{I_F}{2n\mu C_{\mathrm{ox}}\left(\frac{W}{L}\right)U_T^2} \tag{1}$$

where $I_F$ is the drain current in saturation, $n$ is the subthreshold slope factor, $\mu$ is the mobility, and $W$ and $L$ are the effective channel width and length, respectively, $U_T = (kT/q)$ is the thermal voltage and $C_{\mathrm{ox}}$ is the gate oxide capacitance per unit area. A simpler form of inversion coefficient can be found by defining a bias independent parameter known as the technology current $I_0$, which is equal to the normalized drain current of a device that is biased at the center of moderate inversion (i.e., the intersection of the weak and strong inversion asymptotes). The fixed inversion coefficient [6], [9] is then defined as

$$IC_0 = \frac{I_d}{I_0\left(\frac{W}{L}\right)}. \tag{2}$$

Equation (2) shows that the inversion coefficient at the center of moderate inversion is 1. Since a MOSFET has a two decade current transition from weak to strong inversion, the moderate inversion region will be bounded by $IC_0 = 0.1$ and $IC_0 = 10$. Therefore, a device with an inversion coefficient less than 0.1 will be operating in weak inversion and a device with an inversion coefficient greater than ten will be operating in strong inversion. Inversion coefficient is an important idea for analog design because it frees the designer to consider how a circuit will perform as a device is biased in different operating regions. It has been introduced here as a framework for examining the performance of a MOS model over all operating regions and inversion levels.

## III. MOSFET Simulation Models

Analog designers have traditionally had a love–hate relationship with circuit simulators. On one hand circuit simulators offer the possibility of quickly analyzing and troubleshooting very complex circuits. However, the model always limits the accuracy of a simulation, and there have been many examples of MOS models, which are adequate for digital simulations, but neglect effects that are important in analog circuits [10]. The two models being studied in this work come from quite different backgrounds and take very different approaches to MOS modeling. The Berkeley Short-Channel IFGET Model (BSIM) family of models, developed at the University of California at Berkeley, was introduced in the late 1980s as a general purpose, compact model for short channel FETs [11]. BSIM3V3, currently the most widely used BSIM version, is a very complex model that is generally well suited for analog circuit simulation. BSIM3V3 is a highly empirical model that relies on a large number of fitting parameters to achieve good agreement with measured results. In fact, the intrinsic dc model alone requires nearly 100 parameters. The highly empirical nature of the model means that parameter extraction is a very difficult task [12].

The Enz–Krummenacher–Vittoz (EKV) model is unique in that it was developed specifically to aid in the design of low-voltage/low-current analog circuits [13]. In general, the model provides very good simulation results for analog circuits and it excels when modeling devices operating in moderate or weak inversion. Amazingly, the EKV 2.6 model requires only 18 intrinsic dc parameters to achieve these results [14]. EKV requires fewer parameters because it uses a physics based approach for the development of the model equations. The physics

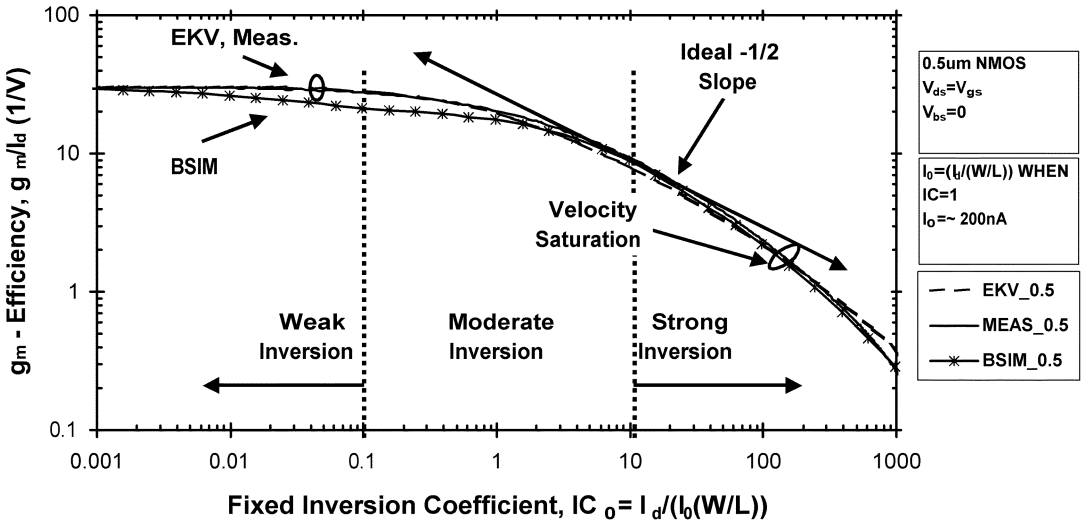


Fig. 2. NMOS transconductance efficiency versus inversion coefficient for short channel FETs.

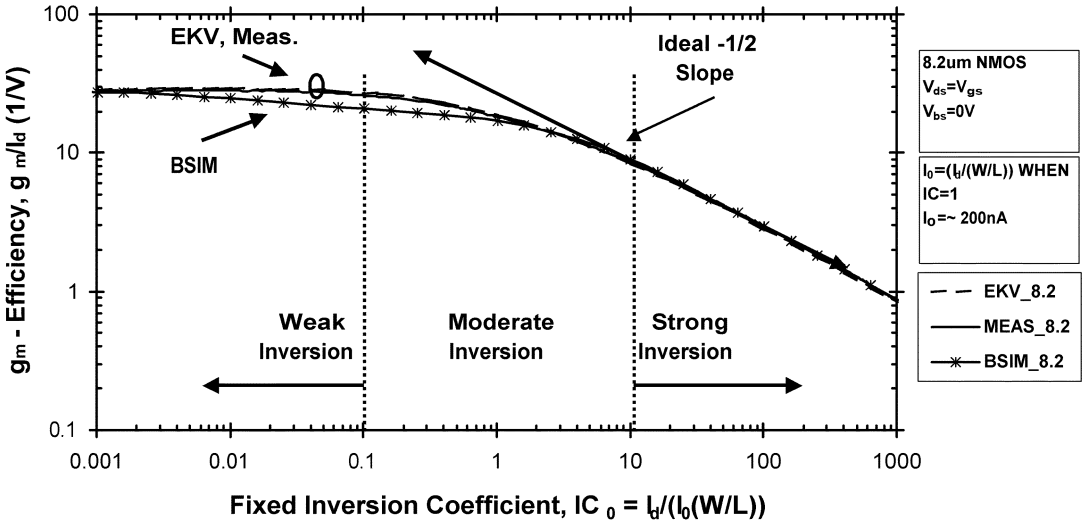


Fig. 3. NMOS transconductance efficiency versus inversion coefficient for long channel FETs.

based approach means that the model is more closely linked to the process parameters, and it makes parameter extraction a much simpler task [12]. Most major Spice simulators support EKV Version 2.6, including Synopsys' Hspice (Level 55), and Mentor Graphics' Eldo (Level 44) [14]. Readers interested in learning more about the inner workings of the BSIM3V3 and EKV models are referred to [12]–[15].

## IV. Measurement and Simulation Results

### A. Simulation Methodology

To evaluate the models for low-voltage analog circuit design, $g_m$ and $g_{ds}$ were simulated for devices with gate lengths ranging from 0.5 $\mu$m to 33 $\mu$m. These two parameters were chosen because they have a first order effect on several important op-amp characteristics, and because they represent a difficult benchmark for a MOS model. Additionally, $I_d$ versus $V_{gs}$ was simulated in order to characterize the large-signal accuracy of the models. In all simulations the device being measured was connected as a MOS diode ($V_{gs} = V_{ds}$), and the drain current was swept from 1 nA to 10 mA. The simulations were performed in this manner because this corresponds to the functionality of the parameter analyzer used for the measurements. The BSIM3V3 and EKV 2.6 models used in this work both represent "typical foundry models" and were in no way optimized for these tests.

### B. Measurement Methodology

$g_m$, $g_{ds}$ and $I_d$ versus $V_{gs}$ were also measured on several test devices with gate lengths ranging from 0.5 $\mu$m to 33 $\mu$m. The measurements were made using a custom semiconductor parameter analyzer with a current sweep from 1 nA to 10 mA. The analyzer guarantees $V_{gs} = V_{ds}$ while all measurements are made.

### C. Transconductance Efficiency Simulations

Figs. 2 and 3 show the $g_m$-efficiency measurement and simulation results as a function of fixed inversion coefficient. For each plot, the measured data was normalized to have the same weak inversion asymptote as the simulation results. This was

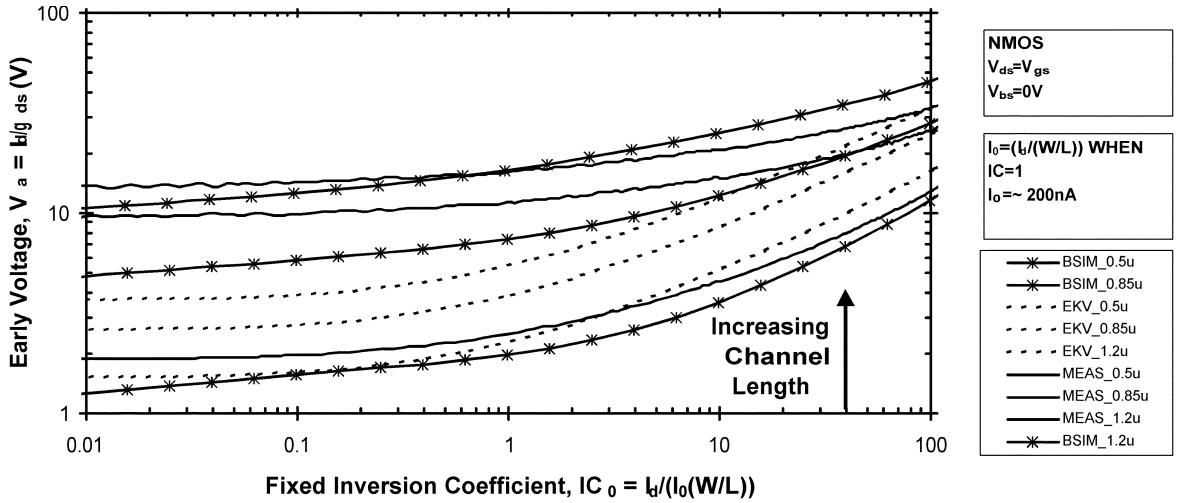


Fig. 4. NMOS *early* voltage versus inversion coefficient for short channel FETs.

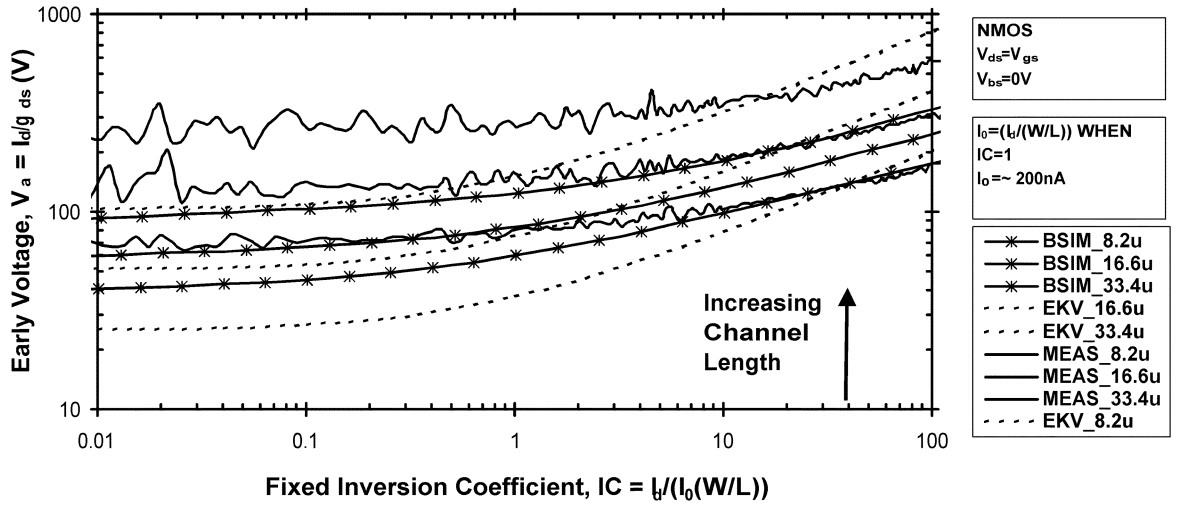


Fig. 5. NMOS *early* voltage versus inversion coefficient for long channel FETs.

done to allow a "fair" comparison between measurement and simulation.

Fig. 2 shows the results for a short channel ($L = 0.5\ \mu\text{m}$) NMOS device. One can see that both models correctly predict the transconductance in deep weak inversion and throughout strong inversion, however, EKV 2.6 is superior in the region $0.01 < IC_0 < 1$. In this region BSIM3V3 is in error by as much as 40%. Note that when the devices enter strong inversion they begin to deviate significantly from the ideal $-1/2$ slope because of velocity saturation and other short channel effects.

Fig. 3 presents the transconductance efficiency results for a long channel ($L = 8\ \mu\text{m}$) NMOS device. Again BSIM3V3 and EKV 2.6 agree in deep weak inversion and throughout strong inversion, however, in the upper end of weak inversion and the lower half of moderate inversion ($0.01 < IC_0 < 1$) BSIM3V3 shows an error of roughly 40%. From these plots one can see that EKV 2.6 provides nearly ideal results at all levels of channel inversion. BSIM3V3 provides good results in for $IC_0 < 0.01$ and $IC_0 > 10$, however, it shows a large error in the region $0.01 < IC_0 < 1$ that is independent of channel length.

### D. Output Conductance Simulations

Figs. 4 and 5 show the measurement and simulation results for NMOS *early* voltage

$$V_a = \frac{I_d}{g_{ds}} \tag{3}$$

as a function of fixed inversion coefficient. Fig. 4 shows the results for three devices with gate lengths ranging from 0.5 $\mu$m to 1.2 $\mu$m, and Fig. 5 shows the results for three devices with gate lengths ranging from 8.2 $\mu$m to 33.4 $\mu$m.

In Fig. 4 the measurements agree with both models reasonably well for the $L = 0.5\ \mu\text{m}$ case. However, the $L = 0.85\ \mu\text{m}$ and $L = 1.2\ \mu\text{m}$ deviate significantly from the measurements for both models. For BSIM3V3 the general trend of the curves is correct, notice that the large change in $V_a$ in going from $L = 0.5\ \mu\text{m}$ to $L = 0.85\ \mu\text{m}$ is present in both BSIM3V3 and measurements. On the other hand the EKV 2.6 model shows a much smaller change in $V_a$ in going from $L = 0.5\ \mu\text{m}$ to $L = 0.85\ \mu\text{m}$.

In Fig. 5 the trends of all the curves are more similar. The relative spacing between the curves for different channel lengths is

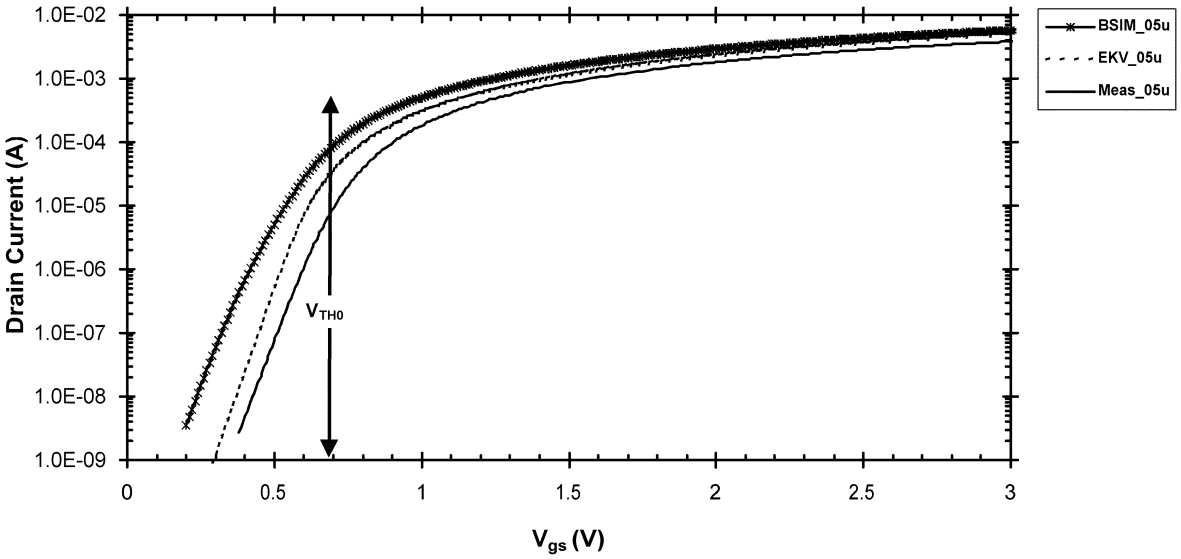


Fig. 6. $I_d$ versus $V_{gs}$ for (25/0.5) NMOS.

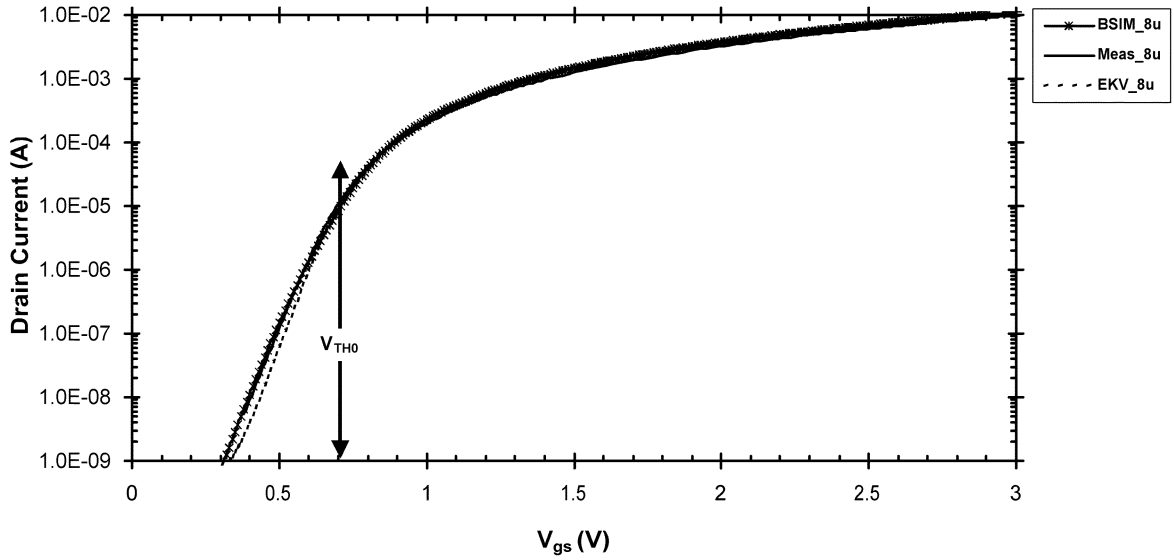


Fig. 7. $I_d$ versus $V_{gs}$ for (400/8) NMOS.

roughly the same for BSIM3V3, EKV 2.6, and measurements. However, the slope of $V_a$ in strong inversion is too large for the EKV 2.6 model, while the slope of the BSIM3V3 $V_a$ is much closer to the measurements. Considering Figs. 4 and 5 together, one can see that BSIM3V3 does a better job of predicting the *early* voltage trends. However, both models do a poor job of predicting the actual Early voltage for all but the $L = 0.5\ \mu$m case, which is a testament to the great difficulty of modeling saturated output conductance over a wide range of channel lengths and inversion levels. The output conductance errors shown by the EKV 2.6 model are mostly due to an over-simplified formulation of drain induced barrier lowering (DIBL); the new model version EKV 3.0 corrects this and shows excellent modeling of output conductance [16].

### *E. $I_d$ Versus $V_{gs}$ Simulations*

While all of the previous analysis focused on small-signal parameters, it is also important to consider the model's large-signal performance. To this end the drain current versus gate-to-source voltage was characterized for each model and measured for the test devices. Figs. 6 and 7 show a comparison of the measured and simulated $I_d$ versus $V_{gs}$ for the NMOS devices presented in Figs. 2 and 3. Fig. 6 shows quite a bit of error between simulation and measurement, especially in the weak-inversion region. This result is not surprising since this is a minimum $L$ device and, thus, the effective $L$ for the fabricated sample could be several percent off the expected $L$. Additionally, the error is worst in the weak inversion region because this region shows the greatest errors in output current for a given input voltage [17]. Fig. 7, on the other hand, shows a very good match between both models and the measurement results, with the only noticeable error in this case being that EKV slightly underestimates the drain current in deep weak inversion.

A comparison of the small- and large-signal model performances underscores the importance of inversion coefficient based design and analysis. It is important note that the data

presented in Figs. 2 and 3 are generated from the data presented in Figs. 6 and 7. However, looking at Figs. 6 and 7 alone it is not at all obvious which model will better predict the small-signal transconductance over all operating regions. In general, $g_m$-efficiency is a much more difficult test for a model because parameter extraction focuses on matching $I$-$V$ characteristics, with small-signal parameters being a secondary concern [10]. Yet in analog circuit design it is often more important to accurately predict the transconductance for a given bias current than it is to predict the $V_{gs}$ for a given bias current. As an example, consider the design of an operational amplifier whose input pair operates at the transition between weak and moderate inversion ($IC_0 = 0.1$). If the design is based on the EKV model presented here, then one could reasonably expect that for the chosen bias current, the amplifier $g_m$ (and, thus, bandwidth and noise) would be predicted very accurately. On the other hand, the only error that would result from the $I_d$ versus $V_{gs}$ characteristics of the EKV model is that, for the chosen bias current, the $V_{gs}$ of the input pair would be slightly incorrect. The result of the $V_{gs}$ error is that the simulator would miscalculate the Input Common-Mode Range (ICMR) of the amplifier, which would actually be indistinguishable from the random shift in the MOSFET threshold voltage that will be exhibited by all fabricated samples.

## V. Conclusion

This paper has presented a comparison of the dc small-signal performance of two popular MOSFET simulation models, BSIM3V3 and EKV 2.6. Detailed simulation results showing transconductance efficiency and saturated output conductance for devices with a wide range of gate lengths and operated over a wide range of channel inversion were compared to measurement results. In all simulations and measurements saturation operation was maintained by forcing $V_{gs} = V_{ds}$. The transconductance efficiency plots show that both models predicted the transconductance in deep weak inversion and throughout strong inversion correctly. However, BSIM3V3 shows an error of nearly 40% in the range $0.01 < IC_0 < 1$, while EKV 2.6 is close to ideal. Due to low-voltage operation and power efficiency concerns, many high-performance analog circuits are now operating critical devices in moderate inversion. Thus, it is very important for a designer to be aware how well their model can handle devices operated in this region.

The saturated output conductance simulations show that neither model can accurately predict output conductance over a large range of channel lengths. In the simulations presented both models agreed with measurements quite well for the $L = 0.5\ \mu\mathrm{m}$ case. This is due to the fact that most of the parameter extraction was done for minimum $L$ devices since that is what will be used in digital circuits. However, analog circuit designers routinely choose $L$ larger than the minimum to achieve high gains in OTAs, good matching in current mirrors and differential pairs, and reduced $1/f$ noise. Considering that the open loop gain of many OTA topologies is inversely proportional to an output conductance term, it is very important that an analog circuit designer read any simulation results with a good deal of skepticism.

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