CpE 271L: Digital Logic Laboratory

Final Project: Design of a Simple CPU

Fall 2023

Report Due By: 12/4/2023

Groups: Can work individually or in a maximum group size of 2.

Report: One report per group

Contents:

1. Introduction
2. Hardware Description (DE10-Lite) – What is it, pros, benefits, what is interesting about it, what is not, etc...
3. Software Description (Quartus Prime) – What does this software help you accomplish, what are its benefits, what are its downfalls, etc...
4. Description of each .VHD file
5. Problems Occurred and Solutions (**at least 2**)
6. Completed Code **(Bold/Highlighted added portions by group)**
7. Completed Finite State Machine Diagram (**find template in the ppt**)
8. Block Diagram with all Components and Connections labeled (no hand-drawn diagrams, use MS Paint/Visio) (**template in handout, expand to include all components and all individual signals/connections)**
9. Conclusion