CDA3201L

Lab #6 Sequential Circuit – Game Show Circuit

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INTRODUCTION

The purpose of this lab is to gain a deeper understanding of sequential circuit design. We designed game show circuit that can be used to determine which contestant "ring in" first to answer the question. This lab also introduces the concept of synchronous circuit design as a clock signal is required to regulate the function of the circuit.

MATERIALS

- Power Supply
- Breadboard and Wiring
- SN74LS08 4-Channel 2-Input AND
- SN74LS109 2-Channel JK Flip-Flop (Replaces Specified 74LS74)

METHODOLOGY

The circuit to be implemented has three primary operational states: idle, and win for each contestant. When the circuit is in the "idle" state (neither button is pushed or someone has already won), the outputs should be retained. When one contestant pushes their corresponding button, the circuit enters the "win" state, setting the output to the respective winner's light and rejecting all future input.

This circuit, per lab specification, is to be implemented using D Flip-Flops (DFFs), but as those are not included in the provided lab kits, that implementation has only been done in simulation. The physical circuit demonstrated relies on JK Flip-Flops (JKFFs) instead. This is achieved by allowing each JKFF to act as the "win storage" for each contestant. When reset and idle, the JKFF will be activated by the corresponding input, enabling the "win" output for that contestant and disabling the button of the other player, ensuring that state is held until the circuit is reset.

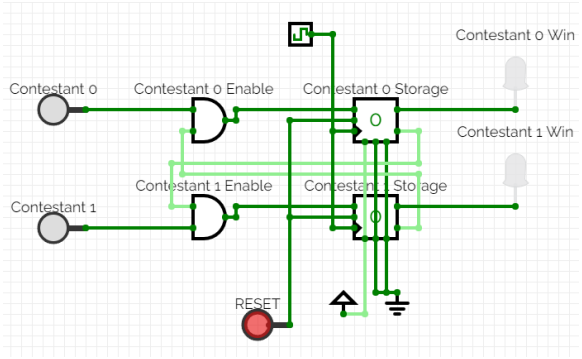

Figure 1 – JKFF Final Circuit Diagram

RESULTS

Assignment Questions

1.

Q_0*		X_1X_0			
		00	01	11	10
Q_1Q_0	00	0	1	1	0
	01	1	1	1	1
	11	1	1	1	1
	10	0	0	0	0

$Q_0^* = Q_0 + X_0Q'_1$

Q_1*		X_1X_0			
		00	01	11	10
Q_1Q_0	00	0	0	1	1
	01	0	0	0	0
	11	1	1	1	1
	10	1	1	1	1

$Q_1^* = Q_1 + X_1Q'_0$

We can substitute this into equations:
$DFF_0 = Q_0 + X_0Q'_1$
$DFF_1 = Q_1 + X_1Q'_0$
$Y_0 = Q_0$
$Y_1 = Q_1$

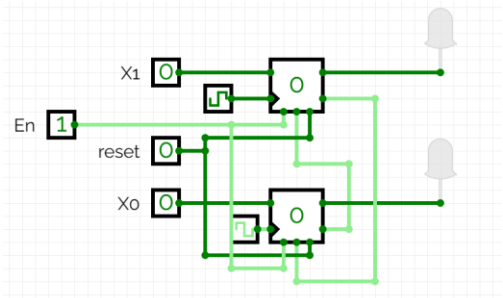

Figure 2 – DFF Final Circuit Diagram

Time	reset	x0	x1	q0	q1
00	0	0	0	0	0
05	0	1	0	1	0
10	0	1	1	1	1
15	1	1	1	0	0
20	1	0	1	0	0
25	1	0	0	0	0
30	1	1	0	0	0

Figure 3 – DFF-Based Circuit Simulation Output

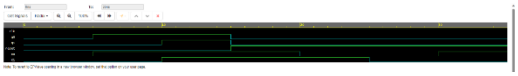

Figure 4 – DFF-Based Circuit Simulation Waveform

Full results and Verilog for this design can be found here: https://edaplayground.com/x/6as9

2.

The circuit is expected to light up LED_0 when contestant 0 wins and light up LED_1 when contestant 1 wins. Theses LEDs will remain the same state until reset is chosen. If one LED is light up, another LED cannot light up even it is clicked or not.

Experiment results

Within simulation, the circuit performed exactly as expected, with the added observation that if both contestants activate their inputs during the same clock pulse, both outputs will illuminate and remain illuminated until reset. This is not within the specification for the circuit, but is also not specified against or otherwise affecting the function of the circuit, so it was not removed. The full simulation can be found here: https://edaplayground.com/x/XMRy.

```
1  module jkff(clk, j, k, q, qbar);
2    input clk, j, k;
3    output reg q, qbar;
4
5    always@(posedge clk)
6    begin
7      if (j == 0 && k == 0)
8      begin
9        q = q;
10       qbar = qbar;
11     end
12     else if (j == 1 && k == 1)
13     begin
14       q = !q;
15       qbar = !qbar;
16     end
17     else if (j == 1)
18     begin
19       q = 1;
20       qbar = 0;
21     end
22     else if (k == 1)
23     begin
24       q = 0;
25       qbar = 1;
26     end
27   end
28 endmodule;
29
30 module gameShow(clk, a, b, res, oa, ob);
31   input clk, a, b, res;
32   output reg oa, ob;
33   wire gateda, gatedb, oan, obn;
34
35   and(gateda, a, obn);
36   and(gatedb, b, oan);
37
38   jkff(clk, gateda, res, oa, oan);
39   jkff(clk, gatedb, res, ob, obn);
40 endmodule;
```

Figure 5 – JKFF Circuit Verilog

Time	CLK	A	B	RES	OA	OB
0	0	0	0	1	x	x
10	1	0	0	1	0	0
20	0	0	0	0	0	0
30	1	0	0	0	0	0
40	0	1	0	0	0	0
50	1	1	0	0	1	0
60	0	0	0	0	1	0
70	1	0	0	0	1	0
80	0	0	1	0	1	0
90	1	0	1	0	1	0
100	0	1	1	0	1	0
110	1	1	1	0	1	0
120	0	0	0	1	1	0
130	1	0	0	1	0	0
140	0	0	1	1	0	0
150	1	0	1	1	0	1
160	0	0	0	1	0	1
170	1	0	0	1	0	0
180	0	0	0	0	0	0
190	1	0	0	0	0	0
200	0	0	0	0	0	0

Figure 6 – JKFF Circuit Simulation Output

The physical circuit matched the simulated behavior exactly, with the exception that the initial powered state of the circuit would tend to be both outputs being enabled rather than ambiguous as in the simulation.

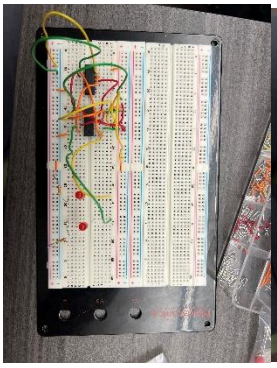

Figure 7 – Circuit: RESET

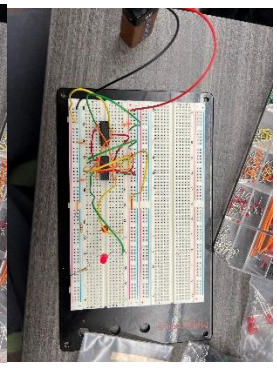

Figure 8 – Circuit: B (Out-X)

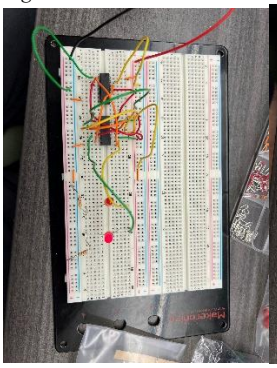

Figure 9 – Circuit: A (Out-B)

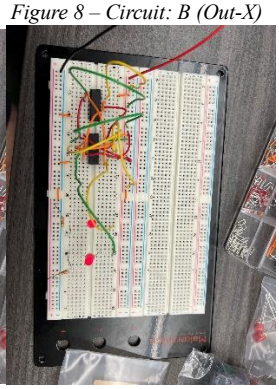

Figure 10 – Circuit: AB (Out-X)

CHALLENGES

Of note, the implemented physical circuit is synchronized with a manual clock signal as the signal from the provided function generators appeared to introduce instability, especially with developing circuits. During testing, the rapid pace of the generated clock signal resulted in an inability to recognize individual transitions during circuit testing as well as behavior which seemed outlandish, such as the standard and inverted outputs of the flip-flops to share the same value (this may also have been due to rapid oscillation causing LEDs to appear permanently enabled).

This issue was discussed with the supervising TA and the manual clock signal was deemed acceptable during demonstration.

CONCLUSION

This lab successfully provided a means for demonstrating sequential circuit design with user input and storage elements. This will serve as a foundation for larger storage operations such as bitwise data storage, counters, and more.