Department of Electrical Engineering

San Jose State University

**EE 198A Senior Project Proposal**

**Energy Management System (EMS)**

**for Storage Cells in Electric Vehicles (EVs)**

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# Executive Summary

Electric Vehicle (EV) sales have been growing at a rapid pace for the past decade. The increase in electric vehicle drivers benefits the environment as it reduces carbon dioxide emissions. The Energy Management System (EMS) for Storage Cells in EVs project is meant to combine two common systems in EVs, the inverter and Battery Management System (BMS), in a more cost effective, efficient, and modular way to make EVs more appealing to customers. The modular approach to combining the inverter and BMS includes creating a multi layer device where each layer can control its own portion of the output voltage signal. This is done to power a 3 phase DC motor. Each submodule within the layers includes a H-bridge switch that’s capable of outputting 0V, +Vout, and -Vout. The PCBs that contain the multilevel inverters are currently directly controlled by a Digital Signal Processing (DSP) controller.

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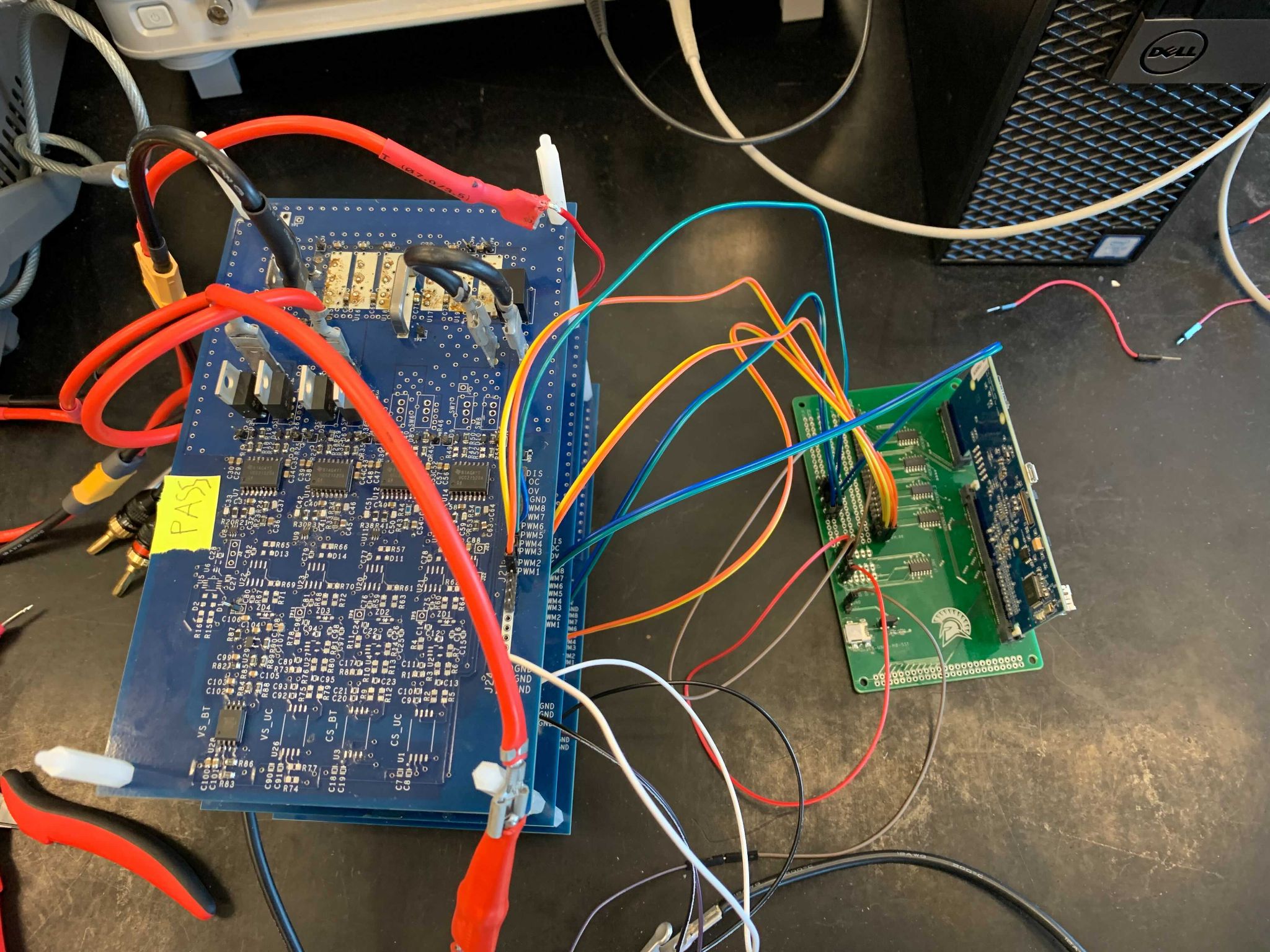
# I. Introduction

The energy management system of storage cells project tackles environmental issues and the conventional practices of the EV industry. Firstly from an environmental perspective, the EMS project contributes to decreasing carbon emissions by making EV’s more enticing to consumers. The EMS project does so by lowering the cost of the EV for the long term by decreasing the costs of maintenance of their cars. Secondly, it is predicted that the EV market will have a total share of the car industry of about 35% in 2035 [2]. Current standards for conventional design for EVs is to separate the inverter and battery management system. This results in more expensive manufacturing for EVs as well as higher cost for maintenance. So as EV sales increase, so will these same manufacturing and maintenance problems. A solution to this issue is this project where it will combine the inverter and battery management system to be one modular system. This will result in a decrease for manufacturing costs as well as lowering the difficulty and cost for maintenance.

# II. Project Overview

## A. Current Hardware System

The current hardware for the Modular Multilevel Converter (MMC) consists of a current and voltage sensor, an inverter board, gate drivers, an H-bridge circuit, and a digital signal processing (DSP) controller (Figure 1). The purpose of the sensors is to track the voltage and current levels and send them to the FPGA. If any issues were present in the MMC, the voltage or current levels would change, and using the FPGA that specific board would be shut off. The gate drivers are used to control the MOSFET’s switching times of when it turns on and off. The gate drivers act as a power amplifier, meaning that they can dissipate heat from the MOSFET and mitigate the losses in switching frequencies. The H-bridge circuit is responsible for generating the PWM signal that would be sent to the motor. The DSP controller holds the PWM modules that would be used to turn on or off the switches of the H-bridge.



### Figure 1. Current Hardware System

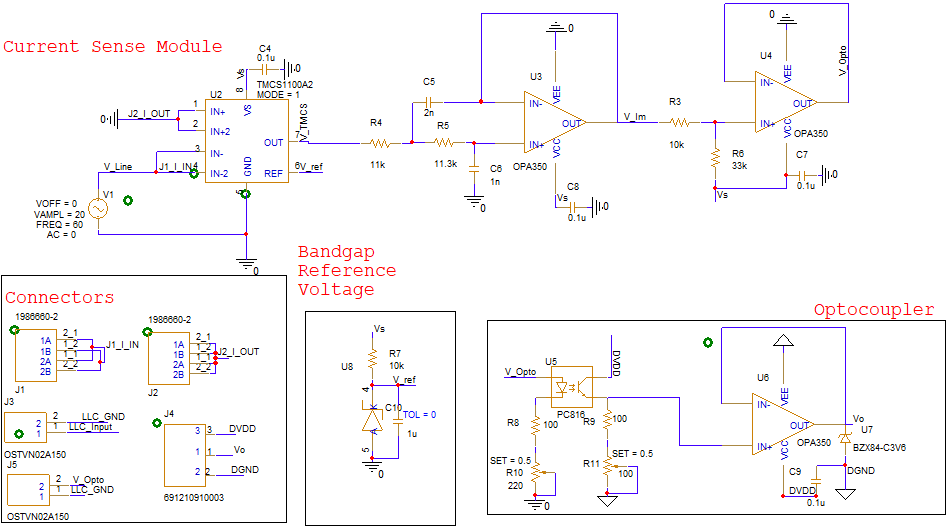
# III. Power Module Design

## A. Current Sense Schematic

Below in figure 2 and 3, is the redesigned current sense module that will be used for testing. The current sense module was redesigned to be powered by an LDO, which is powered from an external power. The old design directly powered the current sense module from the batteries, however this caused problems with the noisy reference to ground. For example, if we had two 12V batteries connected in series, the measured voltage would be 24V. If we took the voltage measurement of the second battery, from an overview perspective, we would see 12V and so would the system. However, the 12V seen by the system would be noisy because it is not referenced to ground. The measured 12V would be the voltage difference between 24V and 12V, instead of 12V to 0V, which is measured with respect to ground. By adding the LDO and using an auxiliary power, we can eliminate the noisy reference and measure the voltage with respect to ground.



### Figure 2. LDO used to power Current Sense Module

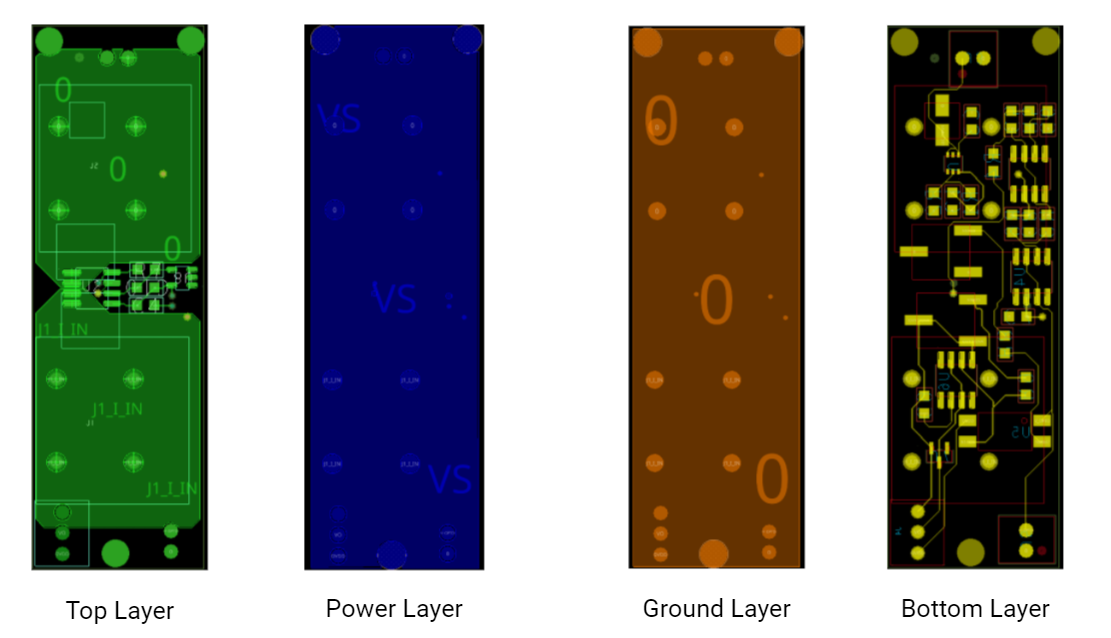


### Figure 3. Current Sense Module

The new current sense module uses the TMCS1100A2, which is a galvanically isolated Hall effect current sensor that is capable of DC or AC current measurement with high accuracy, excellent linearity, and temperature stability [3]. Following the TMCS1100A2 is a low pass filter using the OPA350 OPAMP to filter higher frequencies because we are working in the frequency range of 60Hz to 12kHZ. After the low pass filter, the signal is fed into a buffer amplifier to preserve the signal source. Following the output from the buffer, the signal is fed into an optocoupler to isolate the analog signal and ground from the digital signal and ground. The working principle of the optocoupler is when a current is applied to the input. An infrared LED emits a light that is proportional to the current and activates the photosensitive device on the other side. The optocoupler is another way to provide isolation between circuits. Finally, the signal is fed into another buffer to provide additional protection from any interference, and a Zener diode is added at the output to clamp the voltage to 3.3V, to protect the ADC of the FPGA.

## B. Printed Circuit Board (PCB)

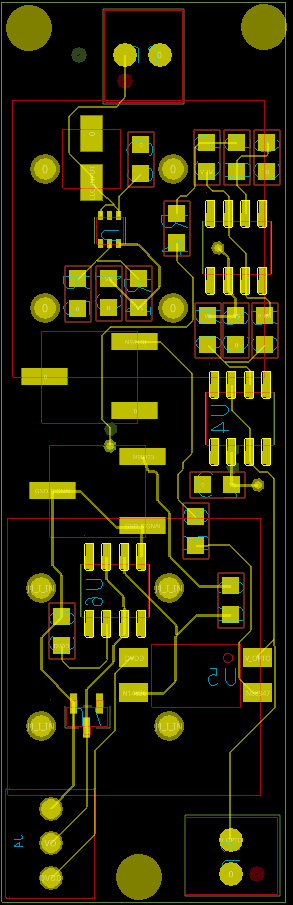
One of the major design tasks that will be completed in the summer of 2021 is creating a PCB for the current sense schematic. Two PCB design rules that were followed are design constraints from the PCB manufacturer and for incoming high current. When designing a PCB, it is important to pay attention to the capabilities of the chosen PCB manufacturer. Usually the PCB manufacturer will provide a constraint file that auto generates constraints into your PCB software. The project advisor had chosen Bay Area circuits as this project’s PCB manufacturer. Unfortunately, Bay Area circuits does not provide a constraint file for this project’s chosen PCB software, which is OrCAD PCB Editor. A necessary step that had to be taken in order to produce a PCB was to learn how to transfer the constraints from Bay Area Circuits capabilities page into OrCAD manually. Another design constraint that had to be followed is designing for high current. One of the main points for designing a PCB that will be used for high currents is ensuring that the current contacts are large enough to handle the high amounts of current. This includes creating a large polygon pour where the software PCB tool kit version 8.05 by Saturn PCB was used in this project’s case to determine the dimensions of the polygon pours. The size of the polygon pours with respect to the components can be seen in the figure below.



### Figure 4. 4 Layers of the Current Sense PCB

The current sense PCB is made up of a total of four layers. The top layer includes the polygon pours as well as a few of the components in the current sense schematic. The second layer down is the power layer. The power layer is receiving it’s a voltage from the LDO which is located on the bottom layer. The third layer down is the ground plane used for the analog side and to reduce interference from the top layer and bottom layer . Lastly, the bottom layer is where most of the components from the current sense schematic are located.

Generally, industry standard PCB design rules were followed during the construction of the current sense PCB. Another example of a general, industry standard PCB design rule is placing components that are on the incoming side for ICs close to the input pins while keeping components on the output side farther away. A larger image of the bottom layer can be found in the figure below:

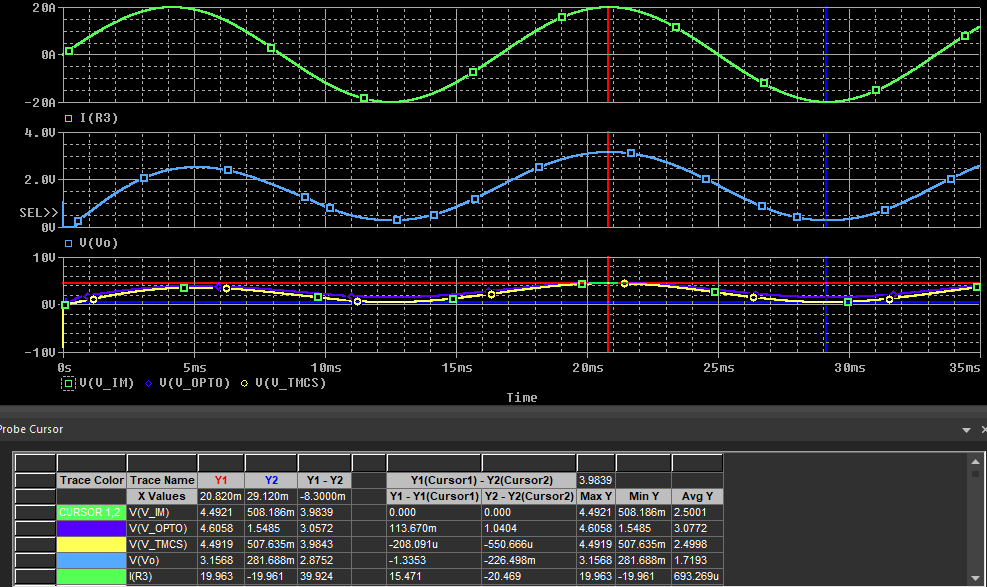


### Figure 5. Closer Look at the Bottom Layer

Another constraint to keep in mind for PCB designing is available components on the market as well as the project’s budget. To stay within the given budget, most of the connectors selected are through hole type. This posed some design obstacles as the rest of the components had to be placed in a way in order to avoid the through-hole pins. Pragmatically, there’s going to be sacrifices made for placing components with respect to industry standards due to component selection but this is a reality PCB design engineers must learn how to work around.

The PMD team learned about how to transfer schematic files from OrCad Capture into OrCad PCB Editor. Polygon pour calculators such as the PCB toolkit V8.05 by Saturn PCB was used and it taught how to create appropriately sized contacts for specific requirements such as temperature change, copper weight, and amperage. The PMD team also learned how to use OrCad Padstack editor in order to create custom footprints for components whose footprints are not readily available. In the end, a current sense PCB about the size of a thumb drive that can handle up to 20A was created.

## C. Simulation Results

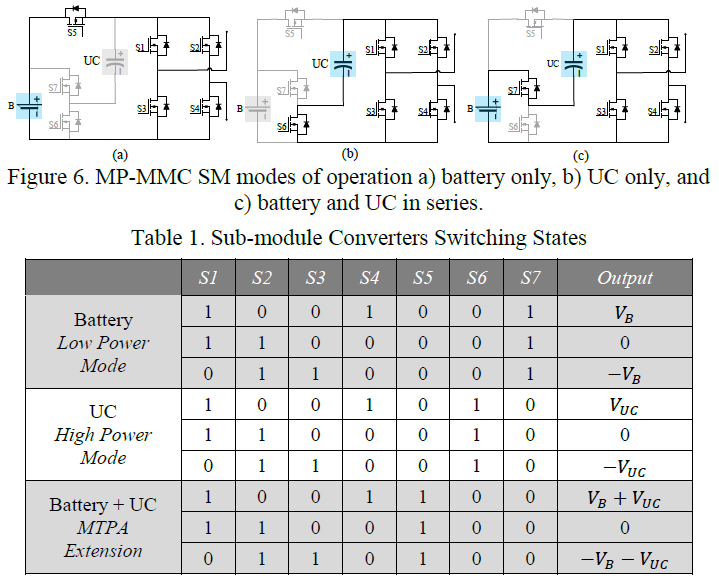


### Figure 6. Output Waveforms

# IV. Embedded Systems (ES)

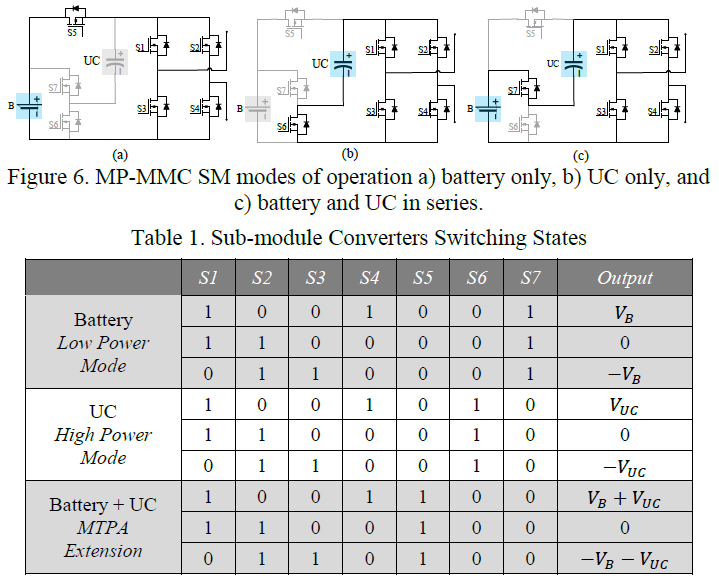
## A. DSP PWM Signals

In order to provide the PWM signals for the H bridge shown in Figure 8, switches 1 - 4, a Texas Instruments C2000 DSP controller was programmed. Given our current hardware setup only includes batteries within the submodules, switches 1 - 4 are the only switches needed, meaning that switches 5 - 7 can be removed. Given that configuration a) in Figure 8, is the only possible mode of operation, this means that “Battery Low Power Mode” is the only section that was focused on when designing the code (Table 1).

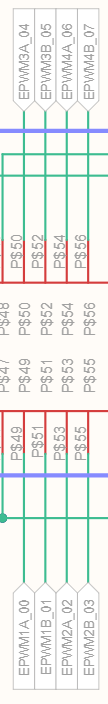


### Figure 7. MP-MMC SM modes a) battery, b) UC, and c) battery and UC in series

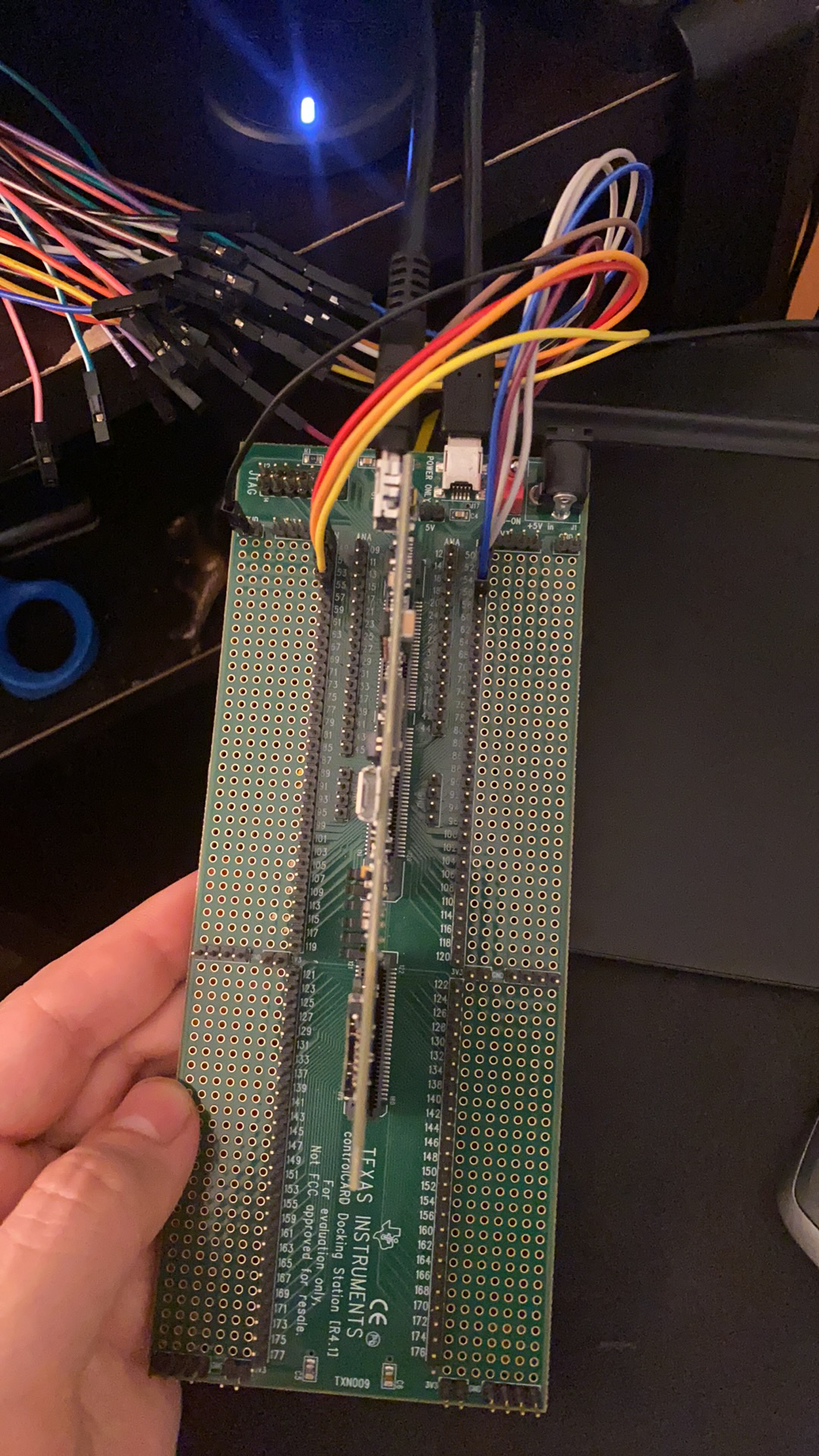
### Table 1. Sub-module Converters Switching States



The current code utilizes PWM modules 1 - 4 which each contain a pair of PWM channels, a low and high frequency channel, which makes for a total of 8 output channels (Figure 9). The green board that the DSP interfaces with in Figure 10 is probed for testing with Analog Devices’ ADALM2000, operating as a Logic Analyzer. These outputs will be discussed later in Subsection C.



### Figure 8. Schematic to locate the PWM modules used for testing



### Figure 9. DSP board with test board, probed by the ADALM2000’s Logic Analyzer

## B. Adapted Sorting Algorithm

In order to test the current hardware system, the algorithm from Professor Badawy’s paper [1] needed to be simplified, in order to accommodate the lack of UCs. Anything in the algorithm that included any purpose behind additional modes of operations regarding the UCs was removed while the test code was written. In order to update the PWM modules in an organized fashion, a PWM module matrix is made which includes that status of each of the four switches for each H bridge. The printed matrix manipulations of the test code can be seen in Figures 10 - 11.

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### Figure 10. Creating and sorting the main matrix based on SOC

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### Figure 11. Evaluating the PWM modules with highest SOC and updating main matrix

## C. PWM Output Results

After the test code was written to verify the logic of the algorithm, it was then implemented into the main code to generate the output shown in Figures 14 -15. Figure 12 - 13 show outputs of two different configurations of the previous code.

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### Figure 12. PWM Output without any sorting

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### Figure 13. PWM Output with SORT\_LEVELS enabled

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### Figure 14. PWM Output with SOC\_sort\_algo enabled (zoomed out)

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### Figure 15. PWM Output with SOC\_sort\_algo enabled (zoomed in)

# V. Work Schedule

### Table 2.



The ES team will continue working on the implementation of the SOC sorting algorithm and will test it on the current hardware system. After this is complete, the SOC algorithm will need to be written to utilize the new current sensing hardware, for active balancing.

The PMD team will be finishing up the current sense PCB. This includes slightly adjusting the polygon pours to make more room for the top layer components, switching the blind vias to through hole vias, and adding the digital ground and ground planes around the PCB. Hiromi will work on remaking the custom footprints and vias in order to increase the width of the silk screen lines. Andrew will learn about Ansys for when the times come to perform thermal, power, and electromagnetic analysis on the system PCB.

# VI. Conclusion

As mentioned previously, the sales of EVs are projected to increase as time goes on, but the cost of purchasing an electric vehicle does not seem to be reducing anytime soon. In order to solve this issue, our team is dedicated to designing and developing the Multilevel Modular Converter for Energy Management Systems in electric vehicles. For the next semester, the PMD team will put more emphasis on testing the newly designed MMC board and modules. ES will focus on implementing the SOC sorting algorithm and selecting an FPGA for further testing.

# References

[1] S. S. George and M. O. Badawy, A Modular Multi-Level Converter for Energy Management of Hybrid Storage System in Electric Vehicles, 2018 IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, CA, USA, 2018, pp. 336-341, doi: 10.1109/ITEC.2018.8450237. Available at: <<https://ieeexplore.ieee.org/abstract/document/8450237>> [Accessed 8 May 2021].

[2] T. Randall, "Here’s How Electric Cars Will Cause the Next Oil Crisis", Bloomberg.com, 2016. [Online]. Available: <<https://www.bloomberg.com/features/2016-ev-oil-crisis/>> [Accessed: 08 May 2021].

[3] Texas Instruments, “TMCS1100 1% High-Precision, Basic Isolation Hall-Effect Current Sensor With ±600-V Working Voltage,” SBOS820A datasheet, Sept. 2019

[Revised Jun 2020].