Revision Date: July 05, 2020

SAN JOSE STATE UNIVERSITY

ELECTRICAL ENGINEERING DEPARTMENT

EE122 LAB MANUAL

SAN JOSE STATE UNIVERSITY

ELECTRICAL ENGINEERING DEPARTMENT

Getting started with the practical design fabrication and testing of analog circuits and systems

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Chapter 3:
Solar Cell Modeling and Applications

Week 3

There is no lab report due for this chapter. There are five check points that the TA will mark off as you go along.

Solar Cell Modeling

A great introduction to solar cells can be found here:

Terms

- I_{load} is the photo generated current.
- I_{sc} is the current the cell produces at zero bias.
- R_s is the series resistance of the solar cell.
- I_s is reverse saturation current of a diode.
- n is the ideality factor of a diode usually between 1-2.
- V_{oc} is open circuit voltage of a solar cell.
- V_{th} is the thermal voltage (KT/q = 26mV) at room temperature.

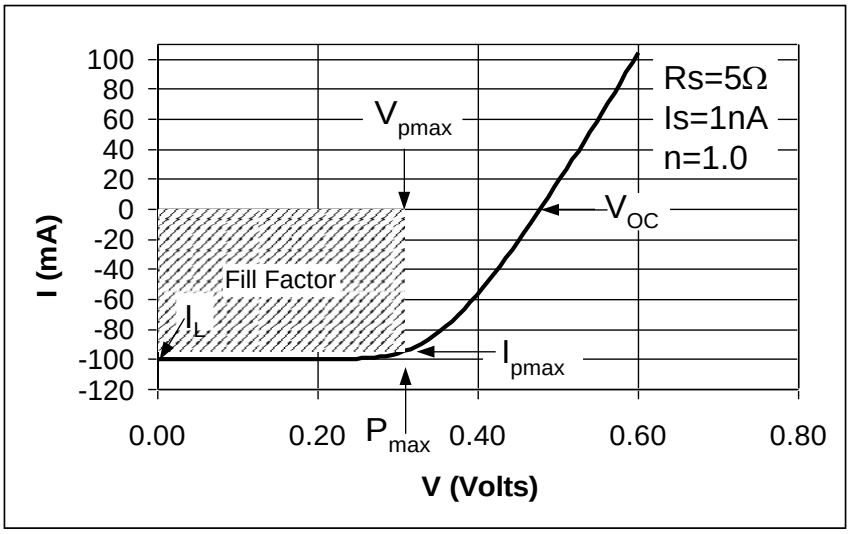

Figure 43: IV response of a solar cell with series resistance showing IL, Voc, Pmax, and FF generated from equation 1 after [5].

Solar Cell Modeling

Looking at the I-V equation for a solar cell under illumination (equation 1.) [5], it can be seen that the only optical parameter that needs to be measured is I_L and that the diode parameters could be extracted from a purely electrical simulation. I_s is the reverse saturation current, n is the ideality factor, V_{th} is the thermal voltage, and Rs is the series resistance of the diode (solar cell). Equation (1) assumes that there is no shunt conductance across the solar cell.

$$I = I_s\left(\exp\left[\frac{V - IR_s}{nV_{th}}\right] - 1\right) - I_L \qquad (1)$$

The load current (I_L), otherwise known as the short circuit current can be found by setting the voltage to zero (short circuit) and then measuring the current under illumination. I_s, n, and R_s can then be found by a purely electrical simulation.

Once I_L, I_s, n, and R_s have been determined, the open circuit voltage (V_{oc}), maximum power (P_{max}), and fill factor (FF) can be found.

V_{oc} is found be setting I from equation 1 to zero and solving for the resulting voltage.

$$V_{oc} = nV_{th} \ln\left(\frac{I_L}{I_s}\right) \qquad (2)$$

Equation (3) represents the power extracted from a solar cell. To find the maximum point, the derivative of the power is taken with respect to current and the current that satisfies equation (4) is the current at the maxim power point (Figure 43).

$$P = IV = I\left[nV_{th}\ln\left(\frac{I + I_L}{I_s} + 1\right) + IR_s\right] \qquad (3)$$

$$nV_{th}\ln\left(\frac{I_{pmax} + I_L}{I_s} + 1\right) + \frac{nV_{th}I_{pmax}}{I_{pmax} + I_L + I_o} + 2R_s = 0 \qquad (4)$$

The maximum power is then easily calculated by substituting Imax into equation (3). The fill factor is then calculated according to equation (6).

$$P_{max} = I_{pmax}\left[nV_{th} \ln\left(\frac{I_{pmax} + I_L}{I_s} + 1 \right) + I_{pmax} R_s \right] \quad (5)$$

$$FF = \frac{P_{max}}{I_L V_{oc}} \quad (6)$$

While equations (1-6) show that it is possible to decouple the optical and electrical simulation of a solar cell, the extraction of n, I_s, n, and R_s needs to be accurate and automated for this technique to be useful in the characterization of solar cells.

To extract n and I_s using the simple method the natural log of the current is plotted vs. the applied voltage (Figure 44). A linear range is selected, and a linear regression is performed. The results are of the form y=Ax+B. The ideality factor n is given by equation (7), while the reverse saturation current is given by equation (8).

$$n = \frac{1}{V_{th} A} \quad (7)$$

$$I_s = \exp(B) \quad (8)$$

R_s is found by finding the linear range of the current vs. voltage plot (Figure 44) and performing a linear regression to extract the slope. Rs is given by:

$$R_s = 1/A \quad (9)$$

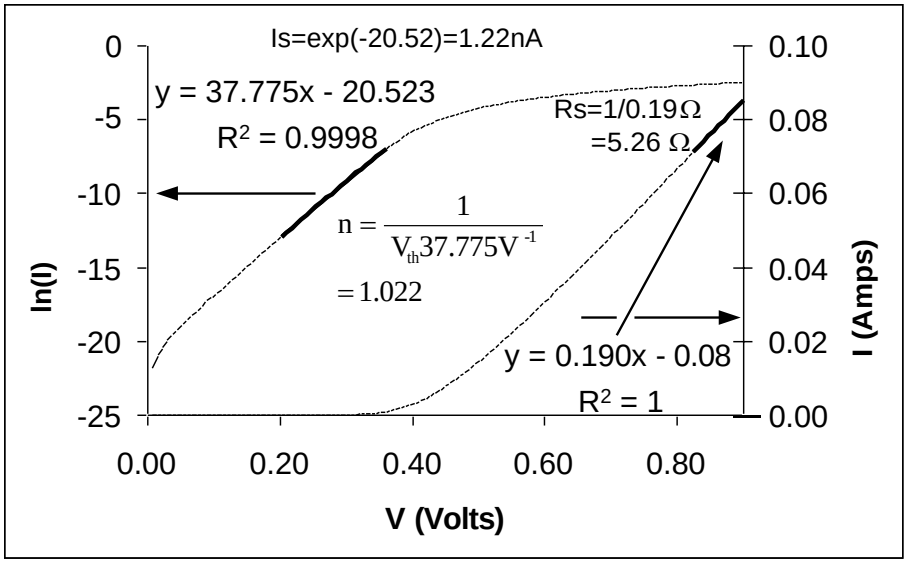

Figure 44: Simple extraction methodology plot for a diode with an IV characteristic generated from equation 1.

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Energy Harvesting

A great article on energy harvesting can be found here. If this link does not work then use this link.

Lab Activities

Modeling a solar cell in LTspice:

- Build the solar cell model shown in Figure 45. It can be downloaded from here:

- Run the file. You should see a blank area open up as is Figure 46.

- Plot V(out) and I(R_s). You should see Figure 47.

- Change the X-axis to V(out). You should see Figure 48.

- Plot the power as V(out)× I(rs) (Figure 49).

******TA Checkpoint A******

- Stepping R_{load} is a method to measure the IV characteristics of solar cell, but it is extremely time consuming to do and it does not lend itself to automation. It can also be hard to extract R_s. It a real test lab an SMU voltage source measurement unit is used. The voltage is swept and the current measured. This is modeled in LTspice as in Figure 50.

- Change your model to match Figure 50, and rerun the simulation, and re-extract V_{oc}, I_{sc} and maximum power (Figure 51, Figure 52).

******TA Checkpoint B******

- Create a solar cell model in LTspice with R_s=0.5 ohm, R_{shunt}=50k ohm, I_s=10nA, I_{load}=-400mA, and n=1.2, at room temperature.

- What is the V_{oc} and maximum power?

- If R_s=2ohm, what is the V_{oc} and maximum power?

******TA Checkpoint C******

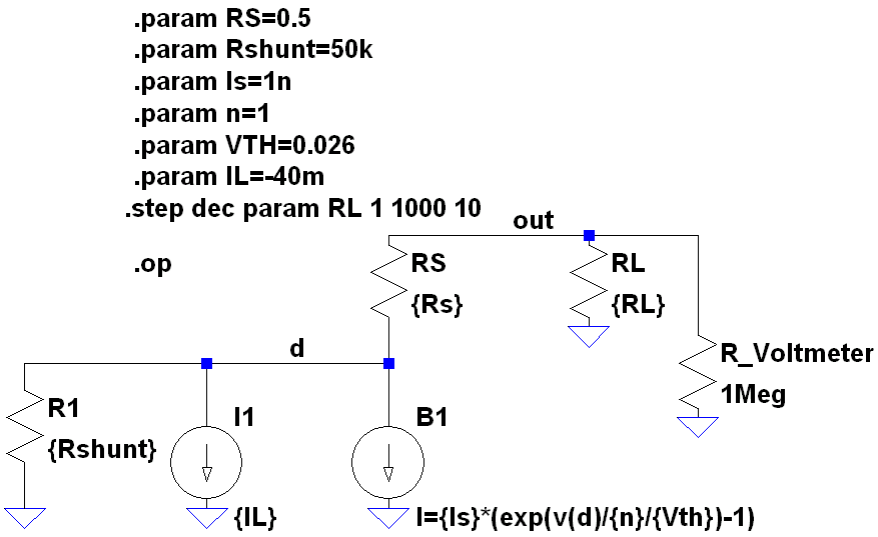


Figure 45: Solar Cell Model with programmable parameters.

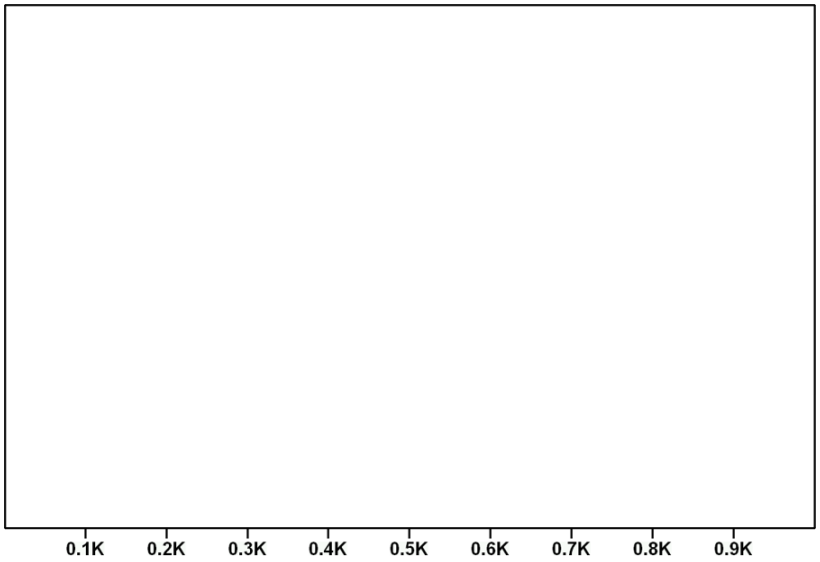


Figure 46: Simulation results without data.

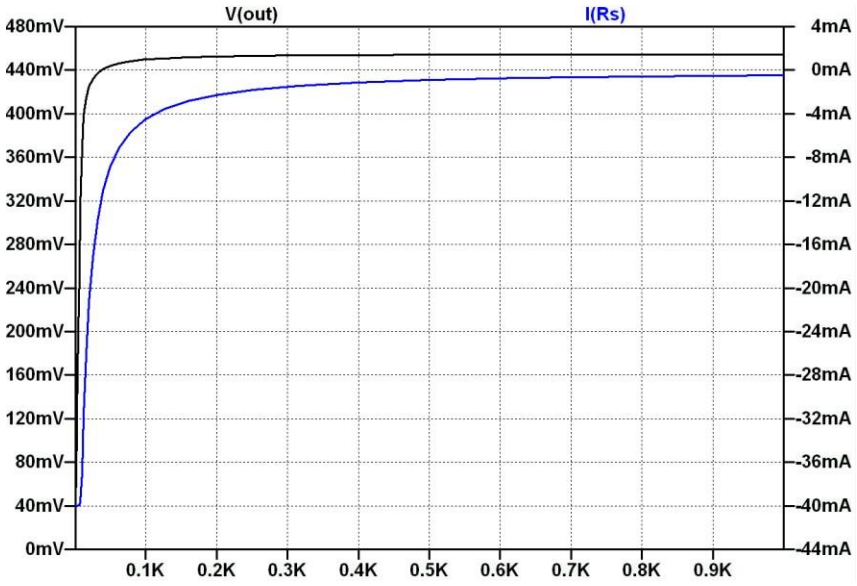


Figure 47: Simulation results of Vout and I(rs) vs Rload.

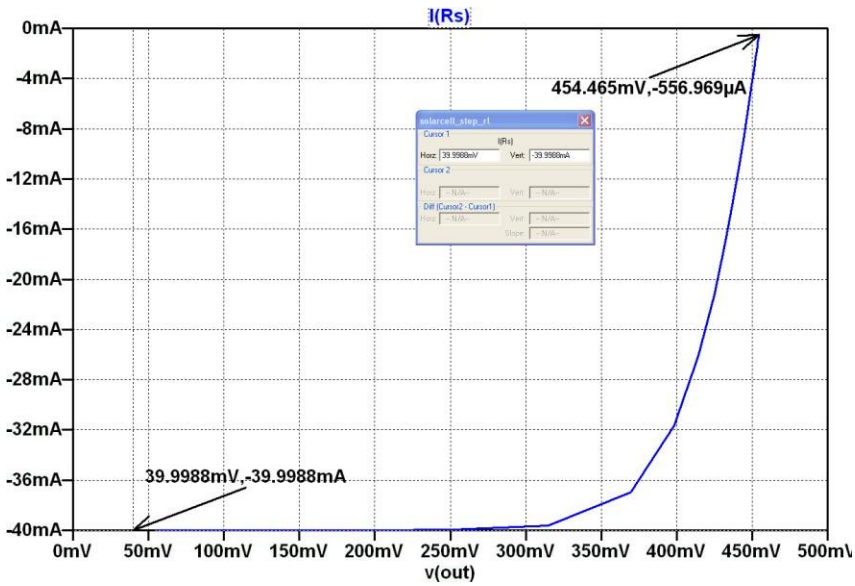


Figure 48: Finding V_{oc} and $I_{sc.}$

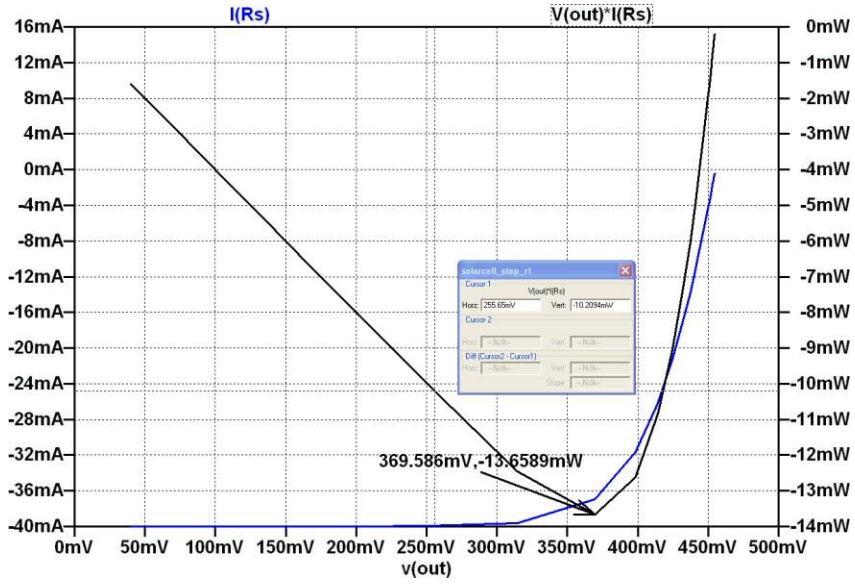


Figure 49: Finding maximum available power.

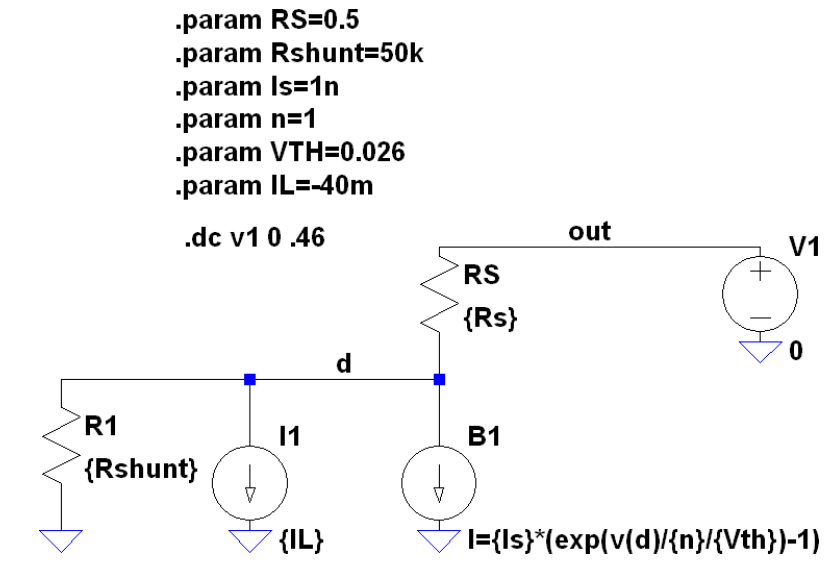


Figure 50: Measuring solar cell response with a voltage source.

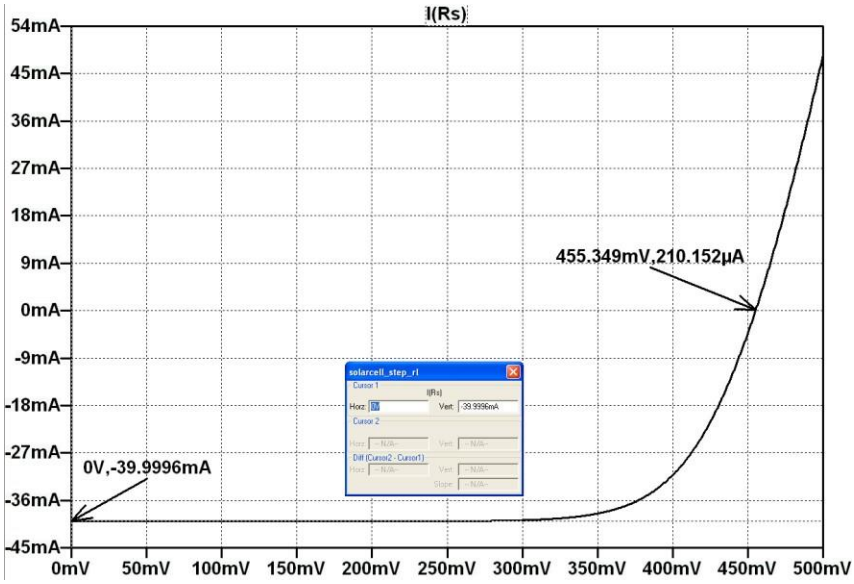


Figure 51: Measuring V_{oc} and I_{sc} from a swept voltage source.

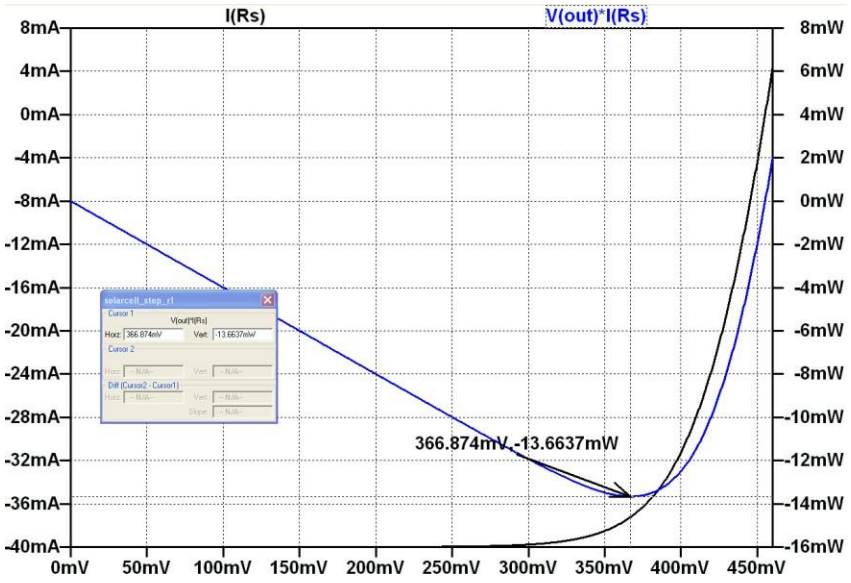


Figure 52: Finding power from a swept voltage source.

Energy Harvesting:

- Open up the LTC3105 test jig in LTspice (Figure 53). (You can create a new schematic, add a new part, and place the LTC3105 (located in power products). Then you can right click on the part and open up the test jig.)

- Run the simulation (Figure 54). (It takes a while.)

******TA Checkpoint D******

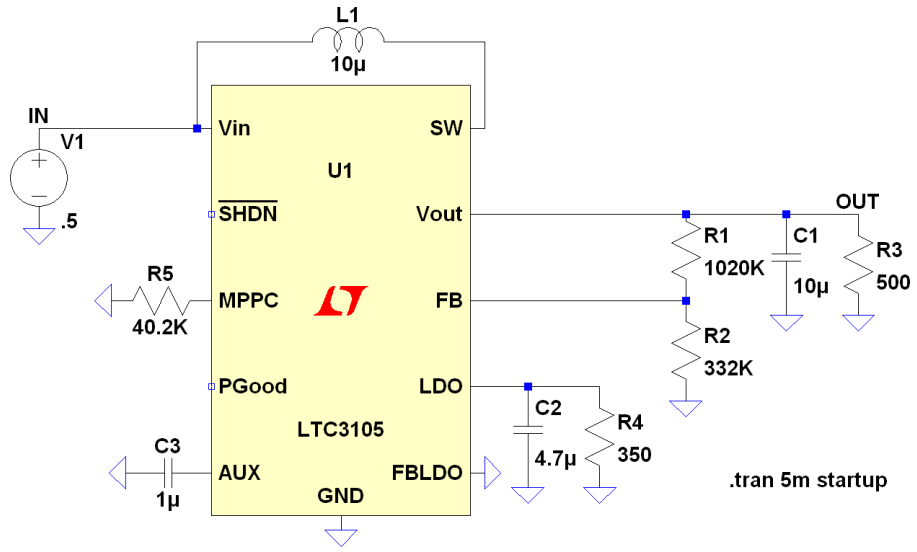


Figure 53: LTC3105 Test Jig.

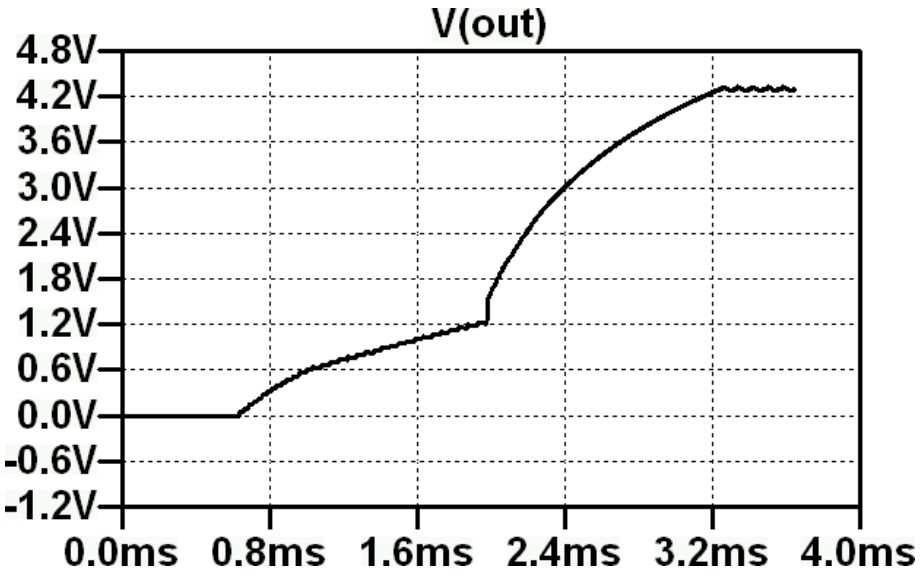


Figure 54: Transient response of LTC3105.

Design an energy harvesting system using the LTC3105 and two solar cells in parallel that have the following electrical characteristics: R_s=0.5 ohm, R_{shunt}=50k ohm, I_s=10nA, I_{load}=- 200mA, and n=1.2, at room temperature to charge a cell phone with a USB. Use the solar cell model you developed in the previous section. You have to research the specification for this. In addition, the design equations are in the LTC3105 Datasheet. (http://www.linear.com/product/LTC3105)

In order to get the simulation to run properly with the behavioral solar cell you have to add a capacitor to V(in) as shown in Figure 55. Also you have to add an initial condition, .ic V(d)=0, and .ic V(In)=0 to the schematic to get the simulation to start properly (Figure 56).

******TA Checkpoint E******

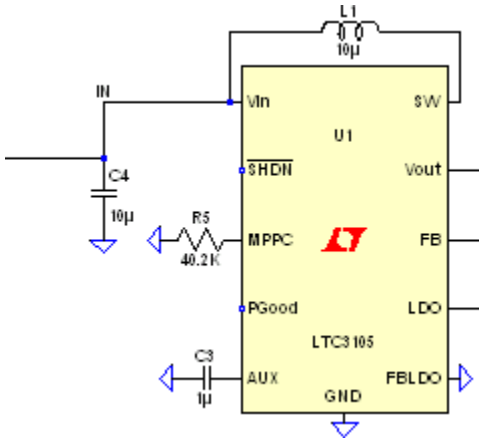


Figure 55: Add a 10uF capacitor to the In node (Vin port on the LTC3105) to make the simulation run properly.

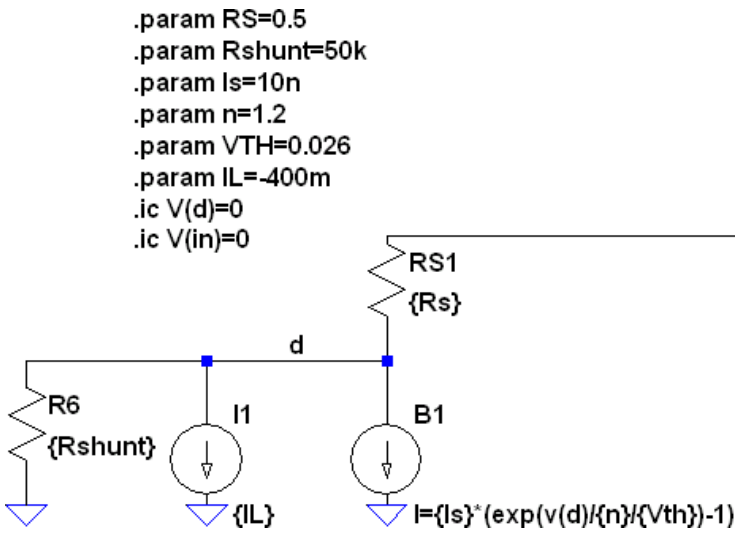


Figure 56: Add initial conditions to schematic.

Lab report:

NA: Show results for check pints A, B, C, D, and E to your TA as you do the lab.

Chapter 4:
Energy Harvesting PCB Design

Week 4

Pre-lab:

- Before starting your design, read the data sheet and highlights all the PCB layout tips.
- Watch these videos:
  - Video on making sure your board as the right layers:
  - Video on PCB hints
  - LTC3105 video
  - Video on past projects

Lab Activity:

You will design your PCB board in diptrace the TA will check your design before you turn it in. There is no lab report due, just the diptrace files.s

- Using Diptrace, design a single layer board that will create a 5V power supply:
  - Try to use the parts that are already created. For the LTC3105, USB, R's and C's use the pre-drawn packages. You have to make your own drawing for the solar cells, and the inductor.
    - Inductor Note: The inductor pad size should be 0.08 inches x 0.08 inches, the distance between the pads should be 0.2 inches from the middle of both pads and 0.12 inches edge to edge between the pads. The data sheet for the inductor can be found here.
  - Mount both solar cells in parallel Make one copper pad 2" by 2" (Figure 58, Figure 59).

(You might get one solar cell that is 2” by 2”.)

- Everything must be in the TOP layer. (Do not use Top Assy.)
    - If you accidentally put something in Top Assy, select the object, and change the layer type to signal.
- Place a + and – sign near your positive and ground signals in copper (Top)
- Place a mark in copper to show you the top of your IC (LT3105)
- Put your name in the copper layer away from the parts.
    - Use the TOP or signal Layer, not Silk!
    - Use the vector option for your text.
- Use surface mount parts from Figure 57. This is done so that we can buy the parts for every project in an efficient manner. Note you might not need all of them. You really need to choose the R values to set the voltage properly at the 5.0V side. The other outputs we do not need.
- Use the 12 pin MSOP package. Another link can be found here. https://dl.dropboxusercontent.com/u/35091424/EE122/05081668_A_MS12.pdf
    - In Diptrace, trace search for the pattern in layout as MSOP. A list of choices will appear,
- Your design must fit in a 3” by 2.5” area.
- You must add a board outline using the Objects, Place objects, board outline tool. You check and see if the board outline was done properly, turn the board outline layer on and off, and you should see it disappear and reappear.
- The output is USB and you need to use this SMT part: http://www.sparkfun.com/datasheets/Prototyping/Connectors/USBFemaleTy peA.pdf
- The holes shown in the USB, are not important because we do not use them. Pins 5 and 6 are just solder pads to hold the USB down.
- Pins 1-4 can be connected as shown at the bottom of:
    - http://en.wikipedia.org/wiki/USB

- Make sure your power and ground lines are wide enough. Current flowing through a thin wire can cause a large resistive loss.
- Make sure that you do not include the output resistor load that you used to see if your project works. The load will be the phone.

- The inductor part has changed. The data sheet for the correct inductor can be found here.

Table 1: BOM for 5V design.

Item	Qty	Reference	Description
1	1	L1	10uH inductor
2	2	C1, C2	10 uF capacitor (size 0805)
3	1	C3	1uH capacitor (size 0805)
4	1	R1	1MegΩ 1% (size 0402)
5	1	R2	250kΩ 1% (size 0402)
6	1	R5	40.2kΩ 1% (size 0402)

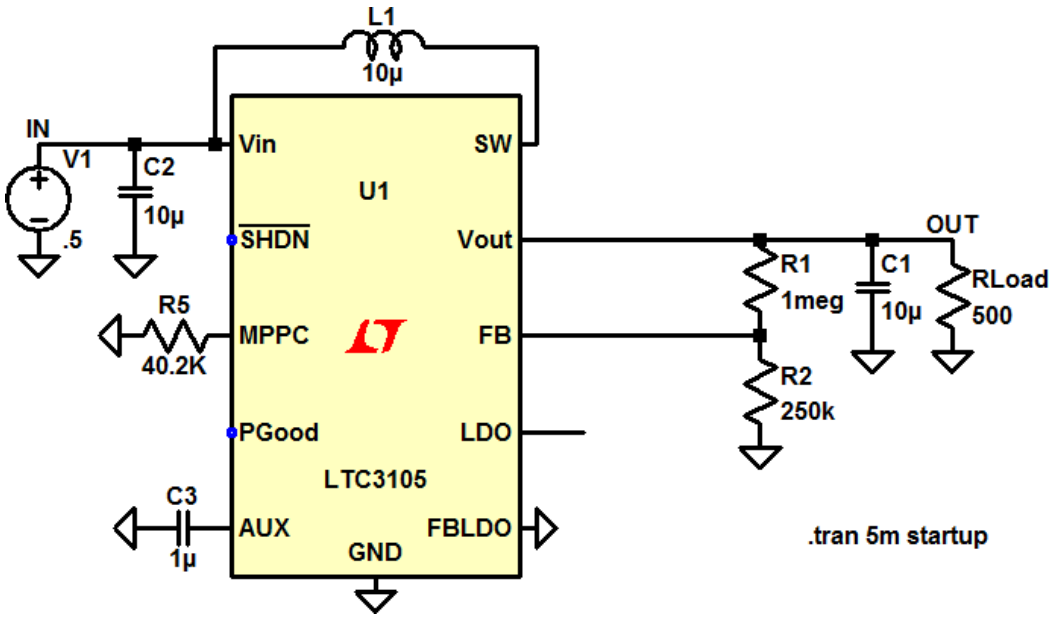


Figure 57: Reference schematic for 5-volt design. Note: R_{load} simulates a 10mA load (5V/500Ω) Note: LDO not connected on purpose.

Link to above schematic:

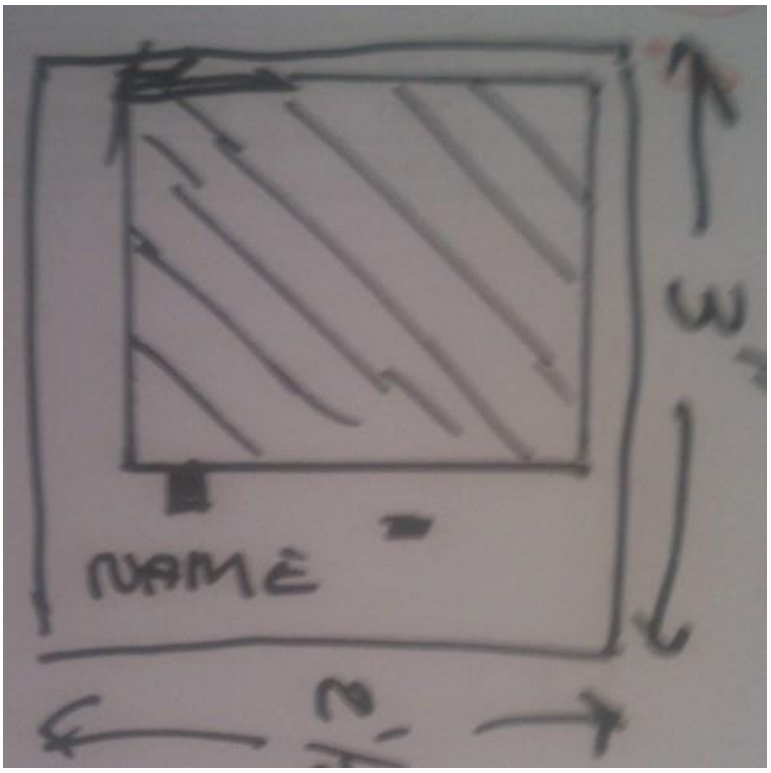


Figure 58: Very rough drawing of footprint of solar cell.

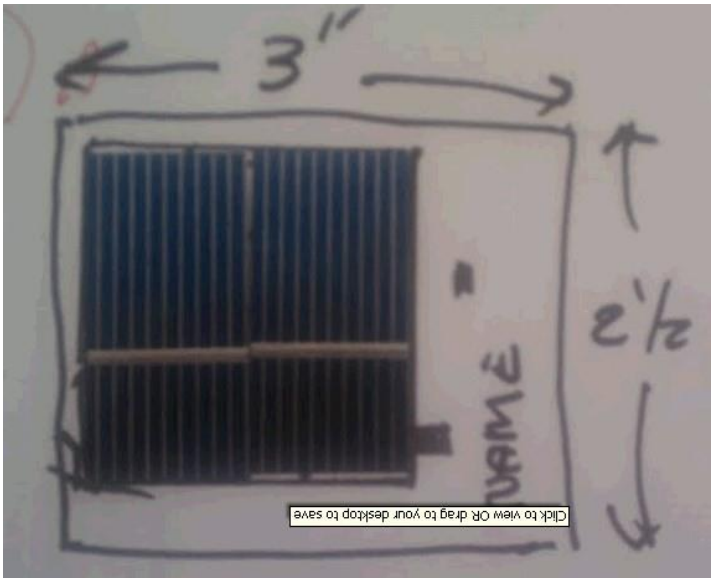


Figure 59: Very rough draft of board with solar cells. The top of the cell is negative, and the bottom is positive. Connect the negative side of the solar cells together with a wire, that then connects to the negative trace on your board.

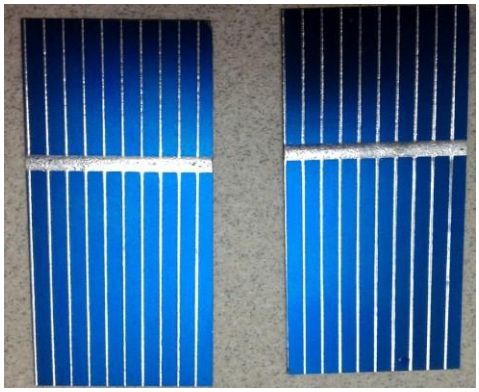


Figure 60: Cells you can use for your energy harvesting circuit. (Your solar cell might be one piece.

The top metal grid is the negative side of the solar cell (-). The bottom of the solar cell is positive (+). You will solder a piece of wire from the top of the solar cell to ground on the board.

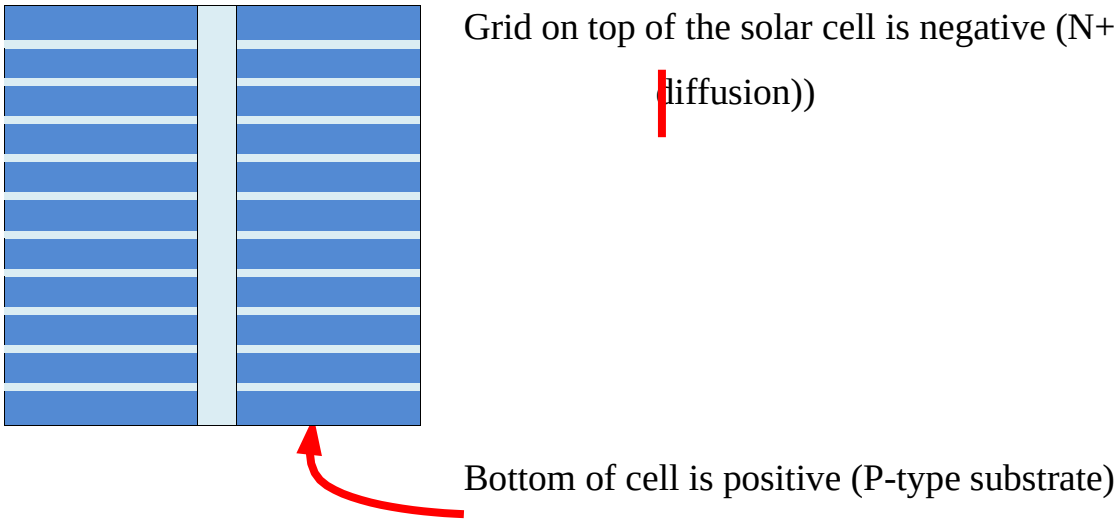


Figure 61: Positive and negative are labeled for solar cells.

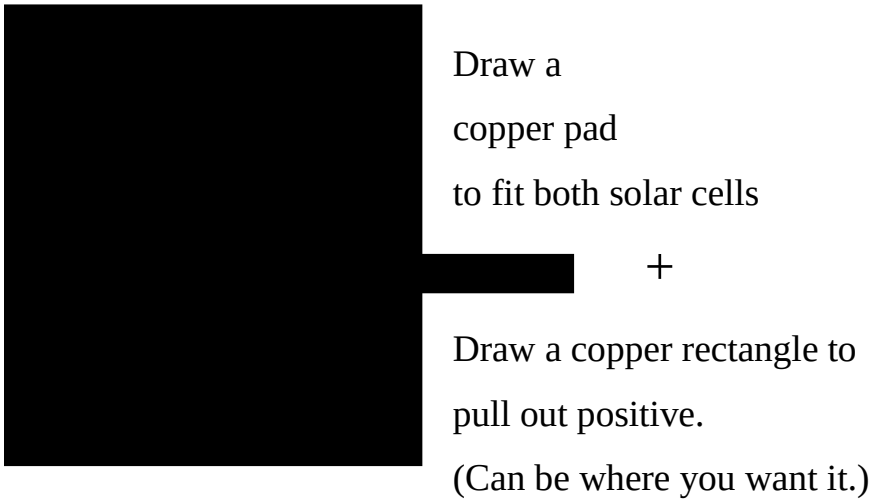


Figure 62: Draw pad for solar cells.

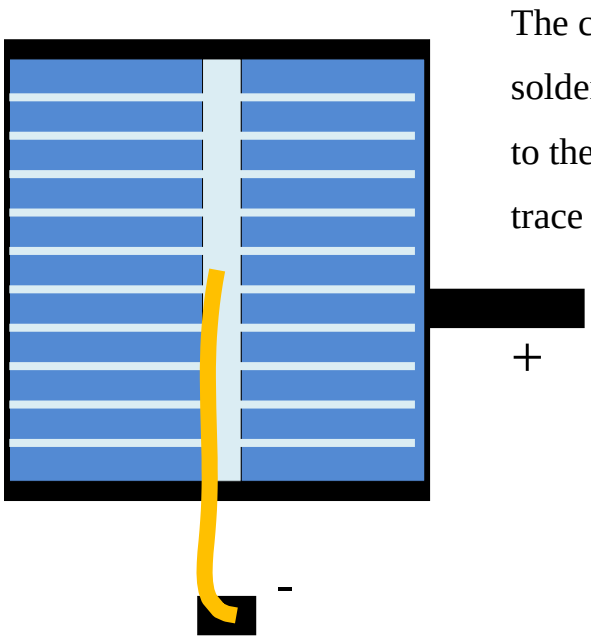


Figure 63: Hint on how to add solar cell to board. (Note: There is only one cell shown here.)

Lab Report / Dip Trace Files:

Watch this video, on how to double check your board for common mistakes: https://youtu.be/EMTmq4vKMJ0

- Turn the diptrace file in on Canvas. Make sure the file is named: Lastname1_solar_charger.dip
- Make sure that everything is in the TOP layer, and that the board outline was created with the objects, place board outline tool, and that the board outline is in the board outline layer.
- When the board comes back you will assemble it, test it, and document your design.

Chapter 6:
Energy Harvesting PCB assembly and test - Presentation

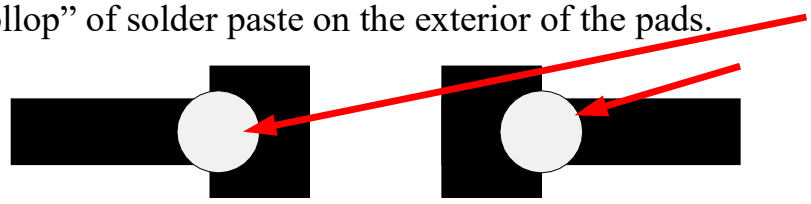
Weeks 6

Introduction:

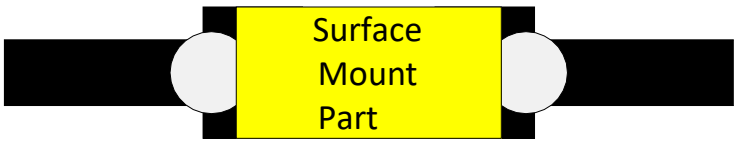
This lab is an extension of the DipTrace lab where you designed the PCB layout and now in this lab there will be a presentation on the PCB assembly and testing. The lab will consist of training how to use the surface mount soldering stations, followed by introducing you to the components and equipment we will be using, if doing fabrication/assembly. Basic information on the Energy Harvesting PCB assembly and testing:

Attaching surface mount parts:

Add “dollop” of solder paste on the exterior of the pads.



Place surface mount part so it slightly touches paste.



Lab Report:

There will be no lab report due for this week.

APPENDIX:

(Additional Information on Soldering)

Energy Harvesting PCB assembly and test

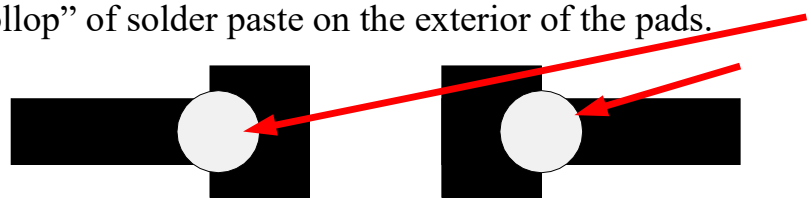
Introduction:

This lab is an extension of the DipTrace lab where you designed the PCB layout and now, the same will be used for further assembling and testing using soldering tools. All the required equipment and tools will be provided to you prior to the start of the session. This lab will be guided by the soldering experts and the TAs will help you to complete the lab. There will be a small presentation at the start of the lab session.

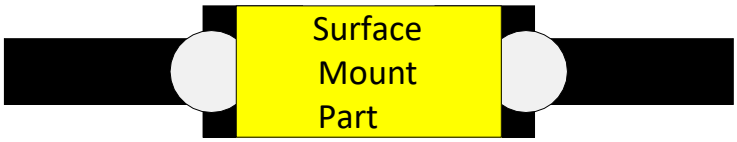
The lab will consist of training how to use the surface mount soldering stations, followed by you assembling your PCB, and ending with the testing of your design. An example of an application note is the actual design note for the LTC 3105 that we used for our design.

Attaching surface mount parts:

Add “dollop” of solder paste on the exterior of the pads.



Place surface mount part so it slightly touches paste.



BILLS OF MATERIALS:

1. Inductors:	
10 uH - For Soldering	**10 uH (Note the inductor looks like a resistor)**
2. Resistors:	
1 MegΩ 1% (size 0402) (1) – For Soldering	**250 kΩ 1% (size 0402) (1) – For Soldering**
40.2 kΩ 1% (size 0402) (1) – For Soldering	**500 Ω (1)**
400 KΩ (2)	**10 GΩ (1)**
35 KΩ (2)	**50 kΩ (1)**
3. Capacitors:	
10 uF (size 0805) (2) – For Soldering	**1 uF (size 0805) (1) – For Soldering**
10 uF (2)	**0.01uF (1)**
4. LTC3105 –MSOP-12 – For Soldering	**LTC3105 IC (1) – For Breadboard**
5. Solar Panel (1) with (Vin and Vout pin connections) – For Breadboard	
6. Solar Panel (1) – for Soldering	
7. USB (1) – For Soldering	
8. Proto board/ bread board (1)	
9. Connecting wires	
10. Diode: 1N4148 (1)	
11. MOSFET: 2N7000 (1)	
12. OPAMP: LT1001/LT1006 (1)	
13. Analog Device ADALM2000 PCIe measurement unit (+/-5 V adjustable DC supply with proper frequency range) (1)	
14. Soldering Equipment – Contact Audrey for the list of required equipment	