```
Hierarchy
  0
    Lab6
😑 💟 🦺 Pipeline Top (Pipeline Top.v)
     V S1 Reg - S1 Register (S1 Register.v)
     V Reg File - nbit register file (nbit register file.v)
          writeselect - nbit demux (nbit demux.v)
          DFFS - DFF (DFF.v)
          S2 Reg - S2 Register (S2 Register.v)

■ V Source Mux - mux R2 or Imm (mux R2 or Imm.v)
     🚊 🔽 ALU 32 - alu top (alu top.v)
       □ V alu1bit - ALU (ALU.v)
               mux b inv - mux 1x2 (mux 1x2.v)
             V adder1b - FA str (FA str.v)
             v alu_select - mux_8to1 (mux_8to1.v)
     🖳 🔽 S3_Reg - S3_Register (S3_Register.v)
```