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EC413

Lab 5: Design Hierarchy Description

The top of my design hierarchy is a top_module that calls the top modules for both the structural and behavioral para_ALUs. The structural ALU's top module calls the para_alu and transfers the data into result and c_out registers. Another level down, the para_alu uses a generate statement to create multiple bit-slice ALUs based on the parameter W in the top_module. The ALUs are created from an alu1bit module. This module uses three sub-modules: a 2 to 1 mux, a 8 to 1 mux, and 1-bit full adder. The top_module also instantiates the top_verification_alu which is behavioral. The lab5.pdf said this would be provided, but I couldn't find it on Blackboard so I made my own. The top_verification_alu also has a parameter W that is passed to the sub-module verification_alu and as well as registers for the result and c_out.

I get a few errors when simulating, but on Piazza the professor said that at least all but one of them is expected. For the SUB operation my error_flag is tripped when for instance I do 32'hffffffff - 32'hfffffffe because c_out is 1 structurally, but c_out_verify is 0 behaviorally. The only other error I get is because the error_flag stays on at the beginning of the AND operation until the first clock tick.