

EE 314A: Final Project Report

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1 Specifications Achieved

Block	Parameter	Design Specifications: Milestone 3	Notes	Achieved: Milestone 3
PA	Center Frequency	5.9 GHz	Channel BW: 20 MHz	5.9 GHz
	Output Power	> 15 dBm		18.03 dBm
	Load Impedance	50 Ω		50 Ω
	Input Power	4 dBm	Max	4 dBm
	Input Source Impedance	50 Ω		50 Ω
	Peak PAE	> 20 %	Center frequency	43.50%
	OP1dB	> 11 dBm		18.21 dBm
	HD2	< -35 dBc	Center frequency, w/ 15 dBm Pout	-39.8 dBc
	OIP3	> 21 dbm	Center frequency	24.75 dBm
	ACPR	-	64 QAM, 802.11n (MCS5) Pin = -4 dBm	Upper: -22.46 dB Lower: -21.93 dB
	EVM	-	64 QAM, 802.11n (MCS5) Pin ∈ [-15 dBm, -10 dBm, -4 dBm]	Pin @ -15 dBm: 2.87% Pin @ -10 dBm: 9.15% Pin @ -4 dBm: 13.46%
	Stability Factor: In-Band	> 1	Pin ∈ [-10 dBm, 4 dBm] f ∈ [2.9 GHz, 8.9 GHz]	<input checked="" type="checkbox"/>
	Stability Factor: Out-of-Band	> 1	Pin = -10 dBm f ∈ [0.2 GHz, 20 GHz]	<input checked="" type="checkbox"/>
	Vdd	1.8 V		1.8 V
FOM_PA				
	FOM_PA	(PAE_max)*(A+B+C)	PAE_max at 5.9 GHz A = Psat - 14 dBm B = (-HD2) - 35 dBc @ Psat C = OIP3 - 21 dBm Psat = min{OP1dB + 4 dB, Pout,max for Pin < 4 dBm}	547
LNA	Center Frequency	2.4 GHz	Channel BW: 400 MHz	2.4 GHz
	Input Source Impedance	50 Ω		50 Ω
	Load Impedance	50 Ω		50 Ω
	VDD	1 V		1 V
	Input Match (S11)	< -10 dB	At center frequency	-10.2 dB
	NF (Standalone)	-	Max across BW	2.1 dB
	NF (Diplexer, TX Off)	< 3 dB	Max across BW	3.15 dB
	NF (Diplexer, TX On)	< 4 dB	Max across BW	6.9 dB
	IIP3	> -23 dBm	At center frequency	-9.9 dBm
	G_T	-	At center frequency	12.6 dB
	P_LNA	-		351 μW
FOM_LNA				
	FOM_LNA	G_T / P_{LNA}^2	At center frequency	$149 \times 10^6 \text{ W}^{-2}$
Chip Area		1024 μm x 1024 μm		790 μm x 790 μm

Table 1: Summary of achieved specifications.

2 Circuit Schematics

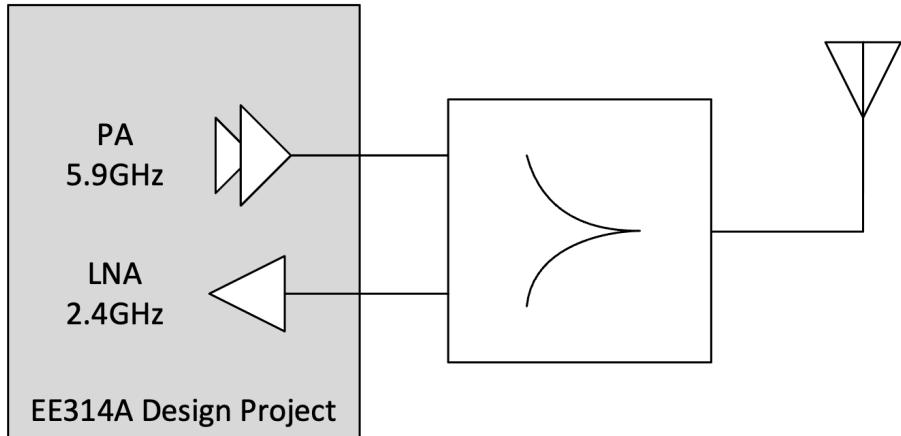


Figure 1: Transceiver TX/RX block diagram.

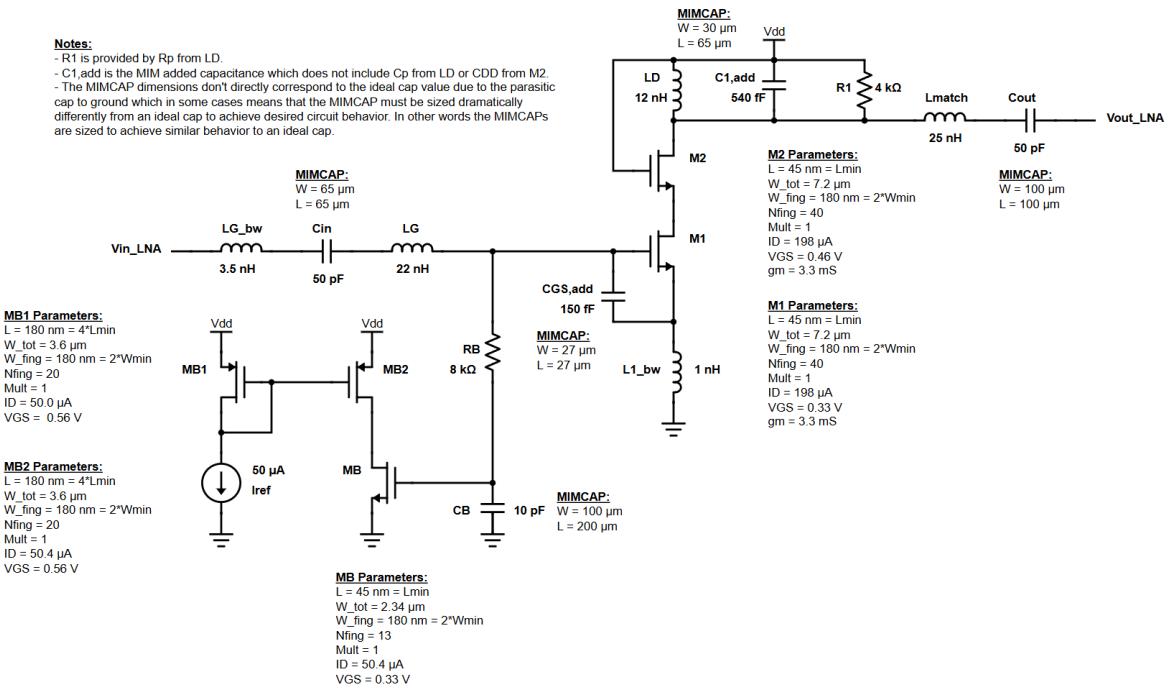
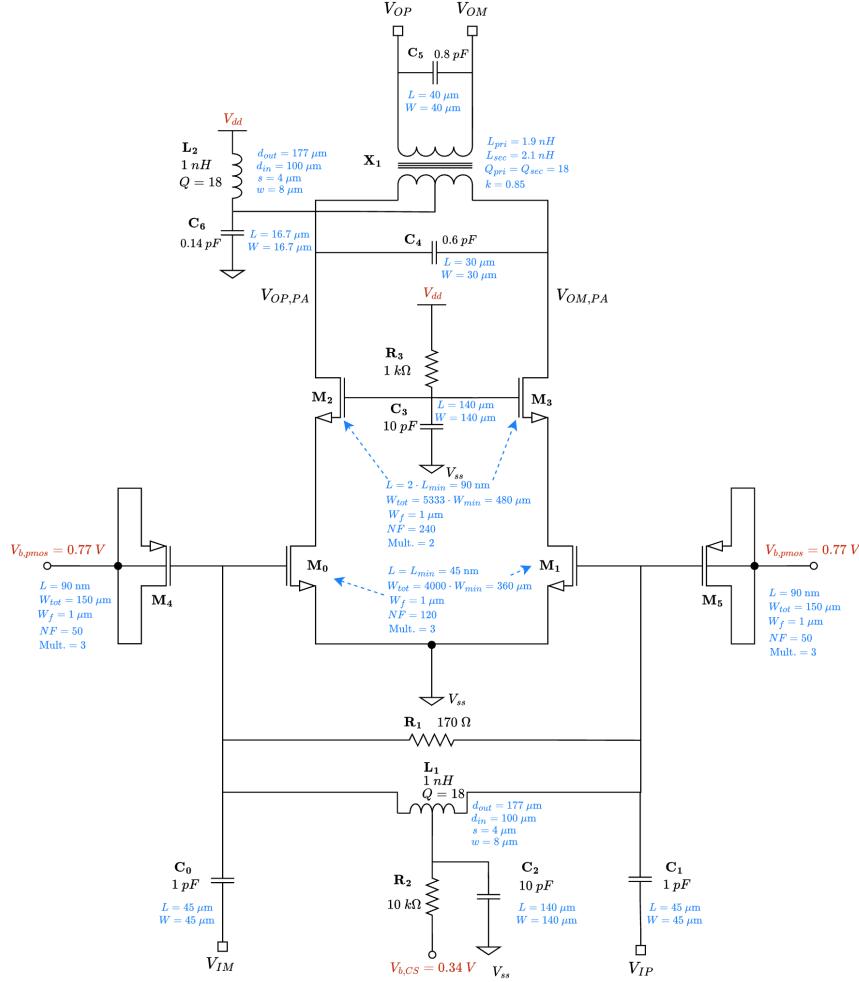
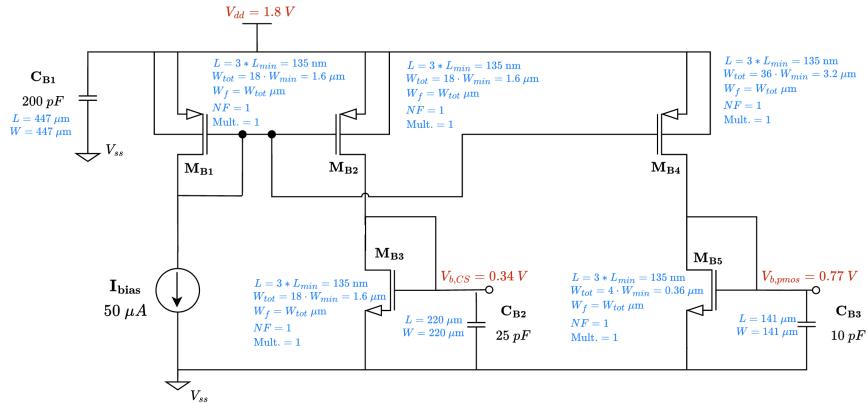


Figure 2: LNA circuit schematic.



(a) PA schematic - output stage.



(b) PA schematic - bias network.

Figure 3: Power amplifier circuit schematic.

3 Design Netlist

```

// Point Netlist Generated on: Jun  3 14:25:54 2025
// Generated for: spectre
// Design Netlist Generated on: Jun  3 14:25:51 2025
// Design library name: shared_wd_ad_ar
// Design cell name: testbench_chip_trx_netlist
// Design view name: config
simulator lang=spectre
include "ade_e.scs"
global 0
parameters temperature=27 vbias_comp_scaler=2 vbias_comp_mirror_sclaer=(3 *
 \
6 * 2) vb_pmos=0.77 pmos_W=1u pmos_NF=50 pmos_L=90n Cin_comp_dim=55u \
Ctrap_dim=16.7u Ctrap=140f Csec_dim=40e-6 Cpri_dim=30e-6 \
Cin_dim=77.5e-6 Cbias_dim=45e-6 cvdd_dim=447e-6 Cvdd=100p \
Cbias_mirror=25p nbond_trx=2 n_bond_vdd=16 Cbias2=10p n_downbond=15 \
Cbias=10p Rbias2=1k Rbias=10k k=0.85 Qs=18 Qp=18 W_gain_stage=1u \
W_casc_stage=1u vbias_scaler=50 vbias_casc_scaler=2 Rterm=170 \
nf_gain_stage=120 nf_casc_stage=240 mult_gain=3 mult_casc=2 Lsec=2.1n \
Lpri=1.9n L_gain_stage=45n L_casc_stage=90n Csec=300f Cpri=300f Cin=3p
 \
frx=2.4G ftx=5.9G prx=-40 ptx=4 RL=50 RS=50 ftx2=6G ptx2=4 frx2=2.5G \
prx2=-40 L_rx_bw=3.5 L1_bw_dim=1 mult_pmos=mult_gain
include "$EE314a_HOME/models/ee314a.mod"

// Library name: shared_wd_ad_ar
// Cell name: ind_bondwire_gnd_paddle
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt ind_bondwire_gnd_paddle board pad vss
parameters _par0 length_in_mm
    Cpad (pad vss) capacitor c=_par0 * 50f
    Rbond (net5 board) resistor r=0.31*length_in_mm/_par0
    Lbond (pad net5) inductor l=1e-9*length_in_mm/sqrt(_par0)
ends ind_bondwire_gnd_paddle
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: ind_bondwire
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt ind_bondwire board pad vss

```

```

parameters _par0 length_in_mm
    Lpin (net9 net3) inductor l=0.5n/_par0
    Lbond (pad net5) inductor l=1e-9*length_in_mm/sqrt(_par0)
    Cpad (pad vss) capacitor c=_par0* 50f
    Rpin (net3 board) resistor r=600.0m/_par0
    Rbond (net5 net9) resistor r=0.31*length_in_mm/_par0
ends ind_bondwire
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: package_trx
// View name: schematic1
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
subckt package_trx rx rx_pkg trx_gnd trx_gnd_pkg tx tx_pkg vdd_rx \
    vdd_rx_pkg vdd_tx vdd_tx_pkg vss vss_pkg lna_ind
    Irx_ind (trx_gnd_pkg lna_ind gnd) ind_bondwire_gnd_paddle _par0=1 \
        length_in_mm=L1_bw_dim
    Ivss_bw (vss_pkg vss gnd) ind_bondwire_gnd_paddle _par0=15 \
        length_in_mm=0.25
    V0 (gnd 0) vsource dc=0 type=dc
    Ivddrx_bw (vdd_rx_pkg vdd_rx gnd) ind_bondwire _par0=10 \
        length_in_mm=0.3
    Ivddtx_bw (vdd_tx_pkg vdd_tx gnd) ind_bondwire _par0=16 \
        length_in_mm=0.3
    Irx_bw (rx_pkg rx gnd) ind_bondwire _par0=1 length_in_mm=L_rx_bw
    Itrxgnd_bw (trx_gnd_pkg trx_gnd gnd) ind_bondwire _par0=2 \
        length_in_mm=0.3
    Itx_bw (tx_pkg tx gnd) ind_bondwire _par0=2 length_in_mm=0.3
ends package_trx
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: ind_2p4GHz_12nH_single-ended_lp
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
subckt ind_2p4GHz_12nH_single-ended_lp P1 P2 GND
    NPORT0 ( P1 GND P2 GND) nport \
        file="/home/users/afdunc/ee314a/opus/EMX_work/
            shared_wd_ad_ar.ind_2p4GHz_12nH_single-ended_lp.work/
            ind_2p4GHz_12nH_single-ended_lp.s2p" \
        datafmt=touchstone
ends ind_2p4GHz_12nH_single-ended_lp
// End of subcircuit definition.

```

```

// Library name: shared_wd_ad_ar
// Cell name: ind_2p4GHz_20nH_single-ended_lp
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt ind_2p4GHz_20nH_single-ended_lp P1 P2 GND
NPORT0 ( P1 GND P2 GND) nport \
    file="/home/users/afdunc/ee314a/opus/EMX_work/
        shared_wd_ad_ar_ind_2p4GHz_20nH_single-ended_lp.work/
        ind_2p4GHz_20nH_single-ended_lp.s2p" \
    datafmt=touchstone
ends ind_2p4GHz_20nH_single-ended_lp
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: ind_2p4GHz_20nH-single-ended_new
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt ind_2p4GHz_20nH_single-ended_new P1 P2 GND
NPORT0 ( P1 GND P2 GND) nport \
    file="/home/users/afdunc/ee314a/opus/EMX_work/
        shared_wd_ad_ar_ind_2p4GHz_20nH_single-ended_new.work/
        ind_2p4GHz_20nH_single-ended_new.s2p" \
    datafmt=touchstone
ends ind_2p4GHz_20nH_single-ended_new
// End of subcircuit definition.

// Library name: ee314a
// Cell name: nmos_rf2
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt nmos_rf2 D G S inh_bulk_n
parameters FingerWidth NumberOfFingers FingerLength Multiplier
M_nmos ( net5 net3 net2 inh_bulk_n) cmosn_ee314 \
    w=FingerWidth*NumberOfFingers l=FingerLength m=Multiplier \
    nf=NumberOfFingers
Rg_par ( net4 net3) resistor r=10/NumberOfFingers/Multiplier
Rs_par ( net2 net1) resistor r=10/NumberOfFingers/Multiplier
Rd_par ( net6 net5) resistor r=10/NumberOfFingers/Multiplier
L3 ( S net1) inductor l=10p + 1e-15*NumberOfFingers*Multiplier
L4 ( net6 D) inductor l=10p + 1e-15*NumberOfFingers*Multiplier
Lg_par ( G net4) inductor l=10p + 1e-15*NumberOfFingers*Multiplier

```

```

ends nmos_rf2
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: mimcap
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt mimcap pin1 pin2
parameters w l
    C1 (pin2 0) capacitor c=(w*l/2.2e-6+2*w+2*l)*8*8.85e-12
    C0 (pin1 pin2) capacitor c=(w*l/0.3e-6+2*w+2*l)*8*8.85e-12
ends mimcap
// End of subcircuit definition.

// Library name: ee314a
// Cell name: pmos4_rf2
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt pmos4_rf2 D G S B
parameters NumberOfFingers Multiplier FingerWidth FingerLength
    Rg_par (net4 net3) resistor r=10/NumberOfFingers/Multiplier
    Rs_par (net2 net1) resistor r=10/NumberOfFingers/Multiplier
    Rd_par (net6 net5) resistor r=10/NumberOfFingers/Multiplier
    L3 (S net1) inductor l=10p + 1e-15*NumberOfFingers*Multiplier
    L4 (net6 D) inductor l=10p + 1e-15*NumberOfFingers*Multiplier
    Lg_par (G net4) inductor l=10p + 1e-15*NumberOfFingers*Multiplier
    M_pmos (net5 net3 net2 B) cmosp_ee314 w=FingerWidth*NumberOfFingers \
        l=FingerLength m=Multiplier nf=NumberOfFingers
ends pmos4_rf2
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: LNA
// View name: schematic_lp_mim
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt LNA Ibias vdd vi vo vss ind_in inh_bulk_n
    L2 (vdd vout vss) ind_2p4GHz_12nH_single-ended_lp
    L5 (vin_lg vg vss) ind_2p4GHz_20nH_single-ended_lp
    R4 (vs ind_in) resistor r=1m isnoisy=no
    R0 (vg vb) resistor r=8K isnoisy=yes
    L3 (vout vout_ind vss) ind_2p4GHz_20nH_single-ended_new
    I14 (vb vb vss inh_bulk_n) nmos_rf2 FingerWidth=2*90n \

```

```

    NumberOfFingers=10 FingerLength=45n Multiplier=1
I9 (vout vdd net14 inh_bulk_n) nmos_rf2 FingerWidth=2*90n \
    NumberOfFingers=40 FingerLength=45n Multiplier=1
I3 (net14 vg vs inh_bulk_n) nmos_rf2 FingerWidth=2*90n \
    NumberOfFingers=40 FingerLength=45n Multiplier=1
I51 (vg vs) mimcap w=27.4u l=27.4u
I54 (vout_ind vo) mimcap w=100u l=100u
I52 (vb vss) mimcap w=100u l=200u
I53 (vdd vout) mimcap w=31u l=65u
I50 (vi vin_lg) mimcap w=65u l=65u
I22 (vb Ibias vdd vdd) pmos4_rf2 NumberOfFingers=20 Multiplier=1 \
    FingerWidth=180n FingerLength=180n
I21 (Ibias Ibias vdd vdd) pmos4_rf2 NumberOfFingers=20 Multiplier=1 \
    FingerWidth=180n FingerLength=180n
ends LNA
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: chip_rx_lna
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt chip_rx_lna Ibias vdd vi vo vss ind inh_bulk_n
    I5 (Ibias vdd vi vo vss ind inh_bulk_n) LNA
ends chip_rx_lna
// End of subcircuit definition.

// Library name: ee314a
// Cell name: mimcap_ee314
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt mimcap_ee314 pin1 pin2
parameters w l
    C1 (pin2 0) capacitor c=(w*l/2.2e-6+2*w+2*l)*3.9*8.85e-12
    C0 (pin1 pin2) capacitor c=(w*l/0.3e-6+2*w+2*l)*3.9*8.85e-12
ends mimcap_ee314
// End of subcircuit definition.

// Library name: ee314a_project
// Cell name: pa_xformer
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt pa_xformer vic vim vip vo voc

```

```

parameters Ls _par0 f0 Lp _par1 _par2
    Ind_s1 (vo net1) inductor l=Ls/2 q=_par0 fq=f0 mode=1
    Ind_p2 (vic vim) inductor l=Lp/2 q=_par1 fq=f0 mode=1
    Ind_s2 (net1 voc) inductor l=Ls/2 q=_par0 fq=f0 mode=1
    Ind_p1 (vip vic) inductor l=Lp/2 q=_par1 fq=f0 mode=1
    K1 mutual_inductor coupling=_par2 ind1=Ind_p2 ind2=Ind_s2
    K0 mutual_inductor coupling=_par2 ind1=Ind_p1 ind2=Ind_s1
ends pa_xformer
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: ind_5p9GHz_1nH_diff
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt ind_5p9GHz_1nH_diff P1 P2 Vdd GND
NPORT0 ( P1 GND P2 GND Vdd GND) nport \
        file=/home/users/austinxr/ee314a_2024/opus/EMX_work/
        shared_wd_ad_ar_ind_5p9GHz_1nH_diff.work/ind_5p9GHz_1nH_diff.s3p
        " \
datafmt=touchstone
ends ind_5p9GHz_1nH_diff
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: ind_5p9GHz_1nH_SE
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl
// pspice dspf
subckt ind_5p9GHz_1nH_SE P1 P2 GND
NPORT0 ( P1 GND P2 GND) nport \
        file=/home/users/austinxr/ee314a_2024/opus/EMX_work/
        shared_wd_ad_ar_ind_5p9GHz_1nH_SE.work/ind_5p9GHz_1nH_SE.s2p" \
datafmt=touchstone
ends ind_5p9GHz_1nH_SE
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: chip_tx_pa_m3
// View name: schematic_cgs_comp
// Inherited view list: spectre cmos_sch cmos.sch schematic verilog_a ahdl

```

```

// pspice dspf
subckt chip_tx_pa_m3 Ibias vdd vim vip vom vop vss inh_bulk_n
    I58 (vbias_comp vss) mimcap_ee314 w=224e-6 l=224e-6
    I48 (Cbias vss) mimcap_ee314 w=Cbias_dim l=Cbias_dim
    I53 (vtap vom) mimcap_ee314 w=Ctrap_dim l=Ctrap_dim
    I43 (vbias vss) mimcap_ee314 w=224e-6 l=224e-6
    I44 (vdd vss) mimcap_ee314 w=cvdd_dim l=cvdd_dim
    Cpri (vop_pa vom_pa) mimcap_ee314 w=Cpri_dim l=Cpri_dim
    Csec (vop vom) mimcap_ee314 w=Csec_dim l=Csec_dim
    I50 (vip vip_in) mimcap_ee314 w=Cin_comp_dim l=Cin_comp_dim
    I47 (vb_cascode vss) mimcap_ee314 w=Cbias_dim l=Cbias_dim
    I49 (vim vim_in) mimcap_ee314 w=Cin_comp_dim l=Cin_comp_dim
    R9 (vbias Cbias) resistor r=Rbias
    R8 (vim_in vip_in) resistor r=Rterm
    R12 (vdd vb_cascode) resistor r=Rbias2
    IPRB2 (vop net6) iprobe
    IPRB1 (net2 net13) iprobe
    IPRB0 (net8 net4) iprobe
    I57 (vbias_comp Ibias vdd vdd) pmos4_rf2 NumberOfFingers=1 \
        Multiplier=1 FingerWidth=vbias_comp_mirror_sclaer*90n \
        FingerLength=3*45n
    I54 (vbias_comp vip_in vbias_comp vbias_comp) pmos4_rf2 \
        NumberOfFingers=pmos_NF Multiplier=mult_pmos FingerWidth=pmos_W \
        FingerLength=pmos_L
    I22 (vbias Ibias vdd vdd) pmos4_rf2 NumberOfFingers=1 Multiplier=1 \
        FingerWidth=3*6*90n FingerLength=3*45n
    I30 (Ibias Ibias vdd vdd) pmos4_rf2 NumberOfFingers=1 Multiplier=1 \
        FingerWidth=3*6*90n FingerLength=3*45n
    I55 (vbias_comp vim_in vbias_comp vbias_comp) pmos4_rf2 \
        NumberOfFingers=pmos_NF Multiplier=mult_pmos FingerWidth=pmos_W \
        FingerLength=pmos_L
    I21 (vtap vom_pa vop_pa net6 vom) pa_xformer Ls=Lsec _par0=Qs f0=5.9G \
        Lp=Lpri _par1=Qp _par2=k
    L1 (vip_in vim_in Cbias net9) ind_5p9GHz_1nH_diff
    L0 (vdd vtap vss) ind_5p9GHz_1nH_SE
    I31 (vop_pa vb_cascode net8 inh_bulk_n) nmos_rf2 \
        FingerWidth=W_casc_stage NumberOfFingers=nf_casc_stage \
        FingerLength=L_casc_stage Multiplier=mult_casc
    I56 (vbias_comp vbias_comp vss inh_bulk_n) nmos_rf2 \
        FingerWidth=2*90n*vbias_comp_scaler NumberOfFingers=1 \
        FingerLength=3*45n Multiplier=1
    I14 (vbias vbias vss inh_bulk_n) nmos_rf2 \
        FingerWidth=2*90n*vbias_scaler NumberOfFingers=1 \
        FingerLength=3*45n Multiplier=1
    M0 (net4 vim_in vss inh_bulk_n) nmos_rf2 FingerWidth=W_gain_stage \

```

```

    NumberOfFingers=nf_gain_stage FingerLength=L_gain_stage \
    Multiplier=mult_gain
M1 (net13 vip_in vss inh_bulk_n) nmos_rf2 FingerWidth=W_gain_stage \
    NumberOfFingers=nf_gain_stage FingerLength=L_gain_stage \
    Multiplier=mult_gain
I32 (vom_pa vb_cascode net2 inh_bulk_n) nmos_rf2 \
    FingerWidth=W_casc_stage NumberOfFingers=nf_casc_stage \
    FingerLength=L_casc_stage Multiplier=mult_casc
ends chip_tx_pa_m3
// End of subcircuit definition.

// Library name: ee314a-project
// Cell name: mimcap
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
subckt mimcap_schematic pin1 pin2
parameters w l
    C1 (pin2 0) capacitor c=(w*l/2.2e-6+2*w+2*l)*8*8.85e-12
    C0 (pin1 pin2) capacitor c=(w*l/0.3e-6+2*w+2*l)*8*8.85e-12
ends mimcap_schematic
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: chip_trx
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
subckt chip_trx gnd gnd_rx lna_ind_in vdd_rx vdd_tx vi_rx vim_tx vip_tx \
    vo_rx vo_tx vocm_trx vss inh_bulk_n
I24 (net2 vocm_trx) isource dc=50u type=dc
I12 (net1 vocm_trx) isource dc=50u type=dc
Ilna (net1 vdd_rx vi_rx vo_rx vocm_trx lna_ind_in inh_bulk_n) \
    chip_rx_lna
Ipa (net2 vdd_tx vim_tx vip_tx vocm_trx vo_tx vocm_trx inh_bulk_n) \
    chip_tx_pa_m3
Ivddrxdecap (vdd_rx vss) mimcap_schematic w=100u l=100u
Ivddtxdecap (vdd_tx vss) mimcap_schematic w=100u l=100u
R0 (gnd_rx vocm_trx) resistor r=1m
ends chip_trx
// End of subcircuit definition.

// Library name: shared_wd_ad_ar
// Cell name: diplexer
// View name: schematic

```

```

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
subckt diplexer antenna rx tx vss
    C12 (tx net12) capacitor c=501.1f
    C11 (net10 net9) capacitor c=349.5f
    C10 (net9 antenna) capacitor c=501.1f
    C9 (net8 net10) capacitor c=342.1f
    C8 (net7 net8) capacitor c=341.0f
    C7 (net6 net7) capacitor c=342.1f
    C6 (net12 net6) capacitor c=349.5f
    C5 (net5 vss) capacitor c=1.235p
    C4 (net4 vss) capacitor c=1.316p
    C3 (net2 vss) capacitor c=1.327p
    C2 (net3 vss) capacitor c=1.327p
    C1 (net1 vss) capacitor c=1.316p
    C0 (net11 vss) capacitor c=1.235p
    L12 (rx net11) inductor l=7.25n
    L11 (net10 vss) inductor l=2.289n
    L10 (net9 vss) inductor l=2.439n
    L9 (net8 vss) inductor l=2.269n
    L8 (net7 vss) inductor l=2.269n
    L7 (net6 vss) inductor l=2.289n
    L6 (net12 vss) inductor l=2.439n
    L5 (net4 net5) inductor l=8.617n
    L4 (net5 antenna) inductor l=7.25n
    L3 (net3 net4) inductor l=8.803n
    L2 (net2 net3) inductor l=8.833n
    L1 (net1 net2) inductor l=8.803n
    L0 (net11 net1) inductor l=8.617n
ends diplexer
// End of subcircuit definition.

```

```

// Library name: shared_wd_ad_ar
// Cell name: testbench_chip_trx_netlist
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I82 (vss_pkg 0) iprobe
Ipackage (net4 vi_rx net1 trx_gnd net3 vo_tx net2 vdd_rx net9 vdd_tx vss \
           vss_pkg net5) package_trx
Ichipcore (0 vss net5 net2 net9 net4 vim_tx vip_tx vo_rx net3 net1 vss 0) \
           chip_trx
Idiplexer (v_antenna vi_rx vo_tx trx_gnd) diplexer
VDD_TX (vdd_tx 0) vsource dc=1.8 type=dc
VDD_RX (vdd_rx 0) vsource dc=1 type=dc

```

```

PORT2 (vo_rx vss) port r=RL num=2 type=dc isnoisy=no
PORT3 (vip_tx vim_tx) port r=RS num=3 type=dc mag=1 isnoisy=no
PORT1 (v_antenna trx_gnd) port r=RS num=1 type=sine freq=frx dbm=prx \
    freq2=frx2 dbm2=prx2 mag=1 noisetemp=27 isnoisy=yes
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5
    \
    digits=5 cols=80 pivrel=1e-3 sensfile="..//psf/sens.output" \
    checklimitdest=psf
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppont where=rawfile
hb hb tstabenvlpstop=0 autotstab=yes oversample=[1 1]
+ fundfreqs=[(frx) (frx2)] maxharms=[5 5] errpreset=moderate
+ annotate=status
sp sp ports=[PORT1 PORT2] start=1M stop=10G dec=200 donoise=yes \
    oprobe=PORT2 iprobe=PORT1 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save PORT1:p PORT2:p PORT2:p PORT3:p PORT3:p VDD_TX:p VDD_RX:p vdd_tx \
    vo_rx vss
saveOptions options save=allpub

```

4 Power Amplifier

The power amplifier (PA) design implements a class-AB differential cascode gain stage with a broadband transformer output matching network. The full design can be seen in Fig. 8a, with the associated DC bias circuit in Fig. 3b. Given the tunable broadband operating bandwidth and moderate requirements on PAE and linearity, a class-AB was identified as a good solution in order to balance these specifications as class-AB has been demonstrated to achieve good linearity, efficiency, and output power over wide bandwidths [1; 2; 3]. For this reason, class-AB designs are prevalent in high peak-to-average-power-ratio (PAPR) mobile devices where a balance among the primary PA design metrics is desired.

The class-AB is characterized by its conduction angle, which is nominally defined between the ranges $3\pi/2 \leq \theta \leq \pi/2$ for standard class-AB, and $\pi \leq \theta \leq 3\pi/2$ for *deep* class-AB. For increased efficiency, deep class-AB is preferred, but this comes at the expense of increased second and third harmonic components, reducing the linearity.

In general, the only difference between PA class A, B, AB, and C is the bias point of the transconductance device. The tradeoffs in Fig. 4 give a qualitative picture to how the bias point should be selected per the application requirements.

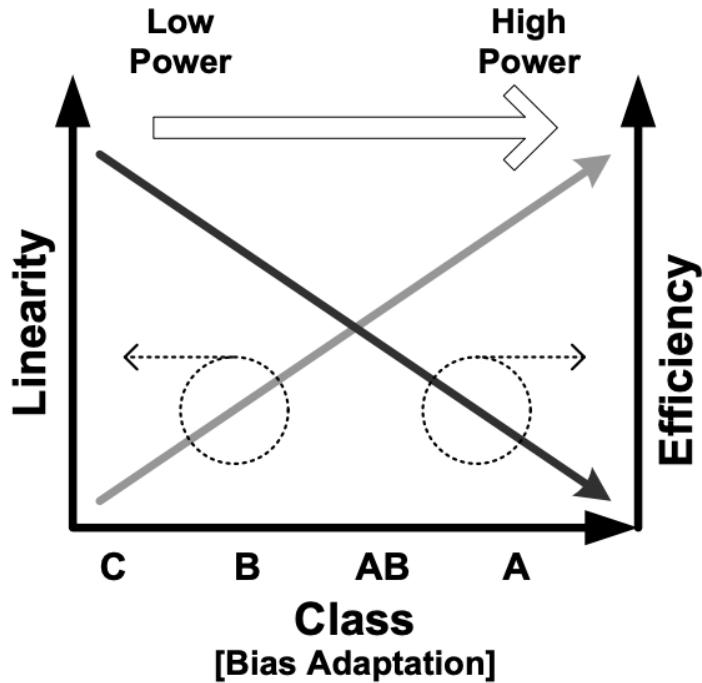


Figure 4: Conceptual trade-offs of PA classes as a function of bias point [4].

A cascode topology is implemented in order to allow for greater overall output swing capability, as the common-gate stage buffers the input common-source stage from the output and helps distribute the voltage stress across the drain-to-source of each transistor. The cascode also improves reverse isolation and hence PA stability. A differential architecture is elected as it reduces even-order nonlinearity, enhancing HD2 performance. Additionally, the differential topology rejects common-mode noise which may couple to the PA bias lines, and lends itself nicely to utilizing transformers for input/output matching. The transformer allows for a very broadband match to be achieved, as well as provides the ability to simply bias the common-mode point via a center tap, saving valuable chip area that otherwise would

be spent on RF chokes. Lastly, the differential structure can greatly reduce the degeneration effect of bondwires at the source of the CS amplifier.

4.1 Device Sizing

To size the PA common-source element (which is providing the trans-conductance), we get an initial estimate for the necessary peak current capability and thus device sizing based on the power delivery requirements to the antenna. The cascode (common-gate element) is initially sized using the same W/L parameters as the common-source. Both designs had their sizing finalized after sweeping over candidate bias points and size permutations in order to balance P_{out} , PAE, and linearity across the operating bandwidth.

4.1.1 Loadline Analysis

Below we describe the theory of the PA loadline for a single-ended output stage at a reduced conduction angle and how this was used to obtain an initial device sizing prior to load-pull optimization. The current-handling capabilities are estimated using a load-line analysis at a reduced conduction angle, as shown in Fig. 5.

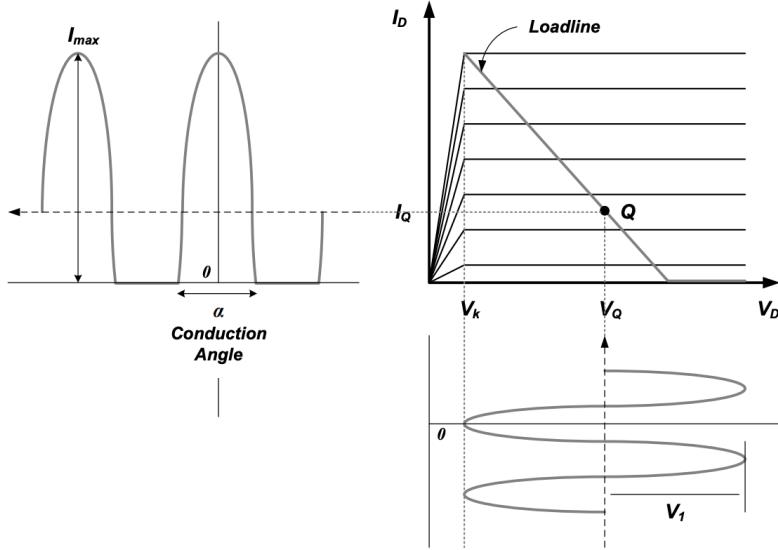


Figure 5: PA load-line at a reduced conduction angle [4].

A Fourier analysis of the current waveform allows representation of the drain current in terms of the DC, fundamental, and harmonics as:

$$\begin{aligned} i_D(\theta) &= I_Q + (I_{\max} - I_Q) \cdot \cos \theta, -\frac{\alpha}{2} < \theta < \frac{\alpha}{2} \\ &= 0, -\pi < \theta < -\frac{\alpha}{2} \text{ and } \frac{\alpha}{2} < \theta < \pi \end{aligned} \quad (1)$$

which we can simplify to:

$$i_D(\theta) = I_{\max} \cdot \frac{\cos \theta - \cos \left(\frac{\alpha}{2} \right)}{1 - \cos \left(\frac{\alpha}{2} \right)}, -\frac{\alpha}{2} < \theta < \frac{\alpha}{2} \quad (2)$$

Applying a Fourier series ¹ on (2), we have that:

$$\begin{aligned} i_D(\theta) &= I_{DC} + \sum_{n=1}^{\infty} I_n \cos(n\theta), -\frac{\alpha}{2} < \theta < \frac{\alpha}{2} \\ I_{DC} &= \frac{1}{2\pi} \cdot \int_{-\alpha/2}^{\alpha/2} I_{\max} \cdot \frac{\cos \theta - \cos(\frac{\alpha}{2})}{1 - \cos(\frac{\alpha}{2})} \cdot d\theta \\ I_n &= \frac{1}{\pi} \cdot \int_{-\alpha/2}^{\alpha/2} I_{\max} \cdot \frac{\cos \theta - \cos(\frac{\alpha}{2})}{1 - \cos(\frac{\alpha}{2})} \cdot \cos(n\theta) \cdot d\theta \end{aligned} \quad (3)$$

From Eq. (3) we can see that the higher-order current components degrade the magnitude of the branch current, with the second and third terms having the most prominent impact on the PA performance.

The Fourier analysis of the current waveforms as a function of conduction angle reveals the relation between the strength of the fundamental branch current to the DC and higher order harmonic terms, shown in Fig. 6a. We see that class-AB has non-trivial harmonic content in the second harmonic. The differential topology helps to minimize the second harmonic content, however, second harmonic generation can still manifest in the PA output spectrum due to non-idealities such as improper termination of common node voltages at circuit virtual grounds.

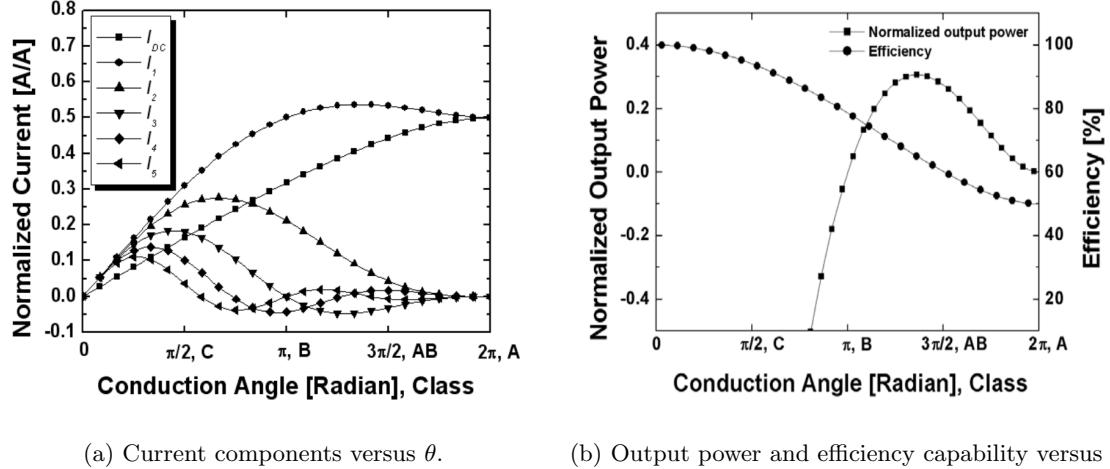


Figure 6: Fourier analysis of a reduced conduction angle PA bias.

Additionally, we can express the efficiency, η , neatly based on the Fourier components:

$$\begin{aligned} I_{DC} &= \frac{I_{\max}}{2\pi} \cdot \frac{2 \cdot \sin(\frac{\alpha}{2}) - \alpha \cdot \cos(\frac{\alpha}{2})}{1 - \cos(\frac{\alpha}{2})} \\ I_1 &= \frac{I_{\max}}{2\pi} \cdot \frac{\alpha - \sin \alpha}{1 - \cos(\frac{\alpha}{2})} \\ \eta &= \frac{P_1}{P_{DC}} = \frac{\frac{V_1}{\sqrt{2}} \cdot \frac{I_1}{\sqrt{2}}}{V_Q \cdot I_Q} = \frac{\alpha - \sin \alpha}{2 [2 \cdot \sin(\frac{\alpha}{2}) - \alpha \cdot \cos(\frac{\alpha}{2})]} \end{aligned} \quad (4)$$

We see from the above analysis and Fig. 6b that class-AB designs afford high fundamental tones with reduced DC energy compared to class A, thus the PAE is improved. For enhanced efficiency, we see a lower conduction angle is better at the expense of harmonic content.

¹Note that for the ideal differential loadline analysis, the summation in (3) is only over odd harmonics

4.1.2 Initial Estimates

For our system, we require an output power of $P_{out} = 15$ dBm delivered to the antenna port at a center frequency of $f_0 = 5.9$ GHz. We budget 3 dB of insertion loss for the output transformer matching network, bondwires, and diplexer; thus the PA should deliver at least 18 dBm, with ideally more in order to optimize the figure-of-merit (FOM)

Given that our output stage is utilizing a cascode architecture, the allowable output node can swing up to V_{dd} and down to $V_{knee} = V_{dsat,1} + V_{dsat,2}$ to maintain saturation of the output stage. As an initial estimate, we say $V_{knee} = 0.2$ V. Given the equations developed in Section 4.1.1, target output power from the PA of 18 dBm, and the allowed output swing, we find that $R_{opt} = 15.6 \Omega$, $I_{1,pk} = 100.9$ mA, $I_{DC} = 0.5 * 48.2$ mA for a class-AB conduction angle of 240° . Given a moderate inversion design target of $g_m/I_d = 8$, and knowledge of the current density of $I_D/W \approx 150 \mu\text{A}/\mu\text{m}$ for $V_{GS} = 0.5$ V, $V_{DS} = 0.5$ V for a minimum length $L = 45$ nm device from the technology characterization sweeps, we find that we require a width of $W \approx 336.2 \mu\text{m}$ to support the design constraints. The initial output stage is a differential cascode topology having the common-source and common-gate blocks sized to $W/L = 336 \mu\text{m}/0.045 \mu\text{m}$, and a gate bias of $V_{b,cs} = 0.5$ V and $V_{b,cg} = V_{dd} = 1.8$ V as a starting point.

4.1.3 Load-Pull

Based on the initial sizing, the circuit was simulated in a Cadence Virtuoso test-bench, making use of periodic steady-state and harmonic balance simulations in order to extract PAE, P_{out} , OP1dB, HD2, and OIP3 performance. Firstly, the design was implemented with ideal gate bias elements, capacitors, and inductors. The device sizes and bias voltages were swept over ranges around the nominal design widths and bias points in order to obtain a PAE and P_{out} capability with enough margin from the output stage. The CS device was optimized to a total device width of $W = 360 \mu\text{m}$, $L = 45$ nm at a nominal gate bias of $V_{bias} = 0.34$ V. The cascode CG device was scaled to a channel length of $L = 90$ nm in order to afford a higher output impedance and enhance the buffering capability of the transconductance device. In practice, the cascode is often a thick oxide device which requires longer channel lengths. The CG width is scaled accordingly to $W = 480 \mu\text{m}$.

Using a port adapter placed at the output and running a load-pull analysis with $P_{in} = 4$ dBm, we observe in Fig. 7 that the optimum load impedance for this sizing, bias point, and input power occurs at $Z_{opt} = 32.35 + j30.31 \Omega$. Given the output power capability of this stage under these device sizing and bias conditions, we proceed to developing an optimal matching at the output and input, which we cover in later sections.

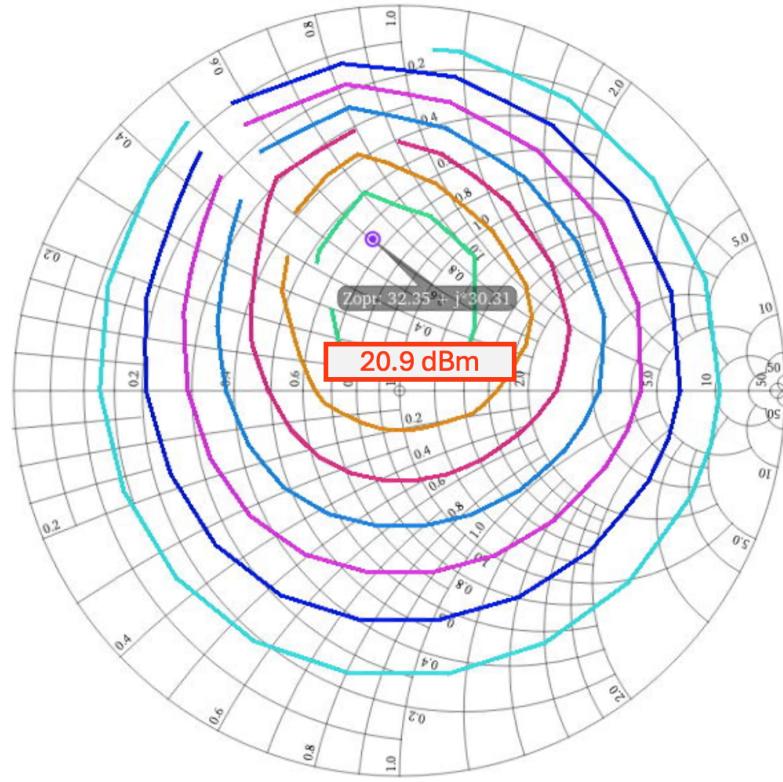
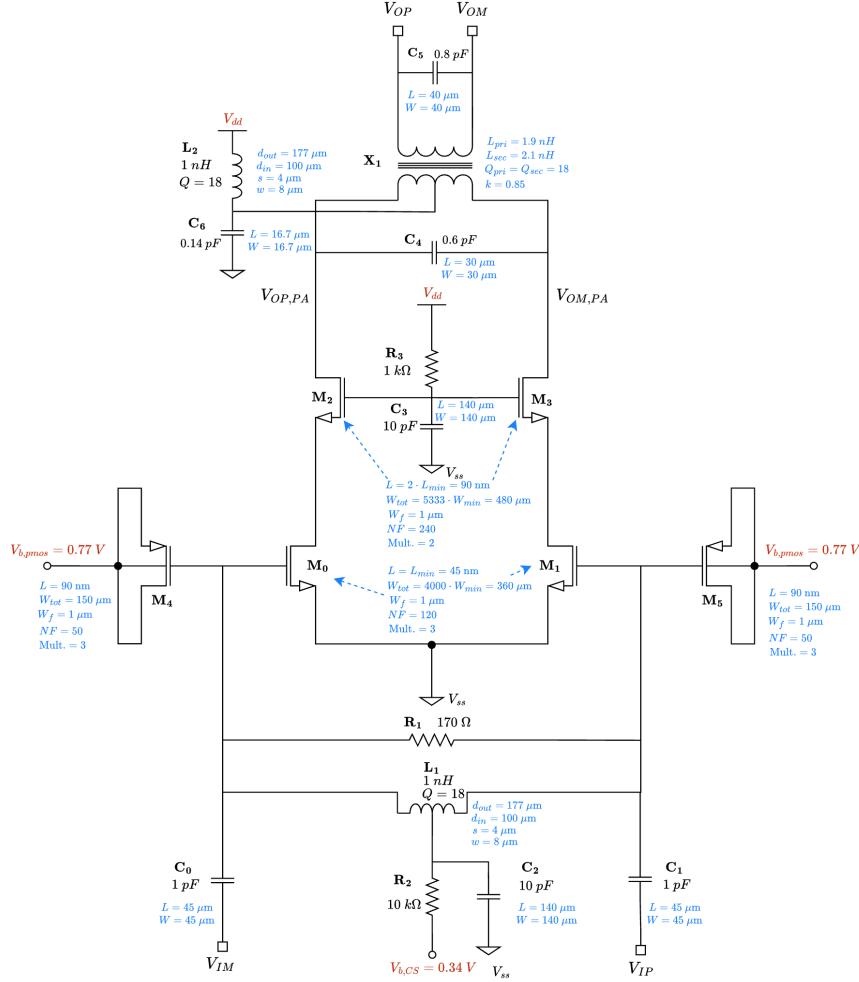


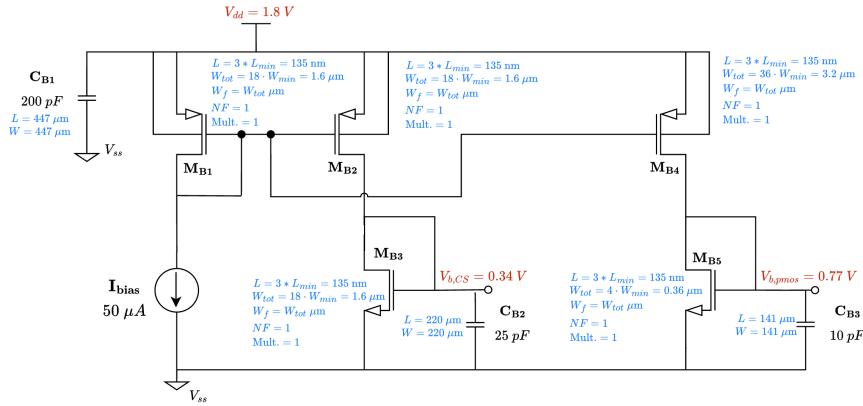
Figure 7: Output stage load-pull, $f = 5.9$ GHz, $P_{in} = 4$ dBm, $Z_{opt} = 32.35 + j30.31 \Omega$.

4.2 Topology Analysis

In the following section, the function of each block within the PA will be covered.



(a) PA schematic - output stage.



(b) PA schematic - bias network.

Figure 8: Power amplifier circuit schematic.

4.2.1 Bias Network & Decoupling

The PA bias network is displayed in Fig. 8b. A reference current source of $I_{bias} = 50 \mu\text{A}$ is mirrored and fed to a network of diode-connected NMOS devices which are sized in order to synthesize the desired gate voltages for the input common-source and C_{gs} compensation stages of 0.334 V and 0.77 V,

respectively.

The channel length for these devices was increased in order to provide more robustness to channel-length modulation effects in the presence of the large amplitude signals that these bias lines can see during the max-input power driving conditions.

4.2.2 Output Match

Following the load-pull based sizing of the output stage in Sect. 4.1.3, the output matching network is designed to present the optimum impedance, $Z_{opt} = 32.35 + j30.31 \Omega$, to the output of the PA. We proceed with the output transformer design using the methodology covered in [5], where the transformer is modeled as a second order doubly-tuned passive circuit shown in Fig. 9.

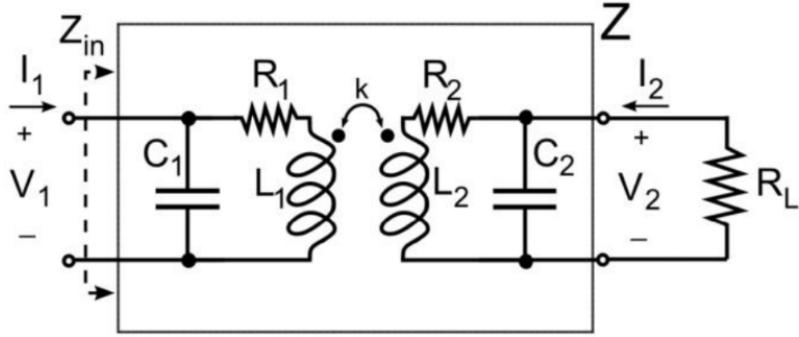


Figure 9: Equivalent model of doubly-tuned transformer matching network [5].

The design was initially prototyped such that the lower-band resonance, ω_L , was set to 5.9 GHz, given the following transformer parameters: $R_L = 50 \Omega$, $C_2 = 200 \text{ fF}$, $C_1 = 200 \text{ fF}$, $L_2 = 2 \text{ nH}$, $Q_1 = 16$, $L_1 = 2 \text{ nH}$, $Q_2 = 16$, $k = 0.85$. Including the second order parasitics of the chip such as bondwires to $V_{ss}/V_{trx,gnd}$, chip-to-board bondwires, and the diplexer itself, parameter sweeps were carried out in Virtuoso in order to arrive at an optimized value for each transformer element highlighted in Fig. 10.

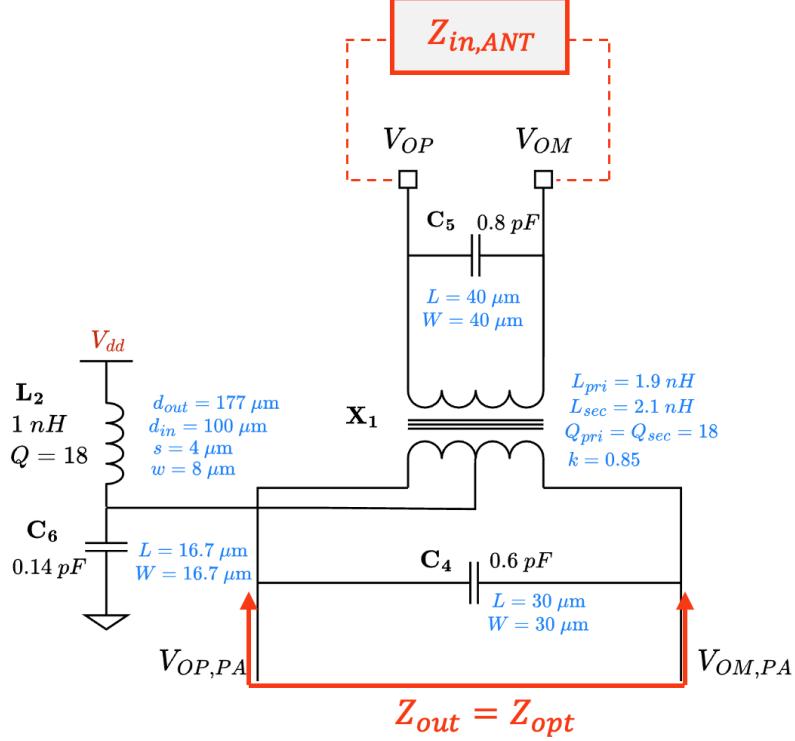


Figure 10: Output stage matching network based on a doubly-tuned transformer network. Z_{out}

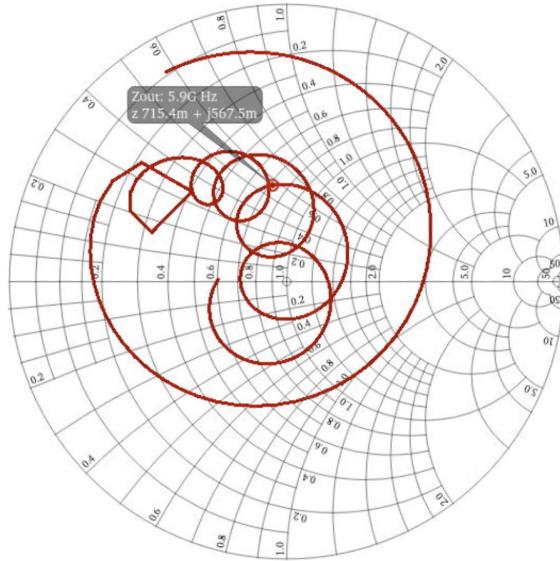


Figure 11: Output stage matching network smith chart to present Z_{opt} . All parasitics included.

4.2.3 Input Matching

With the output stage complete, we proceed to the input stage. During load-pull, the input impedance should be monitored in order to ensure a conjugate match is maintained [6] given the finite reverse isolation from the output to the input, reflected by the PA's S_{12} response. Since we are using a cascode device and the process technology has only moderate parasitic inductance to V_{ss} , the reverse isolation is

high enough such that the output matching network is sufficiently independent from the input network. Thus, the output matching network did not need to be iteratively updated with the input match when one of these networks changed.

Measuring the small-signal input impedance of the CS stage, the input match shown in Fig. 12 was developed. A resistive termination in shunt across the differential input was placed in order to lower the loaded-Q of the input network, hence broadening the bandwidth. Additionally, these input resistors can help provide linearization against the non-linearity of the input stages C_{gs} during maximum input power conditions, and also help make the PA stability more robust across input power drive levels for a wide range of frequencies. The tradeoff with these resistive terminations is that they contribute thermal noise which contributes to the power spectral density of the PA output noise, posing coexistence problems for an FDD based system such as this.

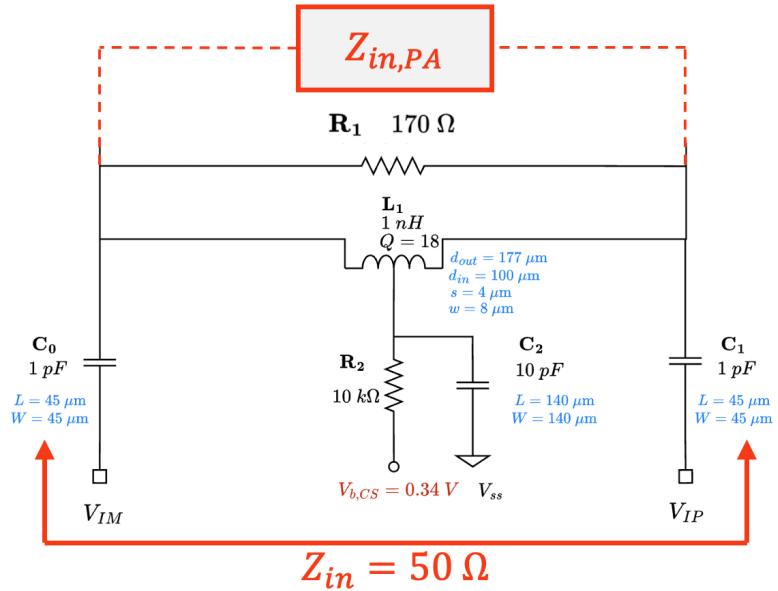
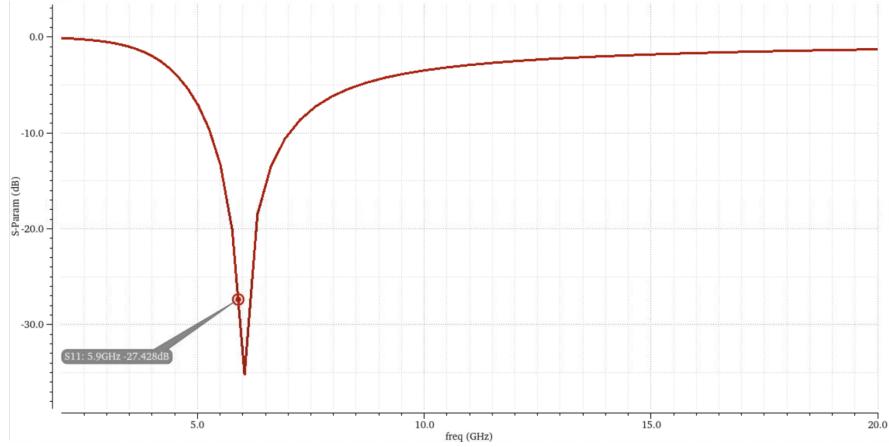
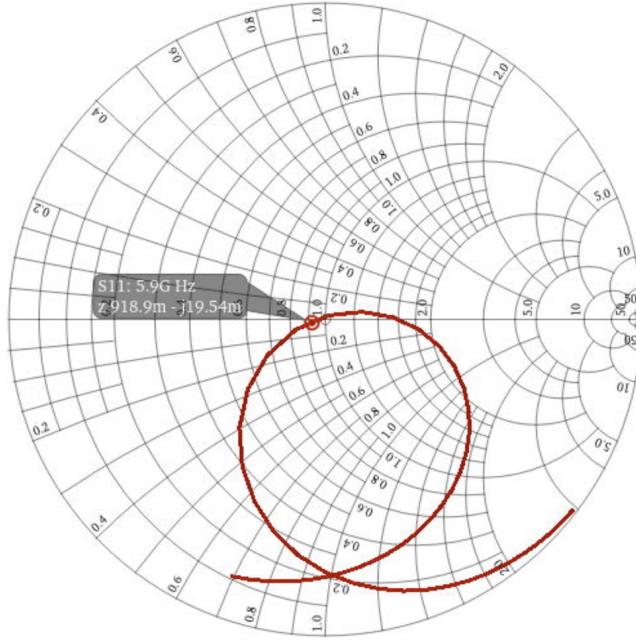


Figure 12: Input stage matching network based on a shunt-L series-C topology with resistive terminations. MIM capacitors and on-chip inductor geometries specified.



(a) Input match return loss.



(b) Input match S_{11} .

Figure 13: Power matching network performance.

The matching inductor is implemented on-chip using a planar octagonal topology. The sizing of the inductor was first estimated from the equations spelled out in [7]. The final design was optimized in EMX for 5.9 GHz and is shown in Fig. 14.

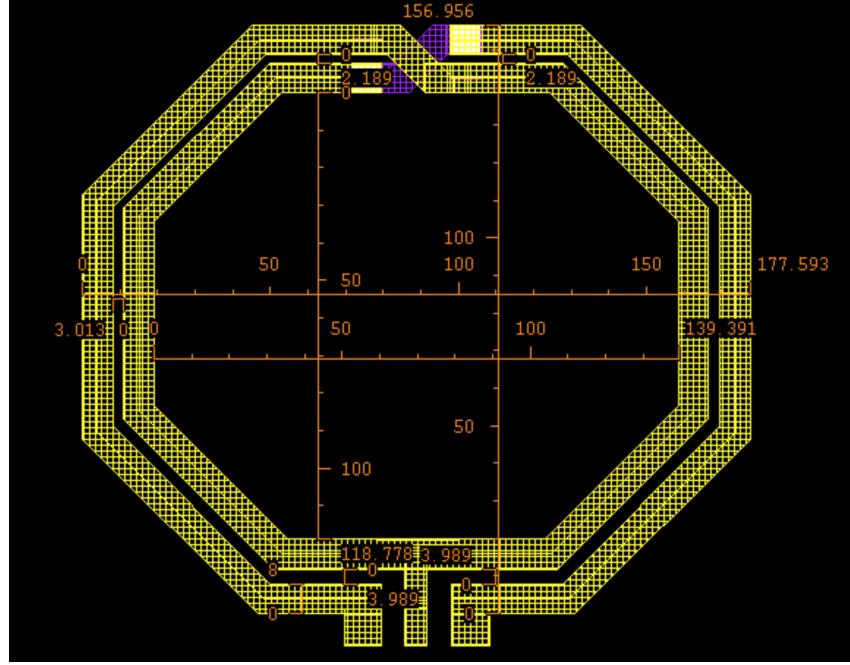


Figure 14: 5.9 GHz differential inductor with a center tap. $s_1 = 3.98 \mu\text{m}$, $s_2 = 3.013 \mu\text{m}$, $d_{\text{out},1} = 177.59 \mu\text{m}$, $d_{\text{out},2} = 156.956 \mu\text{m}$, $d_{\text{in},1} = 100 \mu\text{m}$, $d_{\text{in},2} = 139.391 \mu\text{m}$, $W = 8 \mu\text{m}$, $n = 2$.

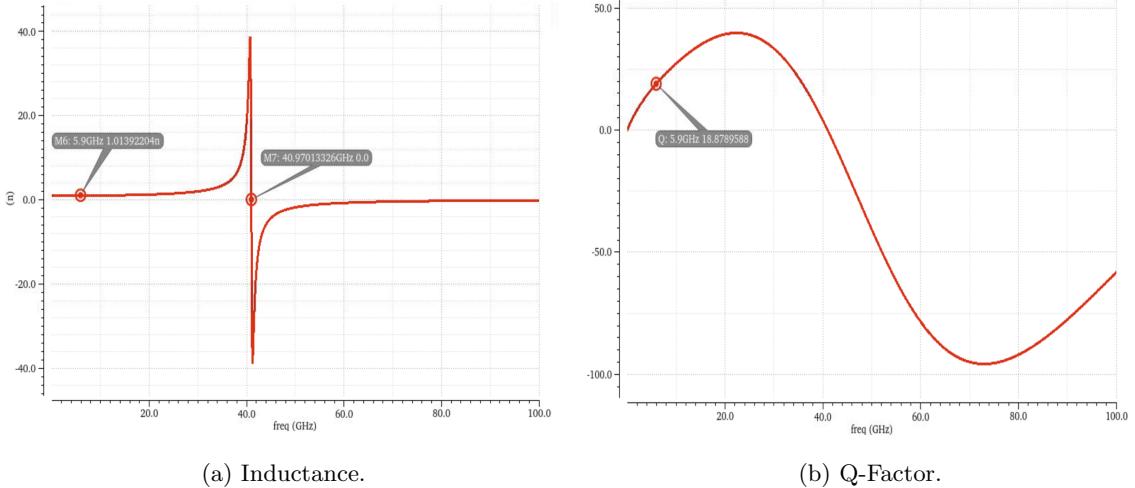


Figure 15: Inductance and Q-factor vs. frequency: center tapped differential octagonal inductor.

From Fig. 15a, the self-resonant frequency can be estimated from the point where $L(f) = 0$. This occurs at $f_{\text{SRF}} = 40.97 \text{ GHz}$. Using the low-frequency value of $L_0 = 1.008 \text{ nH}$, this leads to an equivalent parallel capacitance of

$$C_p = \frac{1}{(2\pi f_{\text{SRF}})^2 \cdot L_0} = 93.97 \text{ fF}$$

4.2.4 Common Mode Stability

The half-circuit of the differential PA in Fig. 8 has potentially unstable behavior if not addressed. In particular, the common-mode of the output stage sees a purely inductive load without any extra output

resistance, leading to potentially a negative input resistance and thus unstable behavior [6]. To remedy this, resistor R_3 is added to the gate nodes of the cascode output stage in order dampen the resonances on the supply bias line that appear at the gate bias points. Resistor R_2 is also added at the input to further degenerate the common-mode gain, improving PA stability ². Without these resistors in place, the PA design was unable to meet the K -factor stability requirements.

4.2.5 Second Harmonic Termination

The differential topology turns even order nonlinearities into a common-mode signal for both polarities in the output stage, thus leading to even order cancellation by differential symmetry. That being said, non-idealities in the circuit can lead to the creation of second order non-linear distortions. From Fig. 8, the common nodes at the sources of M_0/M_1 and gates of M_2/M_3 create a virtual ground at the odd harmonics of the PA, but not the even harmonics. In a real device, asymmetries within the circuit and non-zero impedance conditions at these nodes can lead to higher second harmonic levels. To remedy the second harmonic generation by the PA, the impedance at the common-mode nodes can be engineered to terminate the harmonic. The harmonic trap can be placed at different points in the PA depending on what the circuit allows, but the most improvement to $HD2$ is achieved by terminating the second-harmonic currents at the output drain nodes of the cascode transistors M_2 and M_3 .

Placing a second harmonic trap at both drains implies two different LC circuits, occupying significant die area and also changing the PA output impedance. A more elegant approach is to use the symmetry of the output stage in order to terminate the second harmonic [8]. We utilize a harmonic trap at the center tap of X_1 by inductor L_2 in series with the leakage inductance of the transformer, and capacitor C_6 . This simplifies the footprint of the trap, and also does not disturb the differential output impedance of the PA which has already been optimized based on load-pull for PAE and output power. With knowledge of the primary inductance L_{pri} and secondary inductance L_{sec} along with the coupling coefficient between the two, the leakage model for the transformer may be used to account for the inductance that the common-mode path sees in order to relax the design of the trap.

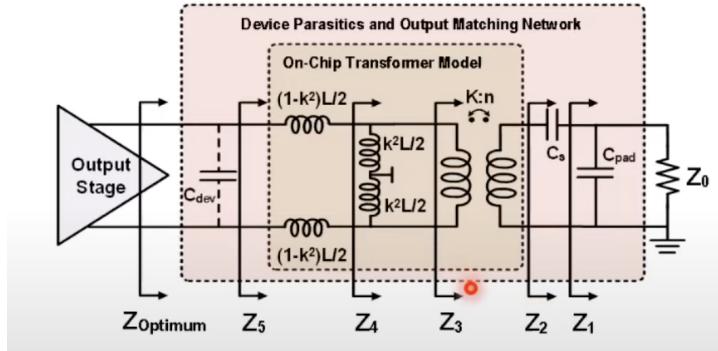


Figure 16: Differential PA with an output transformer matching network.

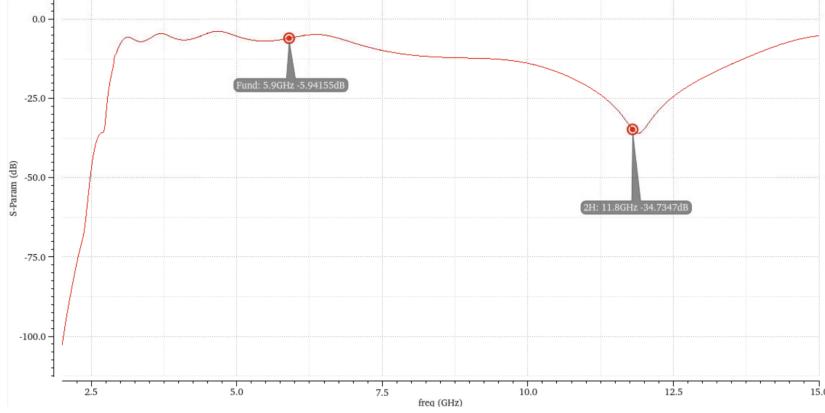
The output PA in the final design has $L_{pri} = 1.9$ nH, $L_{sec} = 2.1$ nH, with a coupling coefficient $k = 0.85$ between the two. The common-mode inductance is thus:

$$L_{CM} = \frac{L_{pri}}{2} - k^2 \cdot \frac{L_{pri}}{2} = 135 \text{ pH} \quad (5)$$

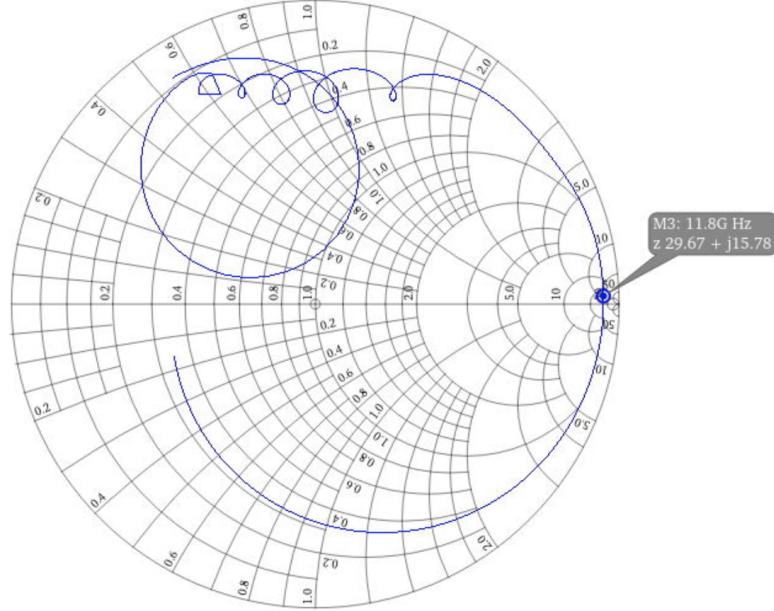
This impedance is small and will be overpowered by the impedance of the supply line itself. To better control the second harmonic termination, a dedicated 1 nH inductor L_2 is added for the harmonic trap.

²The cascode structure also improves stability by increasing input-to-output isolation

Accounting for L_2 , the common-mode inductance, and the parasitic inductance of the supply line leads to a trapping capacitance around 0.15 pF. The actual capacitor, $C_6 = 0.14$ pF was tuned via parameter sweeps to maximize common-mode rejection of the second harmonic signal when exciting the output transformer X_1 in common mode as shown in Fig. 17.



(a) Insertion loss measured from a common-mode excitation at X_1 and the resulting response at the antenna port; diplexer, bondwires, and package parasitics accounted for.



(b) Common-mode input impedance looking into the output transformer with a trap placed at $2 \cdot f_0 = 11.8$ GHz.

Figure 17: Second harmonic rejection by notching the second harmonic common-mode response.

Given that the final PA has its peak PAE close to the maximum input power of 4 dBm and also the IP1dB compression point, the second harmonic signal level was significant before adding the trap. Without the trap, the $HD2$ was observed to be around -34 dBc, while the trap provided a 5 dB improvement.

The series planar footprint of the single-ended series 1 nH inductor L_2 added for the harmonic trap

is shown in Fig. 18, along with the EMX extracted inductance and Q-factor in Fig. 19

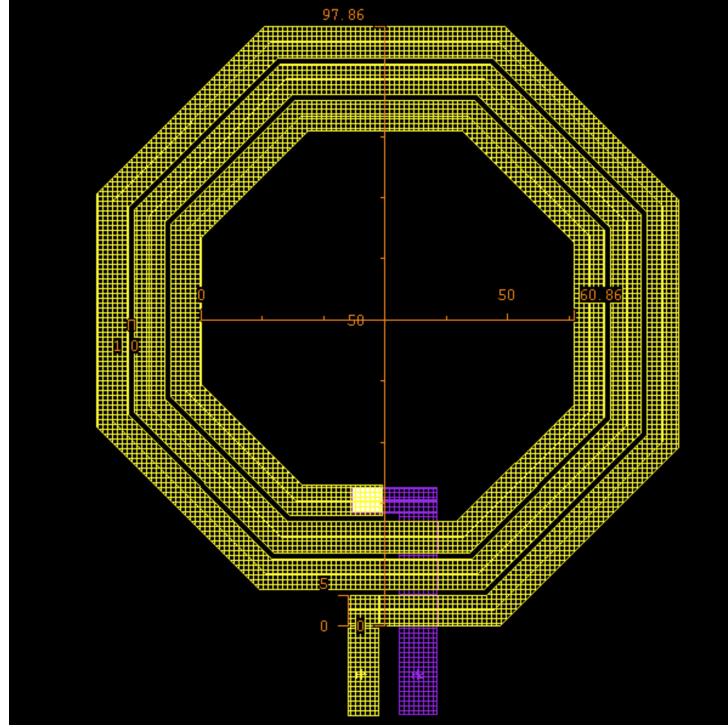


Figure 18: 5.9 GHz single-ended inductor. $s = 1 \mu\text{m}$, $d_{\text{out}} = 97.86 \mu\text{m}$, $d_{\text{in}} = 60.86 \mu\text{m}$, $W = 5 \mu\text{m}$, $n = 3$.

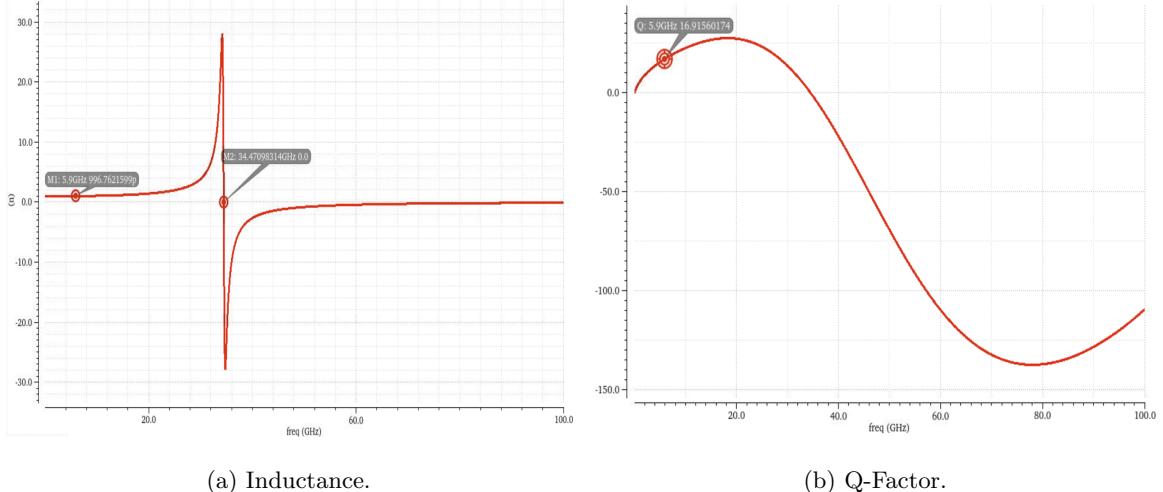


Figure 19: Inductance and Q-factor vs. frequency: singled-ended octagonal inductor.

From Fig. 19a, the self-resonant frequency can be estimated from the point where $L(f) = 0$. This occurs at $f_{\text{SRF}} = 34.47 \text{ GHz}$. Using the low-frequency value of $L_0 = 1.002 \text{ nH}$, this leads to an equivalent parallel capacitance of

$$C_p = \frac{1}{(2\pi f_{\text{SRF}})^2 \cdot L_0} = 133.6 \text{ fF}$$

4.2.6 Analog Pre-distortion

In class-AB CMOS PAs, AM-PM distortion is a major contributor to PA nonlinearity and EVM³ degradation. The main cause of this AM-PM nonlinearity is due to the nonlinear behavior of the input NMOS common-source stage $C_{gs,n}$ as a function of the applied bias voltage [9]. This behavior can be observed by the NMOS gate capacitance variation as a function of the applied V_{GS} as shown in Fig. 20:

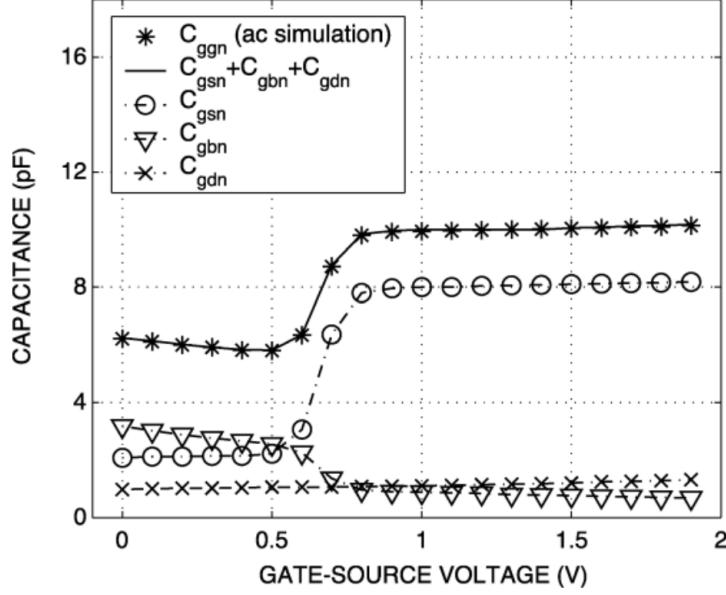


Figure 20: Behavior of $0.5 \mu\text{m}$ NMOS gate capacitance as a function of gate-to-source voltage for a fixed drain-to-source voltage.

As the input signal swing increases, the device input-capacitance can steeply change depending on where the PA is biased. That is, AM-PM distortion is generated by the nonlinearity of the C_{gs} as the input amplitude drive non-linearly dictates an output phase shift. For the final design, the bias point is chosen to be class-AB at a nominal $V_{GS} = 0.34$ V where this is a problem and leads to degradation of EVM. To reduce AM-PM distortion of the class-AB PA, a varactor-based capacitance compensation is used at the input to the common source stage at both M_0 and M_1 . This is also referred to as analog-predistortion, as it linearizes the PA output response against this effect. A digital based linearization approach (digital predistortion) would lump effects like C_{gs} non-linearity into its model.

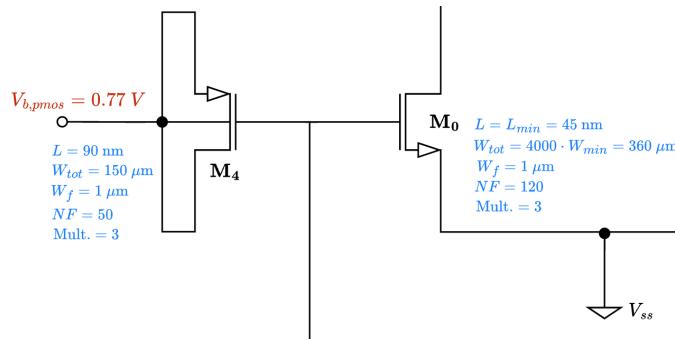


Figure 21: C_{gs} nonlinearity compensation via a PMOS varactor cell at the input of each differential input NMOS.

³Refer to Sect. 4.5.

The PMOS varactors M_4 and M_5 are reverse-biased and sized in order to achieve a linearizing effect against the NMOS C_{gs} . The linearized response is shown in Fig. 22.

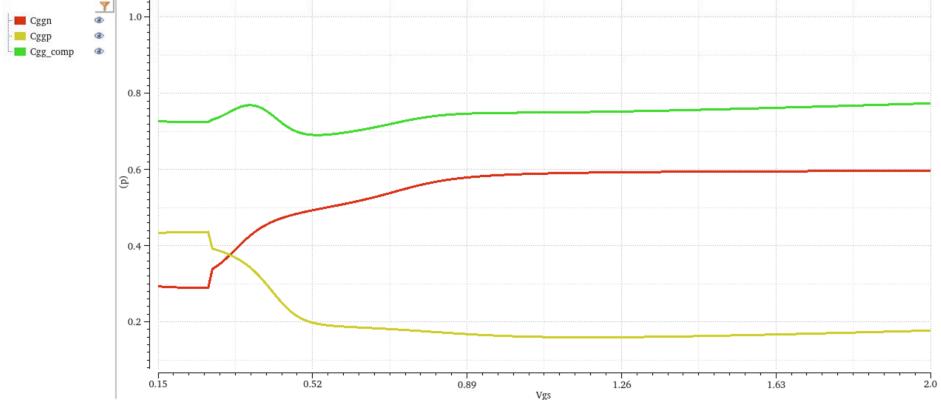


Figure 22: C_{gs} nonlinearity compensation via a PMOS varactor cell at the input of each differential input NMOS.

It is evident from Fig. 22 that the PA bias point operates along a steeply varying C_{gs} slope, indicating poor AM-PM performance. Adding this varactor based compensation cell improved the OIP3 by around 3 dB, which is a significant amount for a PA operating in the compressed domain.

4.3 Simulation Results

The following section will display each PA key-performance indicator (KPI) in detail based on the design specifications. To reiterate, the achieved performance of the final PA design is highlighted in Fig. 23.

Block	Parameter	Design Specifications: Milestone 3	Notes	Achieved: Milestone 3
PA	Center Frequency	5.9 GHz	Channel BW: 20 MHz	5.9 GHz
	Output Power	> 15 dBm		18.03 dBm
	Load Impedance	50 Ω		50 Ω
	Input Power	4 dBm	Max	4 dBm
	Input Source Impedance	50 Ω		50 Ω
	Peak PAE	> 20 %	Center frequency	43.50%
	OP1dB	> 11 dBm		18.21 dBm
	HD2	< -35 dBc	Center frequency, w/ 15 dBm Pout	-39.8 dBc
	OIP3	> 21 dbm	Center frequency	24.75 dBm
	ACPR	-	64 QAM, 802.11n (MCS5) Pin = -4 dBm	Upper: -22.46 dB Lower: -21.93 dB
	EVM	-	64 QAM, 802.11n (MCS5) Pin ∈ [-15 dBm, -10 dBm, -4 dBm]	Pin @ -15 dBm: 2.87% Pin @ -10 dBm: 9.15% Pin @ -4 dBm: 13.46%
	Stability Factor: In-Band	> 1	Pin ∈ [-10 dBm, 4 dBm] f ∈ [2.9 GHz, 8.9 GHz]	✓
	Stability Factor: Out-of-Band	> 1	Pin = -10 dBm f ∈ [0.2 GHz, 20 GHz]	✓
	V_{dd}	1.8 V		1.8 V
	FOM_PA	(PAE_max)*(A+B+C)	PAE_max at 5.9 GHz A = Psat - 14 dBm B = (-HD2) - 35 dBc @ Psat C = OIP3 - 21 dBm Psat = min{OP1dB + 4 dB, Pout,max for Pin < 4 dBm}	547

Figure 23: PA achieved performance.

4.3.1 Output Power, PAE, & P1dB

From Fig. 24, the achieved P_{out} and PAE at max input power is 18.02 dBm and 43.5%, respectively. Additionally, the saturated output power is 18.48 dBm. The P_{out} observed at a 10 dB power backoff (PBO) from the IP1dB point is 13.9 dBm, with a PAE of 23.84%.

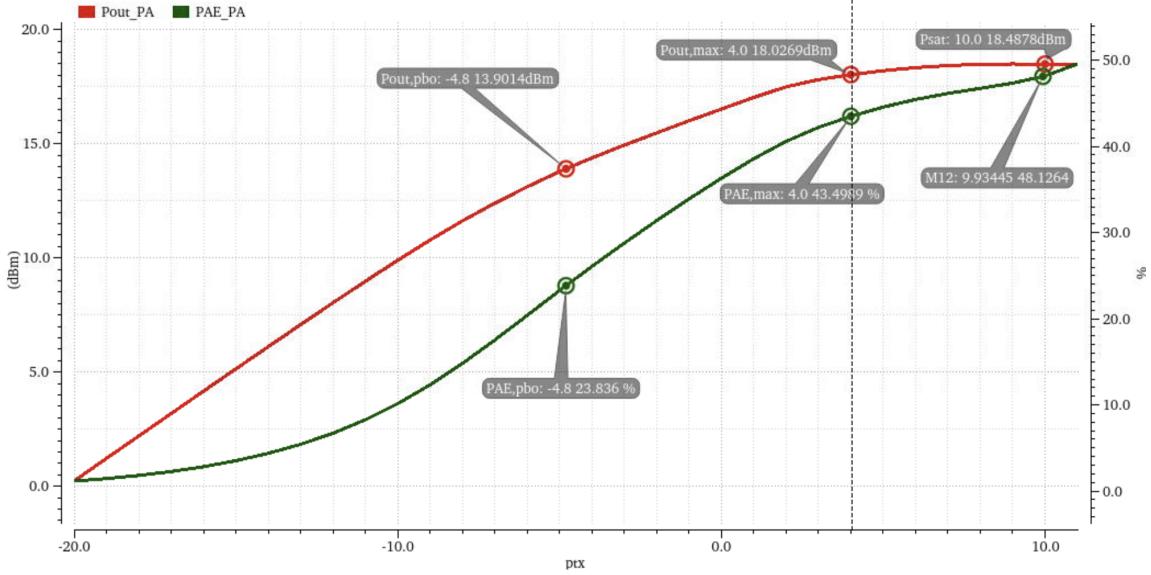


Figure 24: P_{out} , PAE, and P1dB: $f_0 = 5.9$ GHz.

4.3.2 Stability

Although only contextual stability was required for the PA, the final design was verified to be unconditionally stable over 0.2 GHz to 20 GHz for $P_{tx} \in [-12 \text{ dBm}, +4 \text{ dBm}]$.

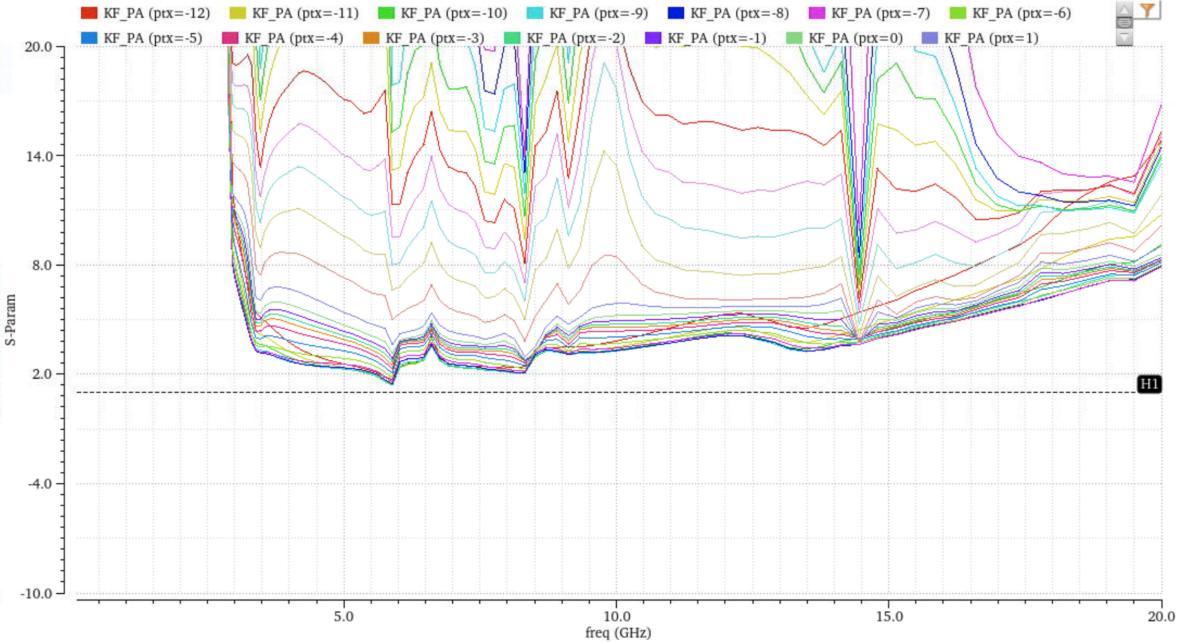


Figure 25: PA stability: 0.2 GHz to 20 GHz, $P_{tx} \in [-12 \text{ dBm}, +4 \text{ dBm}]$.

4.3.3 Linearity: OIP3

From the two-tone test shown in Fig. 26, the output referred third order intercept point (OIP3) under maximum input power conditions of 4 dBm for each tone can be calculated as:

$$\begin{aligned} \text{OIP3} &= P_{\text{fund},\text{low}} + \frac{1}{2} (P_{\text{fund},\text{low}} - P_{\text{im3,low}}) \\ &= 14.91 \text{ dBm} + \frac{1}{2} (14.91 \text{ dBm} - (-6.01 \text{ dBm})) \\ &= 25.36 \text{ dBm} \end{aligned}$$

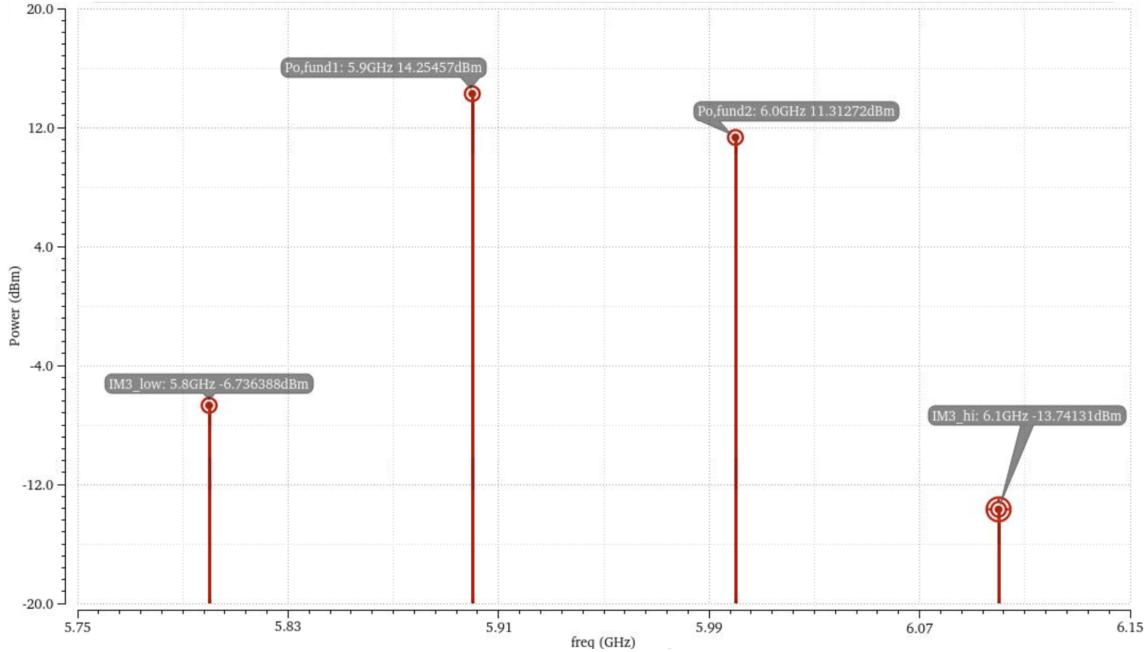


Figure 26: PA OIP3, $f_{tx,1} = 5.9$ GHz, $f_{tx,2} = 6$ GHz, $P_{tx,1} = P_{tx,2} = 4$ dBm.

4.3.4 Second Harmonic Distortion: HD2

From Fig. 27, the second harmonic distortion can be observed as:

$$\begin{aligned} \text{HD2} &= P_{2H} - P_{\text{fund}} \\ &= -35.57 \text{ dBm} - 18.25 \text{ dBm} \\ &= -53.83 \text{ dBc} \end{aligned}$$

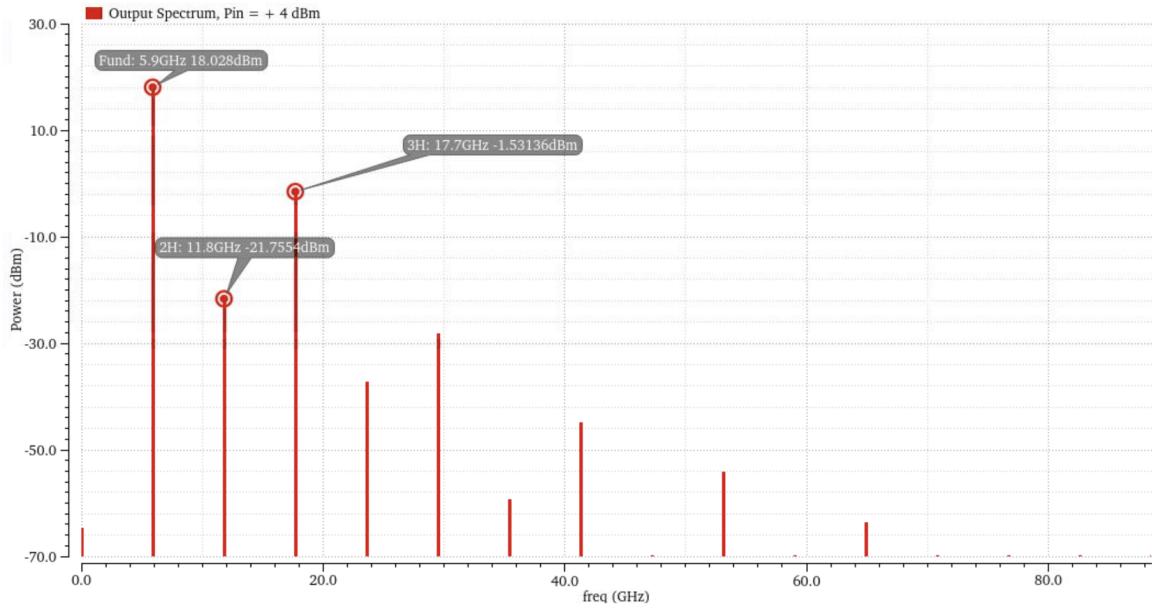


Figure 27: PA output spectrum, $f_{tx} = 5.9$ GHz, $P_{tx} = 4$ dBm.

Note the the second-harmonic trap circuit described in Section 4.4.2 improves HD2 by around 5 dB in the max input power case.

4.4 ACPR and EVM

To qualify the non-linearity of the PA, the Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM) are measured when driving the PA with a IEEE 802.11 MCS5 64-QAM OFDM signal having a channel bandwidth of 20 MHz, roll-off factor of 0.23. Depending on the datarate (and thus MCS) used in a communication link, the PA needs to be operating on a certain region of its operating curve in order to meet spectral emission mask limits determined by the ACPR, or the EVM requirements determined by the MCS used.

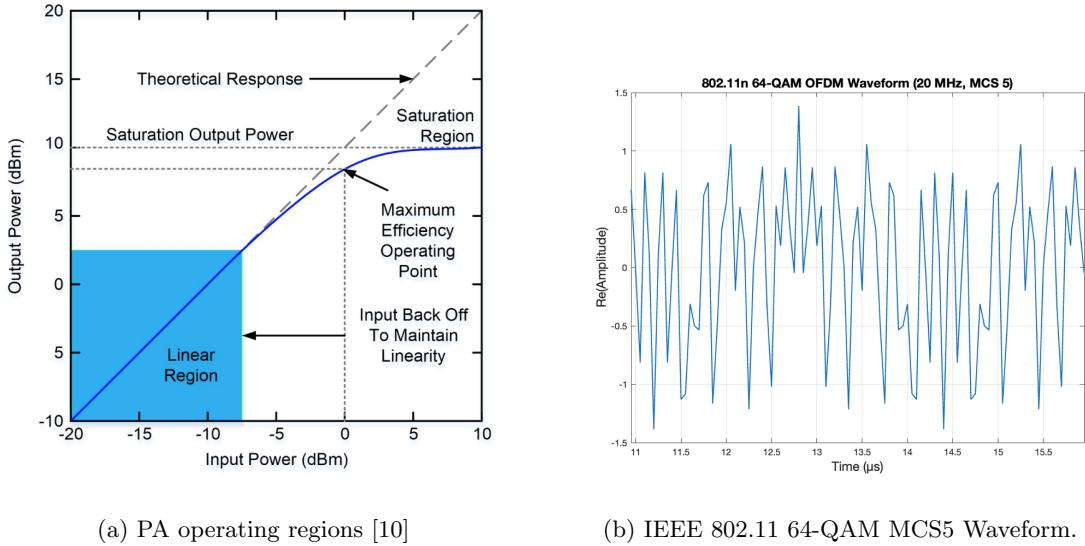


Figure 28: PA operating regions as a function of input power (left). A high PAPR 64 QAM IEEE 802.11n time-domain waveform (right).

4.4.1 ACPR

The ACPR measure of the PA provides insight into the spectral regrowth attributed due to PA non-linearity which causes leakage into interfering bands, potentially desensitizing radios operating on these channels or violating other FCC regulations. The ACPR is compared against a reference PA modeled with ideal blocks having very high linearity in order to get an idea of how our non-idealized PA deteriorates the ACPR, with the ACPR response shown below. The reference PA has an ACPR of -100 dBc on both the upper and lower side-bands.

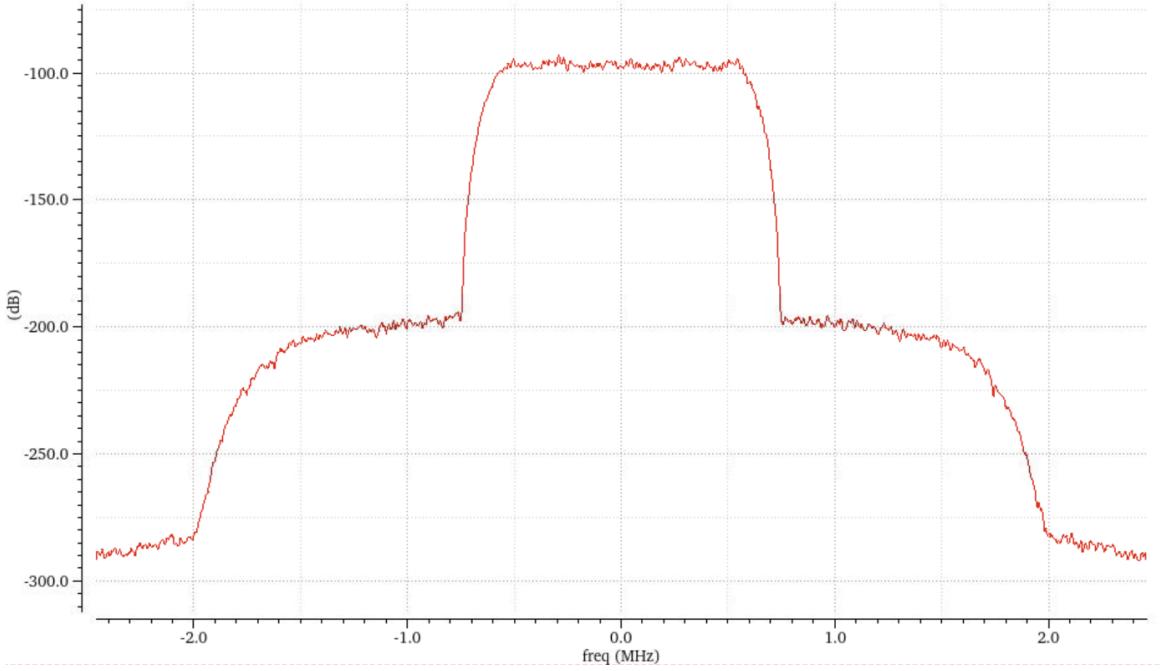


Figure 29: Reference PA ACPR; $P_{tx} = 4$ dBm, $f_0 = 5.9$ GHz.

The implemented PA has the ACPR response shown in Fig. 30, and is shown at max input power $P_{tx} = 4$ dBm, and at $P_{tx} = -4.8$ dBm in red, which is a 10 dB backoff from the IP1dB compression point.

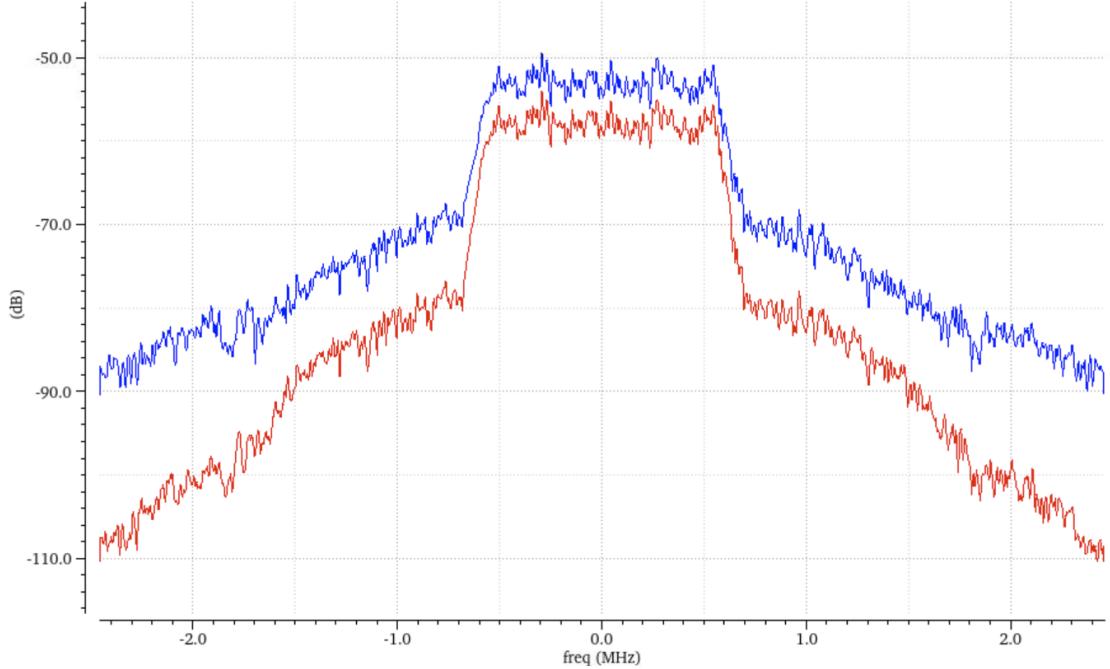


Figure 30: Final PA ACPR; $P_{tx} = 4$ dBm (blue), $P_{tx} = -4.8$ dBm (red), $f_0 = 5.9$ GHz.

We see that for the power back-off case, the upper sideband has an ACPR of -22.46 dBc, and the lower sideband has an ACPR of -21.93 dBc. For the max input power case, the upper sideband has an

ACPR of -17.54 dBc, and the lower sideband has an ACPR of -16.95 dBc. As expected, the ACPR is significantly worse during high input powers close to compression.

4.4.2 EVM

The EVM measure is used to quantify the performance of a system having a complex modulation scheme involving the phase, or amplitude/phase. Due to nonlinearities in the PA, symbols occupying a target location on the IQ constellation for the modulation scheme may be displaced. The shape of the observed distortion on the IQ constellation can give insight into which type of non-linearity is degrading the EVM. The primary sources of EVM degradation are: AM-AM distortion, AM-PM distortion, memory effects, inter-modulation distortion, and harmonic distortion.

The EVM performance of the PA must be guaranteed for certain modulation schemes in order to guarantee a certain bit-error rate performance on the link. Below is a sweep of the EVM for the final PA design versus the input power using the same 802.11 reference signal as before:

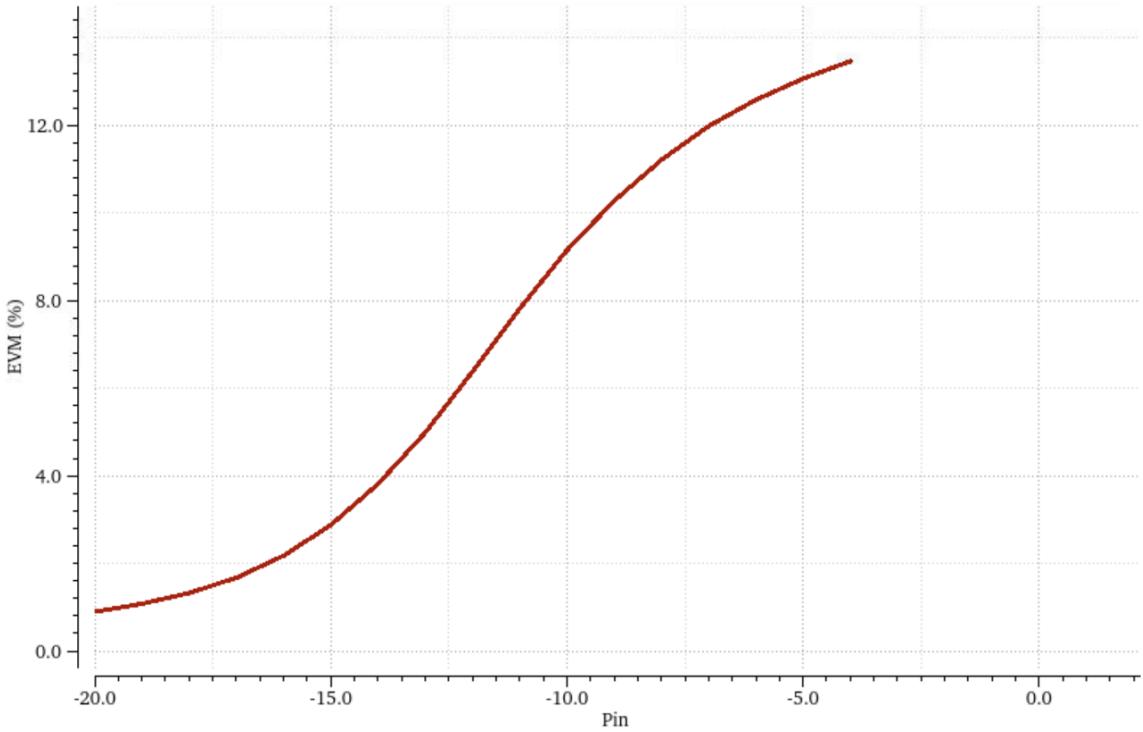
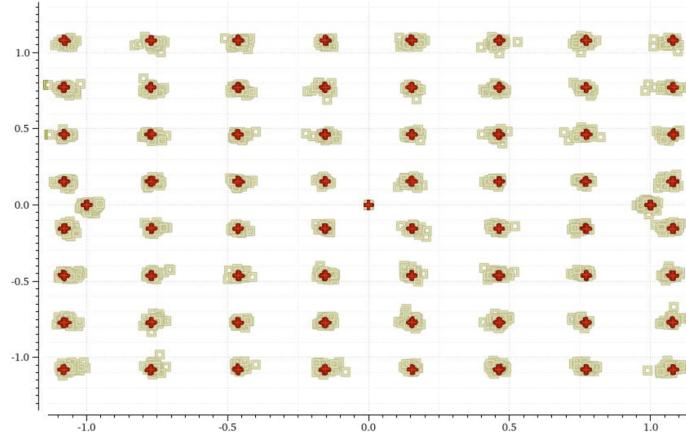
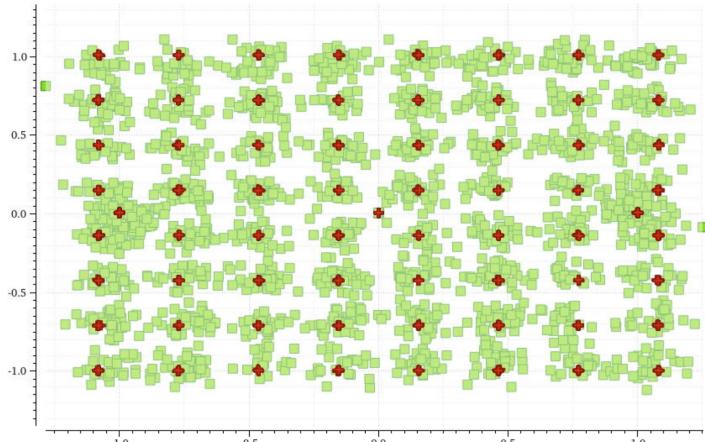


Figure 31: EVM vs. input power for a IEEE 802.11 64-QAM MCS5 input waveform.

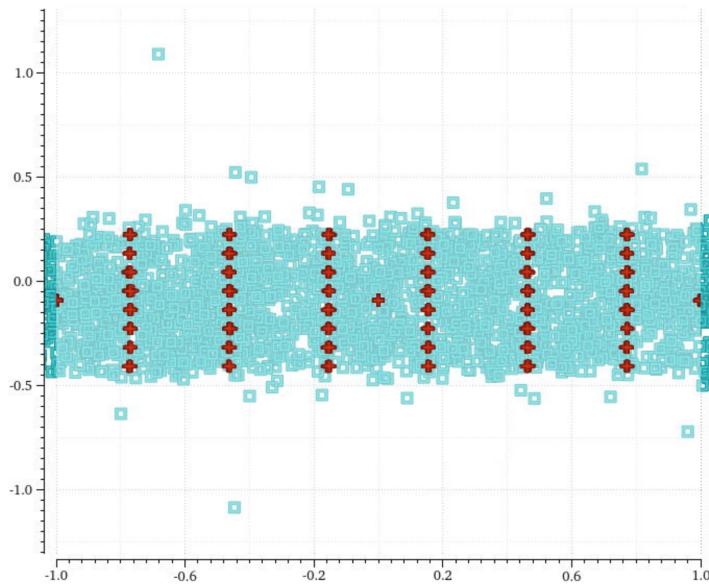
A curve like this in combination with the PA transfer characteristics in Fig. 24 can inform the modem how much power-back-off is required for the PA to meet the EVM requirements of a selected MCS scheme. In Fig. 32, the IQ diagram of the transmitted 64 QAM signal is displayed for different input power drive levels along with the associated EVM measured over 40 different OFDM symbols. From Fig. 32c, it can be see that significant AM-AM distortion is shrinking the constellation, while IMD is blurring the constellation points.



(a) $P_{tx} = -15$ dBm, EVM = 2.87%



(b) $P_{tx} = -10$ dBm, EVM = 9.14%



(c) $P_{tx} = -4$ dBm, EVM = 13.46%

Figure 32: 64-QAM constellation diagrams for different input power levels plotted against an ideal reference PA's constellation; EVM measured over 40 OFDM symbols.

4.5 PA Area Budget

The PA's die area consumption is found in Tab 2, which only considers inductive and capacitive passives (transformers, resistors, and active devices are not included).

Type	Label	Die Area	Percentage of Allowed Die Area
Inductor	L_1	$31,300 \mu m^2$	3.0%
	L_2	$31,300 \mu m^2$	3.0%
	Total	$62,600 \mu m^2$	6.0%
Capacitor	C_0	$2,000 \mu m^2$	0.2%
	C_1	$2,000 \mu m^2$	0.2%
	C_2	$19,600 \mu m^2$	1.9%
	C_3	$19,600 \mu m^2$	1.9%
	C_4	$900 \mu m^2$	0.09%
	C_5	$1,600 \mu m^2$	0.2%
	C_6	$280 \mu m^2$	0.03%
	C_{B1}	$200,000 \mu m^2$	19%
	C_{B2}	$48,400 \mu m^2$	4.6%
	C_{B3}	$19,900 \mu m^2$	1.9%
	Total	$314,000 \mu m^2$	30%
Total Used	-	$377,000 \mu m^2$	36%

Table 2: PA die area summary.

5 Low Noise Amplifier

5.1 Topology Analysis

We chose the cascode common source stage with inductive degeneration as our topology for the LNA due to its ability to achieve NF well below 3 dB. There are three inductors employed in this topology (not including the output matching network) as depicted in Fig. 33: the degeneration inductor at the source of the g_m device (L_1), the gate inductor at the gate of the g_m device (L_G), and the load inductor at the drain of the cascode device (L_D). L_1 and L_G work together to resonate out C_{pad} and C_{GS1} so that the circuit input impedance is ideally purely real at the center frequency of $f_0 = 2.4 \text{ GHz}$. The real part of the input impedance, given by $\text{Real}[Z_{in}] = \frac{g_{m1}L_1}{C_{GS1}}$, is chosen to be well matched to R_S of 50Ω by selecting the proper M_1 device operating point for the chosen L_1 .

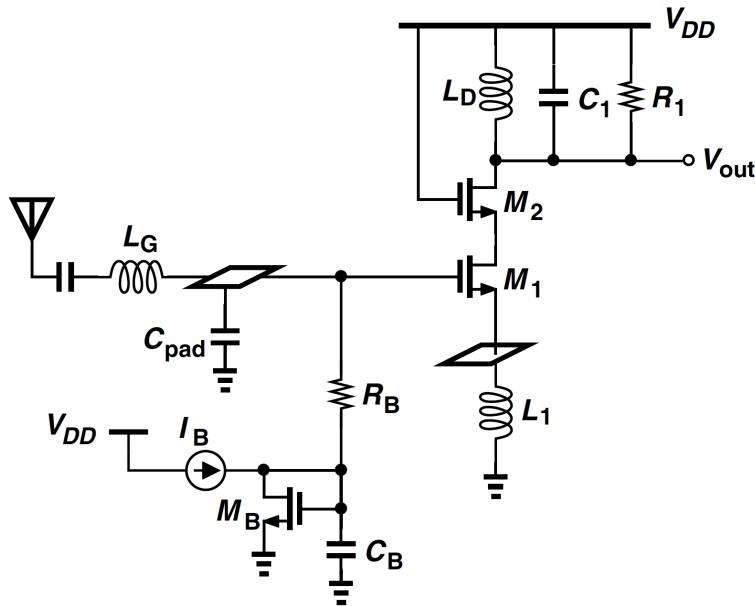


Figure 33: Cascode common source stage with inductive degeneration, courtesy of Razavi [6].

L_1 is typically implemented with a downbond to the package ground since this inductance automatically comes with the physical implementation of the circuit in a bondwire packaging process, meaning that $L_1 \approx 1 \text{ nH}$. Depending on the operating frequency, L_G may also be implemented just with a bondwire, but at the low operating frequency of 2.4 GHz an additional on-chip inductor is all but needed to achieve good input matching for reasonable power consumption levels. Additional capacitance can be added in parallel with the intrinsic C_{GS1} to reduce the L_G value needed to achieve resonance at f_0 . However, this lowers the real part input impedance meaning that g_{m1} needs to increase without adding additional C_{GS1} (increase V_{GS1} at constant device width), which increases LNA power consumption (all assuming that L_1 is fixed). Here we find an important tradeoff for the design between power consumption and passives area: holding the input match quality and L_1 constant, the lower the power consumption is, the larger the L_G value and area needed to achieve resonance at f_0 .

The cascode device (M_2) minimizes the swing on the drain of the g_m device (M_1) thereby nulling the effects of the miller effected capacitance (C_{GD1}). Perhaps more importantly, the cascode mitigates the negative resistance that otherwise results from the inductive load feedback path through C_{GD1} . These benefits are accepted at the cost of additional noise from the cascode device.

R_B is used to present a bias voltage (generated by diode connected M_B and the reference current source) to the g_m device and is chosen to ensure that the input signal experiences minimal attenuation without adding too much thermal noise. A DC blocking capacitor is used at the input to isolate the diplexer from the DC bias voltage and a capacitor, C_B , is introduced so that the input signal is low-pass filtered out of the bias network. L_D contributes both parasitic capacitance, C_1 , and resistance, R_1 , at the output node and is chosen so that C_1 in parallel with C_{DD} from the cascode device resonates with L_D at f_0 , leaving just R_1 as the load. Additional capacitance can be added in parallel with C_1 to reduce the L_D value needed to achieve resonance at f_0 , which is often a favorable tradeoff since large on-chip inductors are more troublesome than capacitors. However, L_D cannot be made too small since its parasitic R_1 needs to be roughly in the $k\Omega$ range to yield an acceptable LNA gain (given to first order by $\frac{V_{out}}{V_{in}} = \frac{R_1}{2L_1\omega_0}$) for our f_0 and L_1 . Finally, a matching network (not shown) is employed to match down to the R_L of $50\ \Omega$. A DC blocking capacitor is used at the output of the LNA so that only the AC signal drives the load, saving substantial power.

5.2 Sizing Approach and Calculations

The two following equations, courtesy of Razavi, are used to determine a rough device sizing and operating point that is further refined through simulations. These equations ensure that there is a good input match to $50\ \Omega$ at f_0 .

$$\omega_0^2 = \frac{1}{(L_G + L_1)(C_{GS1} + C_{pad})} \quad (6)$$

$$R_S = \omega_T L_1 \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}} \right)^2 \quad (7)$$

Reasonable values of L_1 and L_G are assumed initially, and C_{pad} and ω_0 are known. Eq. (6) allows us to solve for C_{GS1} , which is then used in Eq. (7) to find ω_T and g_m . While there are many combinations of g_m and f_T that are possible, there are few that are at a desirable operating point (reasonable device bias current and width). The technology models from Milestone 1 are used to check whether a reasonable W_1 value exists that satisfies the g_m and f_T requirements simultaneously. The obtained values are sensitive to the assumed L_1 and L_G values, so a simple script is used to calculate values to speed up the process.

For Milestone 3, the objective is to maximize FOM_{LNA} given by Eq. 8 at $f_0 = 2.4\ GHz$ while still meeting the general specifications, noting that $G_{T,LNA}$ is the LNA transducer power gain and P_{LNA} is the LNA power consumption.

$$FOM_{LNA} = \frac{G_{T,LNA}}{P_{LNA}^2} \quad (8)$$

From Eq. (8) it is seen that FOM_{LNA} weights P_{LNA} more highly than $G_{T,LNA}$ due to its quadratic dependence, indicating that operating at low power consumption and moderate gain is almost certainly more optimal than operating at high power consumption and high gain, qualitatively speaking. Our Milestone 2 LNA (not designed with FOM_{LNA} in mind) requires a large bias current of around $2\ mA$ whilst offering a substantial $G_T \approx 22\ dB$, and yields a $FOM_{LNA} = 38.4 \times 10^6\ W^{-2}$ as a baseline on which to improve.

Maximizing FOM_{LNA} qualitatively relies on achieving more $G_{T,LNA}$ for less cost of P_{LNA} . Increasing the LNA gain or improving the input and output match are both valid ways of extracting more $G_{T,LNA}$. To first order the LNA voltage gain is given by $\frac{V_{out}}{V_{in}} = \frac{R_1}{2L_1\omega_0}$ and appears to be independent of g_m (though we intuitively expect gain to decrease with decreasing g_m). L_1 is constrained by the goal of

using a bondwire ($L_1 \approx 1 \text{ nH}$), ω_0 is given, and R_1 cannot be made too large because it would either require too large a Q-factor from L_D , require an excessively large area L_D , or require a matching network with excessively large components to match down to 50Ω .

As mentioned in Section 5.1, a major design tradeoff for this LNA is between passives area and power consumption. Since $\text{Real}[Z_{in}] = \frac{g_{m1}L_1}{C_{GS1}}$ is desired to be 50Ω , power consumption must be reduced in a way that maintains the same quality of input match. Lowering I_{bias} by reducing W_1 in order to save power consumption to first order reduces g_{m1} at the same rate as C_{GS1} , thereby preserving the real part input match. However, the lower C_{GS1} value now requires a larger L_G in order to still resonate at f_0 . Reducing power consumption is only practical up to the point that the required L_G value becomes excessively large.

With these boundary conditions in mind, we can size the components for the simulation starting point. For $L_1 \approx 1 \text{ nH}$, $f_T \approx 8.0 \text{ GHz}$ is required to match the input real part impedance to 50Ω , noting that the resonance frequency will not be at $f_0 = 2.4 \text{ GHz}$ yet. The NF_{min} vs V_{GS1} technology curve from Milestone 1 showcases that $L_{min} = 45 \text{ nm}$ offers significantly better noise figure compared to longer length devices, achieving good noise performance from $V_{GS1} \approx 0.25 \text{ V}$ to $V_{GS1} \approx 0.50 \text{ V}$, so we choose $L_{M1} = 45 \text{ nm}$. Looking at the f_T vs V_{GS1} curve, it is seen that the f_T is too large across this desired V_{GS1} range, indicating that an external capacitor, $C_{GS1,add}$, should be placed in parallel with the intrinsic C_{GS1} to achieve the desired f_T . One could choose a large f_T (large V_{GS1}) and make $C_{GS1,add}$ large to bring the f_T down to the desired value. This would have the nice consequence that the required L_G value to resonate at f_0 would be small, however this approach causes a large power consumption due to the small $\frac{g_m}{I_D}$ ratio. Because we are interested in minimizing power we instead opt for $V_{GS1} \approx 0.30 \text{ V}$, yielding $f_T \approx 45 \text{ GHz}$, $\frac{g_m}{I_D} \approx 19 \frac{\text{S}}{\text{A}}$, and $\frac{I_D}{W} \approx 20 \frac{\mu\text{A}}{\mu\text{m}}$. The weak-moderate inversion region comes with the downside of reduced linearity, so the V_{GS1} bias may need to be increased if the IIP3 specification is an issue.

Next, an upper limit on allowable L_G is decided, somewhat arbitrary, to be 25 nH so as not to waste too much die area. Because the bondwire from the diplexer to the LNA can contribute up to 5 nH of inductance, we plan for $L_{G,on-chip} = 20 \text{ nH}$. By using Eq. (6), we find $C_{GS1,total} = 119 \text{ fF}$. Since $\omega_T = \frac{g_m}{C_{GS1,total}} = 50 \text{ G}\frac{\text{rad}}{\text{s}}$, we find that we need $g_m \approx 6 \text{ mS}$. We also know $\omega_{T,intrinsic} = \frac{g_m}{C_{GS1}} = 283 \text{ G}\frac{\text{rad}}{\text{s}}$, so $C_{GS1} = 21 \text{ fF}$. Knowing $C_{GS1,total}$ and C_{GS1} we find that $C_{GS1,add} \approx 100 \text{ fF}$. From the known g_m and $\frac{g_m}{I_D}$ we find $I_D \approx 310 \mu\text{A}$. From I_D and $\frac{I_D}{W}$ we find $W_1 \approx 15 \mu\text{m}$. The cascode device is chosen to have the same dimensions as the g_m device, since Razavi's analysis shows that the LNA performance is largely insensitive to the cascode sizing [6].

The noise current power of R_B ($\frac{i_R^2}{\Delta f} = \frac{4kT}{R_B}$) flows onto the impedance at the gate of the g_m device and creates a noise voltage power which is then gained by the LNA to the output. To have minimal attenuation of the input signal and to reduce noise, $R_B = 10 \text{ k}\Omega$ is chosen. A $C_B = 10 \text{ pF}$ is added to the bias network to low-pass filter out the input signal from the bias network. The bias network is composed of an ideal $50 \mu\text{A}$ current sink (provided to us) which biases a diode-connected PMOS current mirror, which mirrors the current onto the NMOS M_B . The PMOS current mirror utilizes $L = 180 \text{ nm}$ to improve output resistance, yielding a better current source. The length of M_B is chosen to be the same as the g_m device with a width ratio given by the current ratio between the devices, $\frac{W_B}{W_1} = \frac{I_{bias,B}}{I_{bias,1}} \approx 6$. To block the DC gate bias from the diplexer while not attenuating the input signal substantially at $f_{min} = 2.2 \text{ GHz}$, $C_{in} = 50 \text{ pF}$ is chosen.

The final components to select are at the output of the LNA. As mentioned in Section 5.1, L_D needs to be large enough to produce $R_1 \approx \text{few k}\Omega$ to obtain reasonable gain. Since $R_1 = Q \cdot L_D \cdot \omega$, assuming a high Q of 20 at f_0 , L_D needs to be $L_D \approx 10 \text{ nH}$ to achieve $R_1 \approx 3 \text{ k}\Omega$. The inductor, L_D , needs

to resonate with C_{DD2} from the cascode drain and parasitic capacitance C_1 from L_D at f_0 . Without simulating it is difficult to determine these values, but here we assume $C_1 = 50 \text{ fF}$ and $C_{DD2} = 100 \text{ fF}$. Resonance at f_0 requires $C_{DD,\text{total}} \approx 450 \text{ fF}$, so we need to add $C_{DD,\text{add}} \approx 300 \text{ fF}$. At this point we have everything we need to start simulating, however we may as well estimate an output matching network. Due to the narrow-band nature of the LNA a simple L-match can do the trick. We need to match roughly from $3 \text{ k}\Omega$ to 50Ω at $f_0 = 2.4 \text{ GHz}$ yielding $C_{\text{match}} \approx 180 \text{ pF}$ in parallel with C_1 followed by $L_{\text{match}} \approx 25 \text{ nH}$ in series with the load. Finally, $C_{\text{out}} = 50 \text{ pF}$ is used to AC couple the LNA output onto the load. These initial values were simulated in Cadence Virtuoso and refined to arrive at the final design.

5.3 Passives Design

Of the inductors shown in Fig. 33, L_1 is achieved entirely through a bondwire to TRX GND and 3.5 nH out of the needed 25 nH of L_G is achieved by the bondwire from the diplexer RX output to the LNA input. Thus, the needed on chip inductors are $L_{G,\text{on-chip}} \approx 21.5 \text{ nH}$, $L_D \approx 10 \text{ nH}$, and $L_{\text{match}} \approx 25 \text{ nH}$. A Q-factor of at least 15 is desired, noting that $Q \approx 20$ for L_D is needed to achieve the designed for R_1 value. With target values in mind for the inductors, we laid them out in Cadence and used EMX simulations to extract models for circuit level simulation. In order to conserve area, layouts with smaller outer diameter and larger number of turns is employed.

5.3.1 Gate Inductor

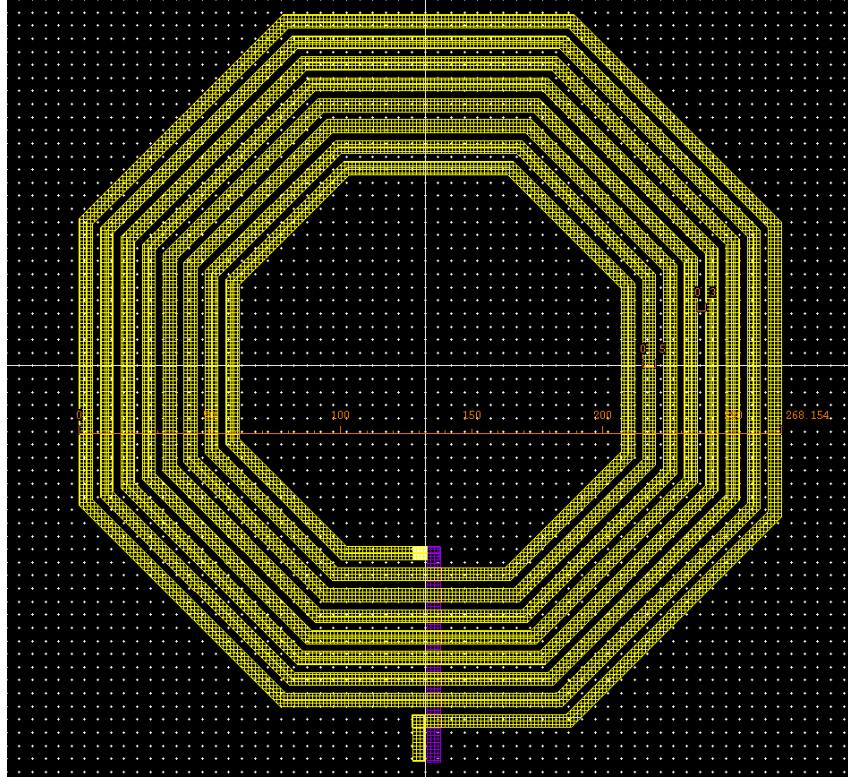


Figure 34: 2.4 GHz single-ended 22 nH inductor. $s = 3 \mu\text{m}$, $d_{\text{out}} = 268 \mu\text{m}$, $W = 5 \mu\text{m}$, $n = 8$.

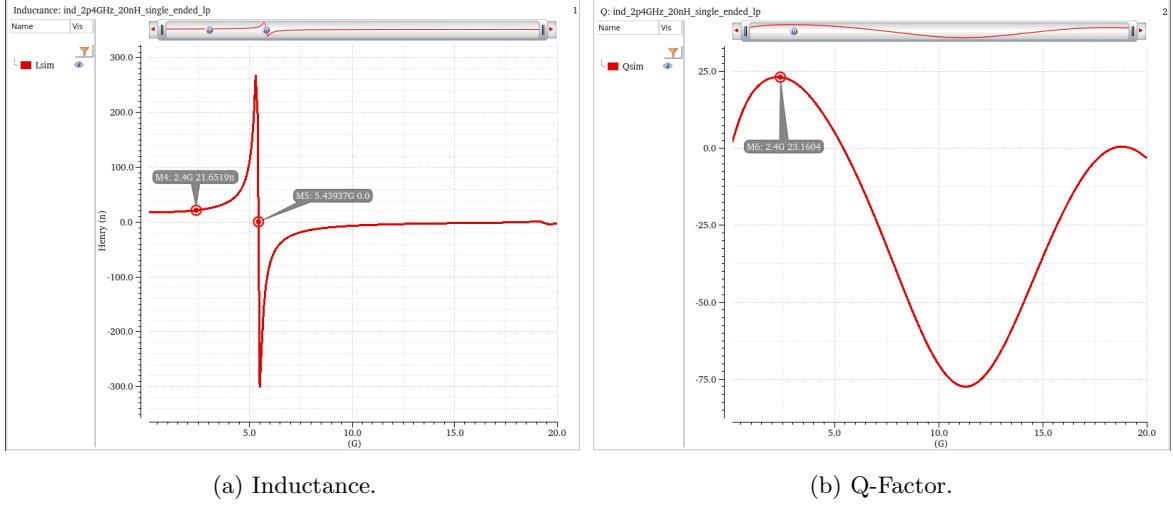


Figure 35: Inductance and Q-factor vs. frequency.

From Fig. 35a, the self-resonant frequency can be estimated from the point where $L(f) = 0$. This occurs roughly at $f_{SRF} = 5.4$ GHz. Using the low-frequency value of $L_0 = 17.5$ nH, this leads to an equivalent parallel capacitance of

$$C_p = \frac{1}{(2\pi f_{SRF})^2 \cdot L_0} = 50 \text{ fF}$$

From Fig. 35b, we find that $Q = 23$ at 2.4 GHz yielding a parallel resistance of

$$R_p = Q \cdot L \cdot \omega = 7.5 \text{ k}\Omega$$

This inductor is used in the input matching network of the LNA.

5.3.2 Drain Inductor

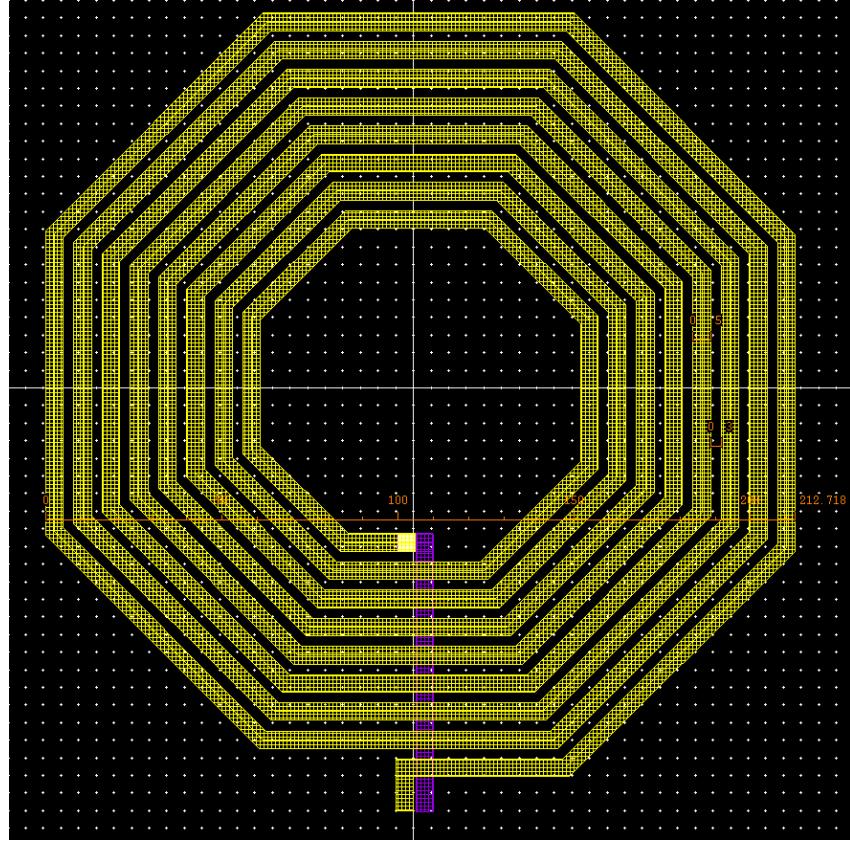


Figure 36: 2.4 GHz single-ended 12 nH inductor. $s = 3 \mu\text{m}$, $d_{\text{out}} = 213 \mu\text{m}$, $W = 5 \mu\text{m}$, $n = 8$.

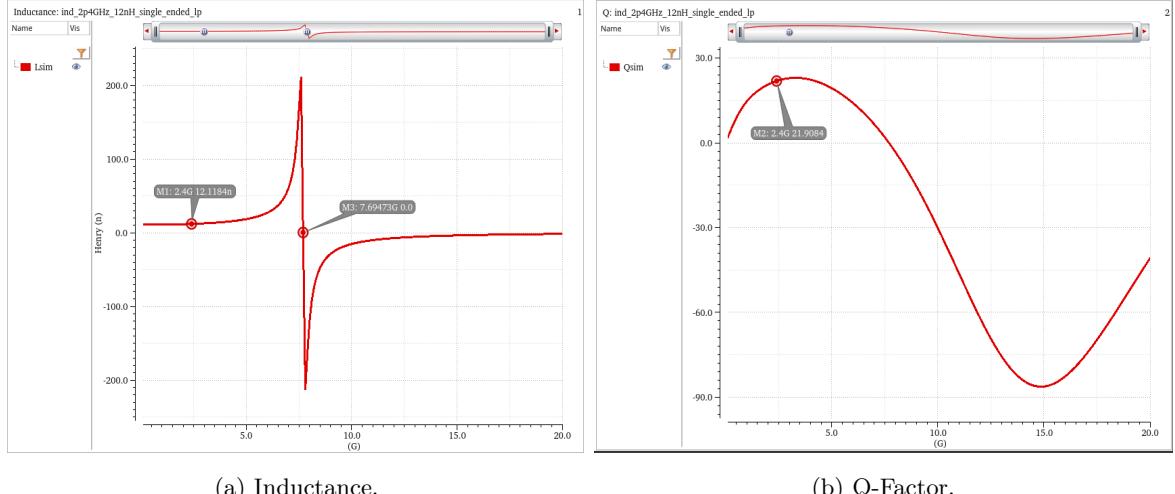


Figure 37: Inductance and Q-factor vs. frequency.

From Fig. 37a, the self-resonant frequency can be estimated from the point where $L(f) = 0$. This occurs roughly at $f_{\text{SRF}} = 7.7 \text{ GHz}$. Using the low-frequency value of $L_0 = 11 \text{ nH}$, this leads to an equivalent parallel capacitance of

$$C_p = \frac{1}{(2\pi f_{\text{SRF}})^2 \cdot L_0} = 39 \text{ fF}$$

From Fig. 37b, we find that $Q = 22$ at 2.4 GHz yielding a parallel resistance of

$$R_p = Q \cdot L \cdot \omega = 4.0 \text{ k}\Omega$$

Notably, R_p serves as the load resistor for the LNA since this inductor is used as an inductive choke to V_{dd} to maximize headroom. The C_p is incorporated into the output matching network without issue.

5.3.3 Output Matching Network Inductor

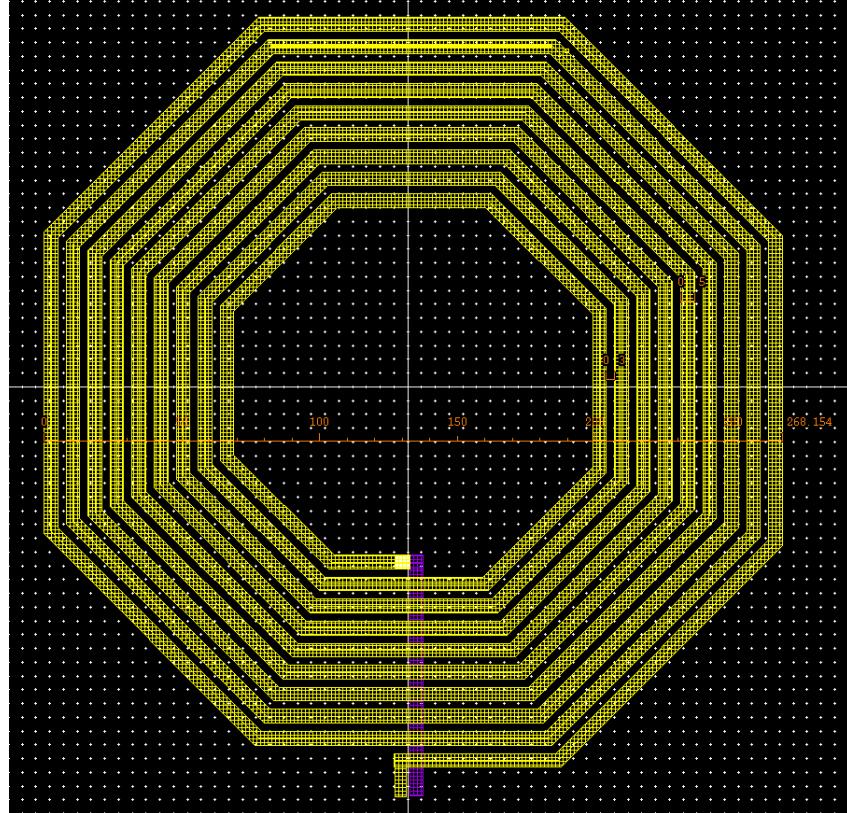


Figure 38: 2.4 GHz single-ended 25 nH inductor. $s = 3 \mu\text{m}$, $d_{\text{out}} = 268 \mu\text{m}$, $W = 5 \mu\text{m}$, $n = 9$.

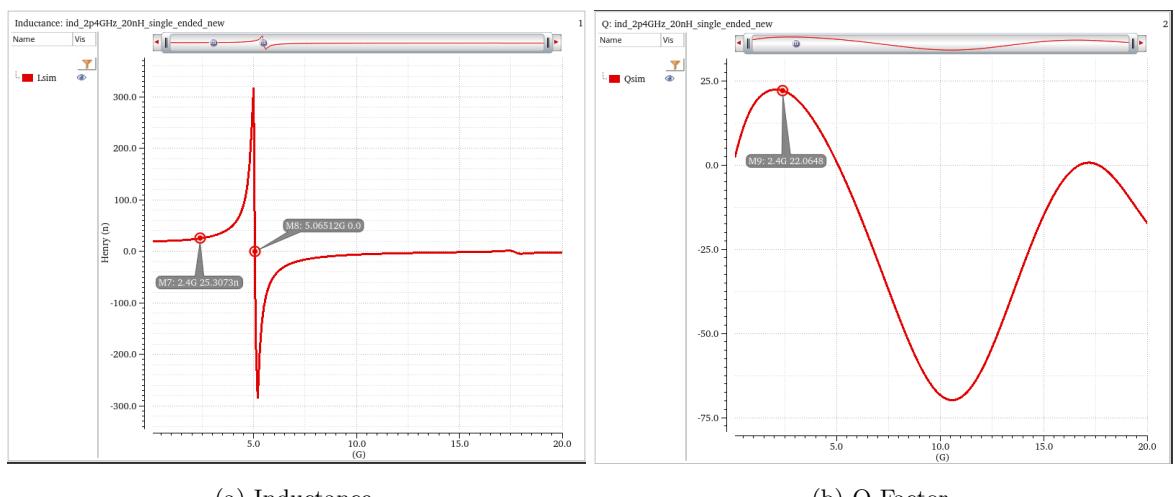


Figure 39: Inductance and Q-factor vs. frequency.

From Fig. 39a, the self-resonant frequency can be estimated from the point where $L(f) = 0$. This occurs roughly at $f_{SRF} = 5.0$ GHz. Using the low-frequency value of $L_0 = 20$ nH, this leads to an equivalent parallel capacitance of

$$C_p = \frac{1}{(2\pi f_{SRF})^2 \cdot L_0} = 51 \text{ fF}$$

From Fig. 39b, we find that $Q = 22$ at 2.4 GHz yielding a parallel resistance of

$$R_p = Q \cdot L \cdot \omega = 8.3 \text{ k}\Omega$$

This inductor is used in the output matching network (L-match) of the LNA.

5.4 Simulation Results

The final design, shown in Fig. 40, includes no ideal power sources, inductors, or capacitors with exception of the reference current source. All the simulation results shown below (with the exception of the standalone NF test) are collected with non-ideal bondwires and with the non-ideal diplexer. Device and MIMCAP sizing, resistance, inductance, and capacitance values, and each device operating point are annotated in Fig. 40.

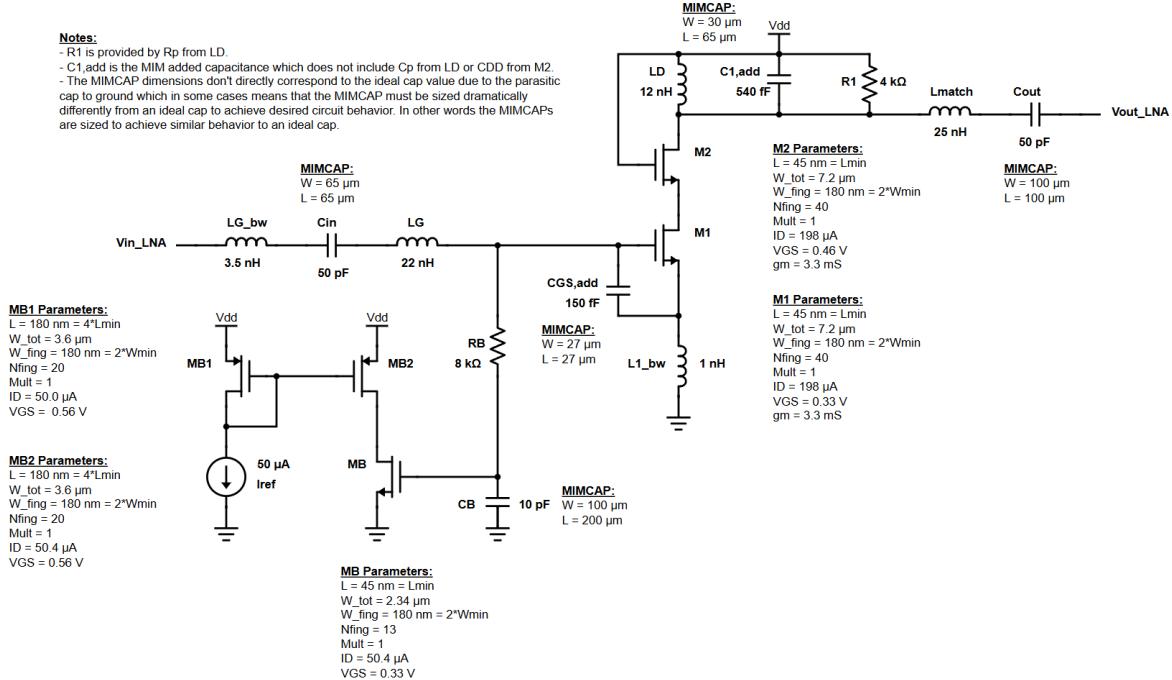


Figure 40: LNA circuit schematic.

Tab. 3 compares the LNA specifications to results achieved from simulation (shown in Fig. 41 - 45). S-parameter, DC, and harmonic balance simulations were run to collect the data shown.

Metric	Specification	Simulation Results	Notes
Input Match (S_{11})	-10 dB	-10.2 dB	At center frequency.
NF (Standalone LNA)	-	2.1 dB	Max across frequency.
NF (TX Off)	3 dB	3.15 dB	Max across frequency.
NF (TX On)	4 dB	6.9 dB	Max across frequency.
IIP3	-23 dBm	-9.9 dBm	At center frequency.
G_T	-	12.6 dB	At center frequency.
P_{LNA}	-	351 μ W	-
FOM_{LNA}	-	$149 \times 10^6 W^{-2}$	At center frequency.

Table 3: LNA achieved simulation results.

Despite the LNA possessing good standalone NF, the diplexer PA-LNA isolation is not sufficient to prevent the PA noise from significantly degrading the LNA NF at the high-end of the frequency band. When a noise summary is conducted, it is found that the PA contributes roughly 45% of the total noise at the output of the LNA at 2.6 GHz. In stark contrast, at 2.2 GHz less than 1% of the total noise at the output of the LNA comes from the PA. The diplexer's own poor matching to 50Ω for the LNA port at 2.6 GHz means that less antenna noise makes it to the LNA, thus requiring lower noise from the PA to hold NF constant. Unfortunately, the PA-LNA isolation is also lowest at 2.6 GHz, meaning that 2.6 GHz is particularly problematic in terms of noise. We look into this further and describe potential solutions in Section 6.

Nonetheless, the design meets all other specifications and offers a significant improvement in FOM_{LNA} compared to Milestone 2, primarily due to the lower power design.

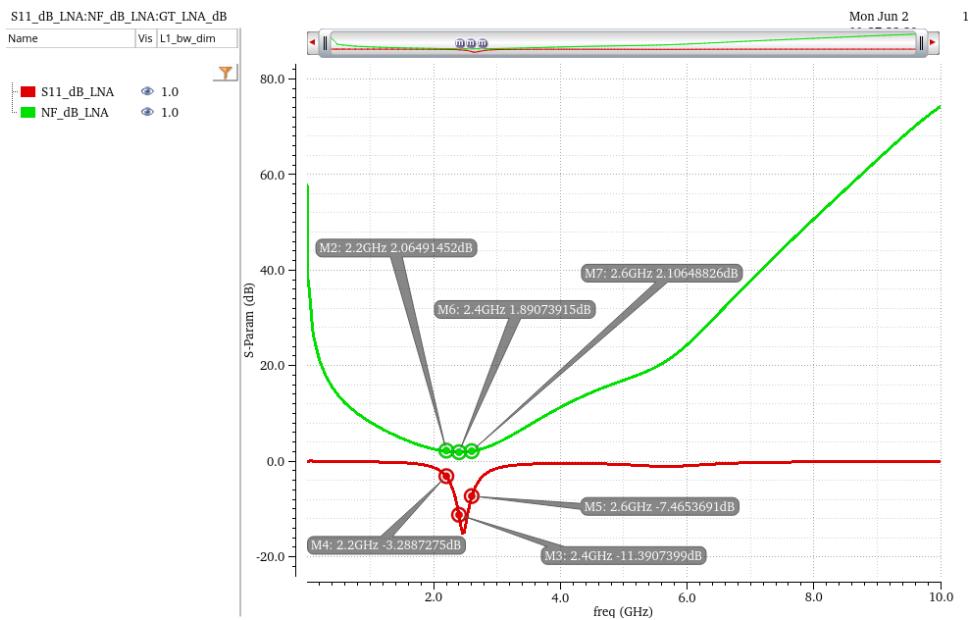


Figure 41: LNA S_{11} and NF simulations (Standalone LNA).

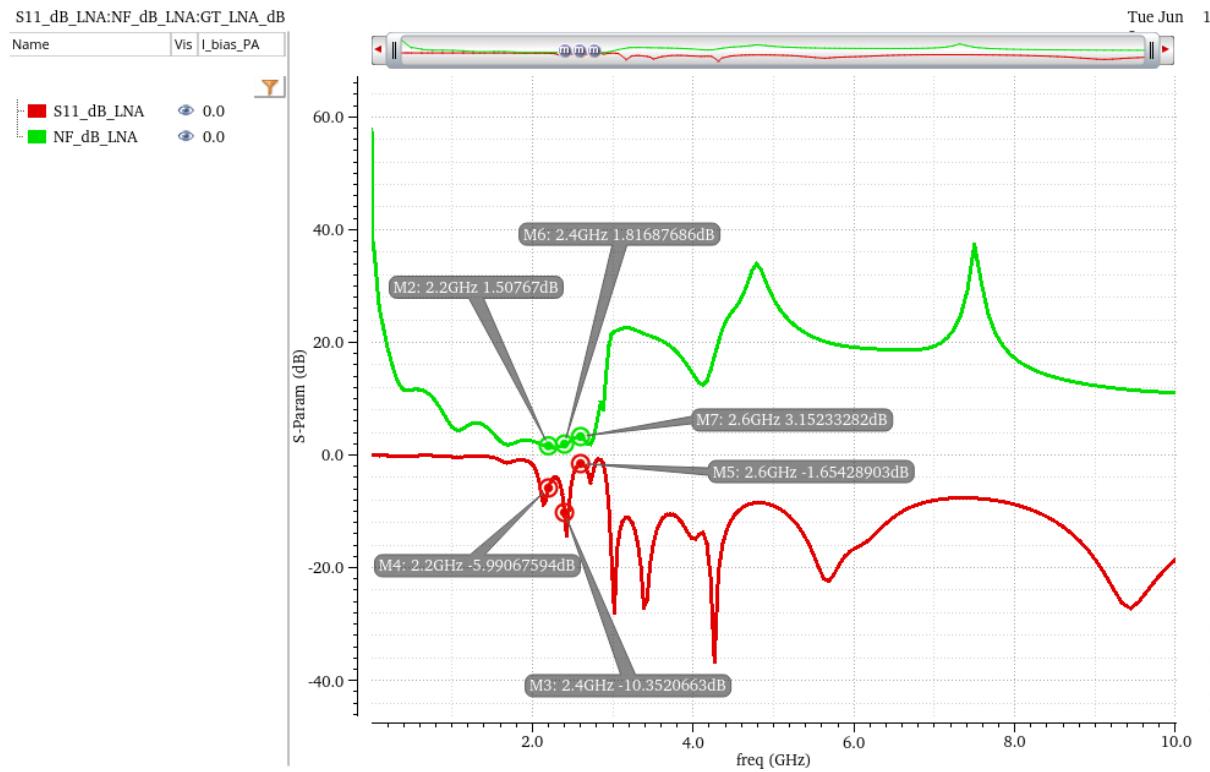


Figure 42: LNA S11 and NF simulations (TX Off).

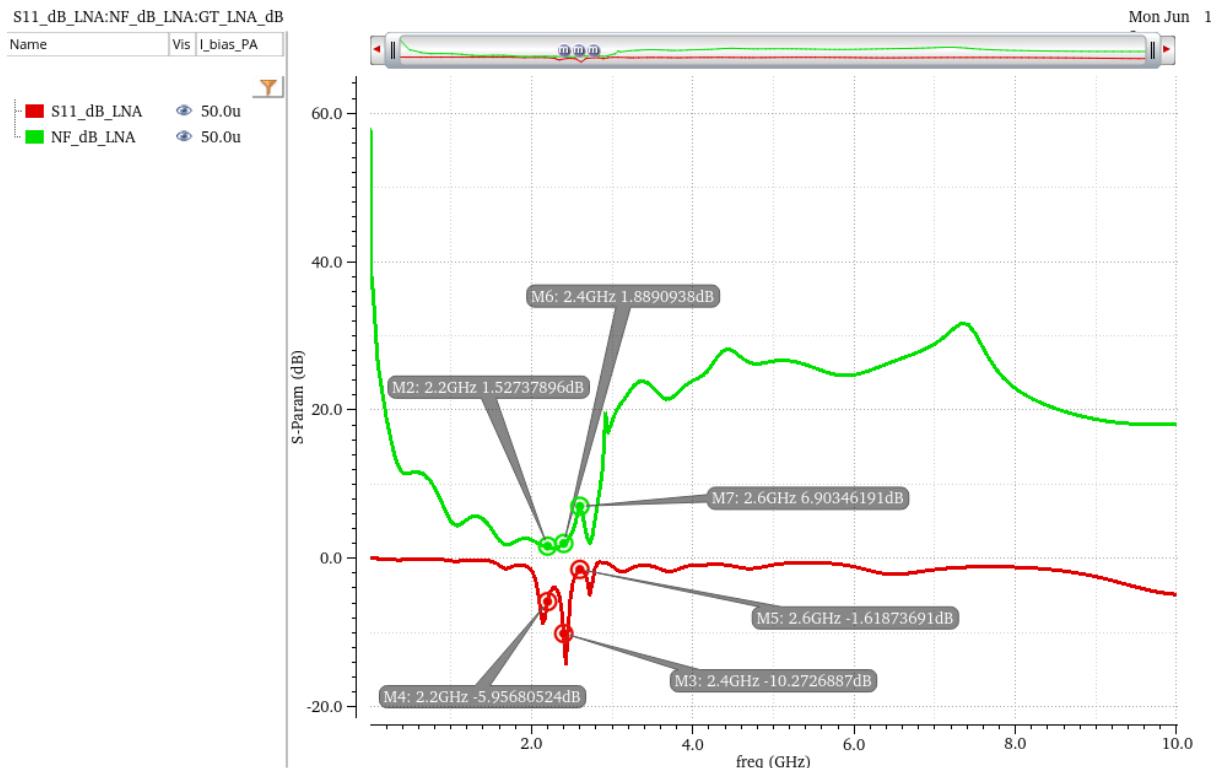


Figure 43: LNA S11 and NF simulations (TX On).

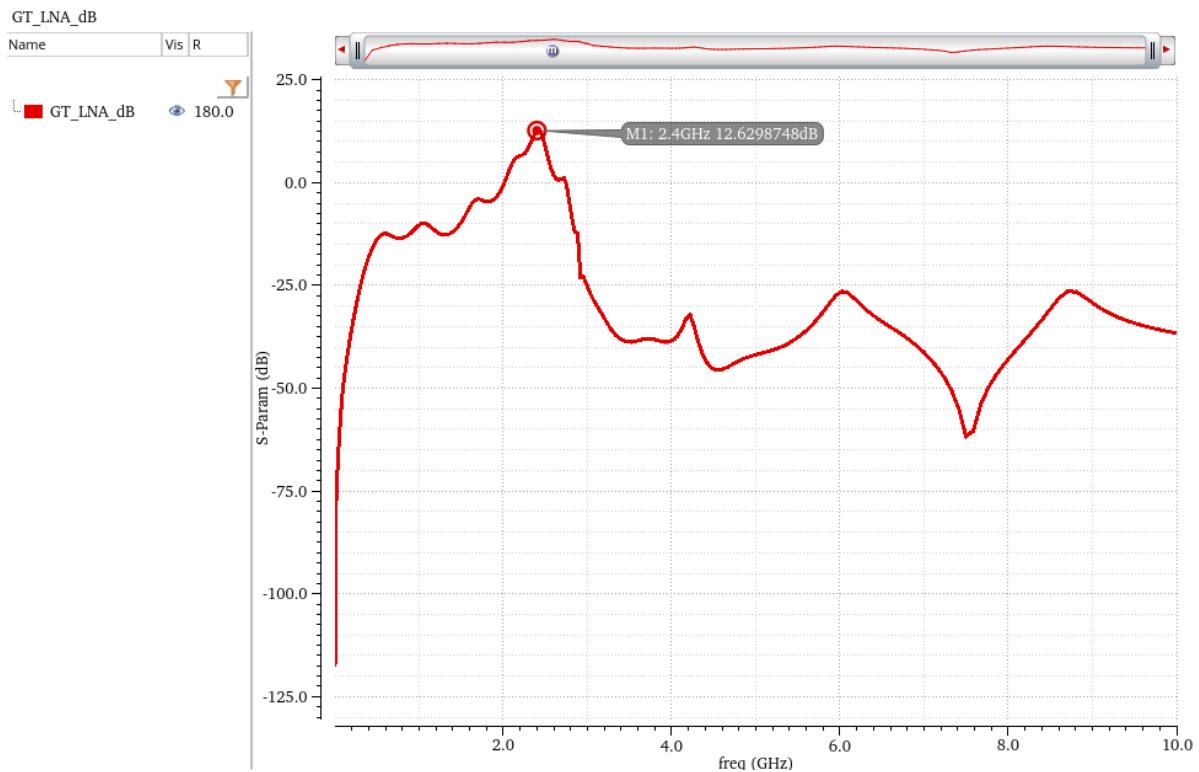


Figure 44: LNA G_T simulation.

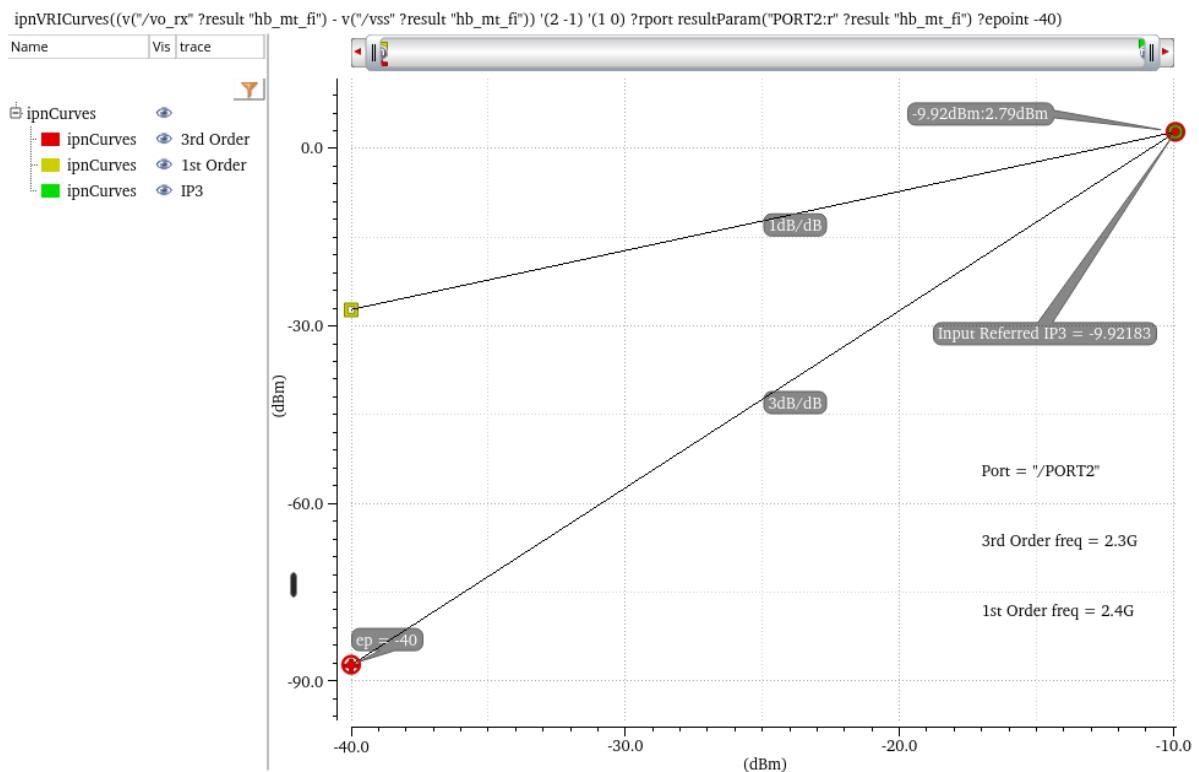


Figure 45: LNA IIP3 simulation.

The LNA's die area consumption is found in Tab 4, which only considers inductive and capacitive passives (resistors and active devices are not included).

Type	Label	Die Area	Percentage of Allowed Die Area
Inductor	L_G	$71,800 \mu m^2$	6.8%
	L_D	$45,400 \mu m^2$	4.3%
	L_{match}	$71,800 \mu m^2$	6.8%
	Total	$189,000 \mu m^2$	17.9%
Capacitor	C_{in}	$4,200 \mu m^2$	0.4%
	C_B	$20,000 \mu m^2$	2.0%
	$C_{GS1,add}$	$730 \mu m^2$	0.07%
	$C_{1,add}$	$2,000 \mu m^2$	0.2%
	C_{out}	$10,000 \mu m^2$	1.0%
	Total	$37,000 \mu m^2$	3.5%
Total Used	-	$226,000 \mu m^2$	22%

Table 4: LNA die area summary.

5.5 LNA Improvements: Low NF Design

Following a similar design approach as above, we designed an LNA with standalone NF less than 1 dB. This design also achieves the full L_G value with a single bondwire, saving die area at the cost of increased power and reduced FOM_{LNA} . As L_G decreases, C_{GS1} must increase to maintain resonance at f_0 . However, this worsens the input match, so g_{m1} must be made larger to compensate. Increasing the device width roughly scales C_{GS1} and g_{m1} at the same rate, preserving the input match at the cost of increased power consumption.

The low NF design is shown in Fig. 46. It employs the same L_D and L_{match} from the previous design. Tab. 5 compares the LNA specifications to results achieved from simulation (shown in Fig. 47 - 51). As was found for the other LNA design, the NF becomes problematic at 2.6 GHz for the same reasons discussed earlier. We look into this further and describe potential solutions in Section 6.

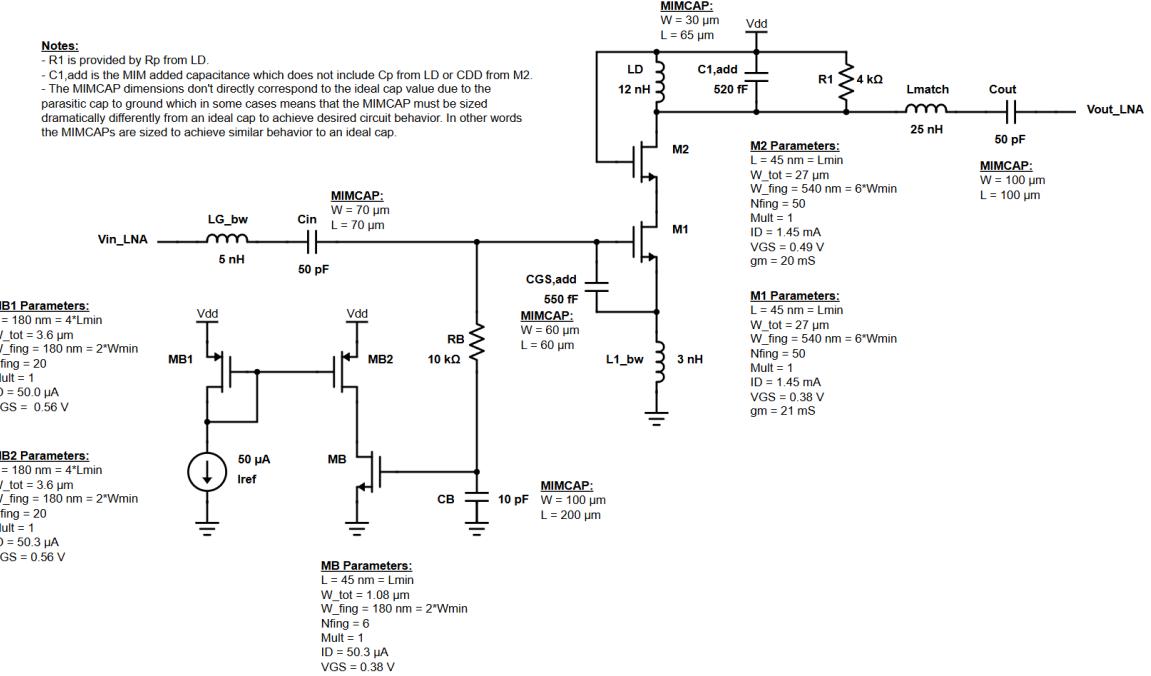


Figure 46: Low NF LNA circuit schematic.

Metric	Specification	Simulation Results	Notes
Input Match (S_{11})	-10 dB	-13.1 dB	At center frequency.
NF (Standalone LNA)	1 dB	0.93 dB	Max across frequency.
NF (TX Off)	3 dB	2.45 dB	Max across frequency.
NF (TX On)	4 dB	8.6 dB	Max across frequency.
IIP3	-23 dBm	-2.3 dBm	At center frequency.
G_T	-	12.2 dB	At center frequency.
P_{LNA}	-	1.56 mW	-
FOM_{LNA}	-	$6.81 \times 10^6 W^{-2}$	At center frequency.

Table 5: Low NF LNA achieved simulation results.

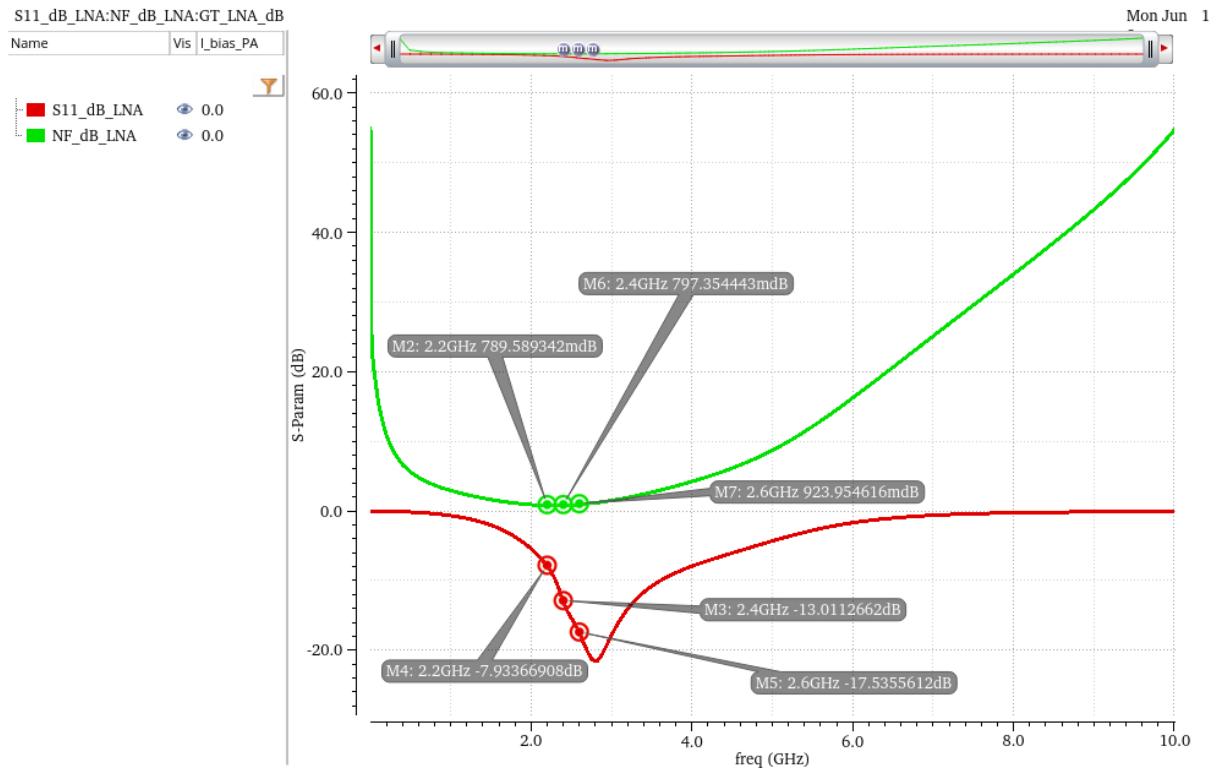


Figure 47: Low NF LNA S11 and NF simulations (standalone LNA).

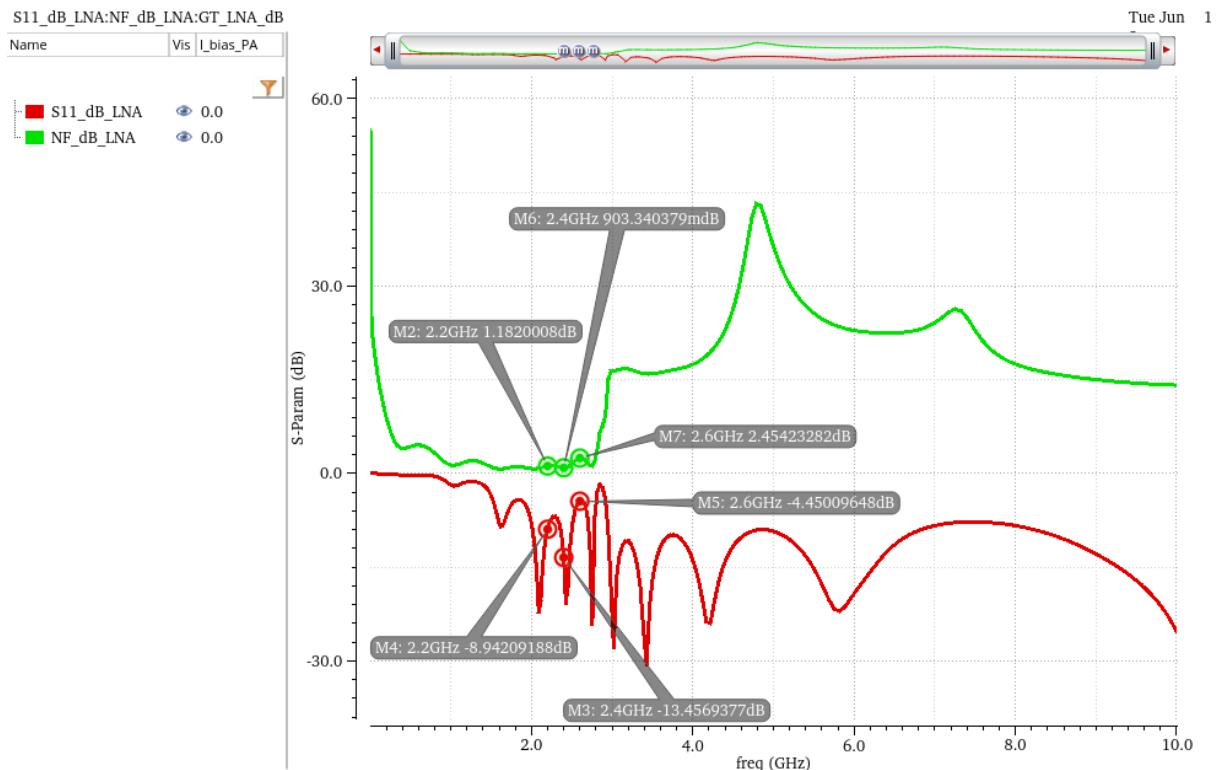


Figure 48: Low NF LNA S11 and NF simulations (TX Off).

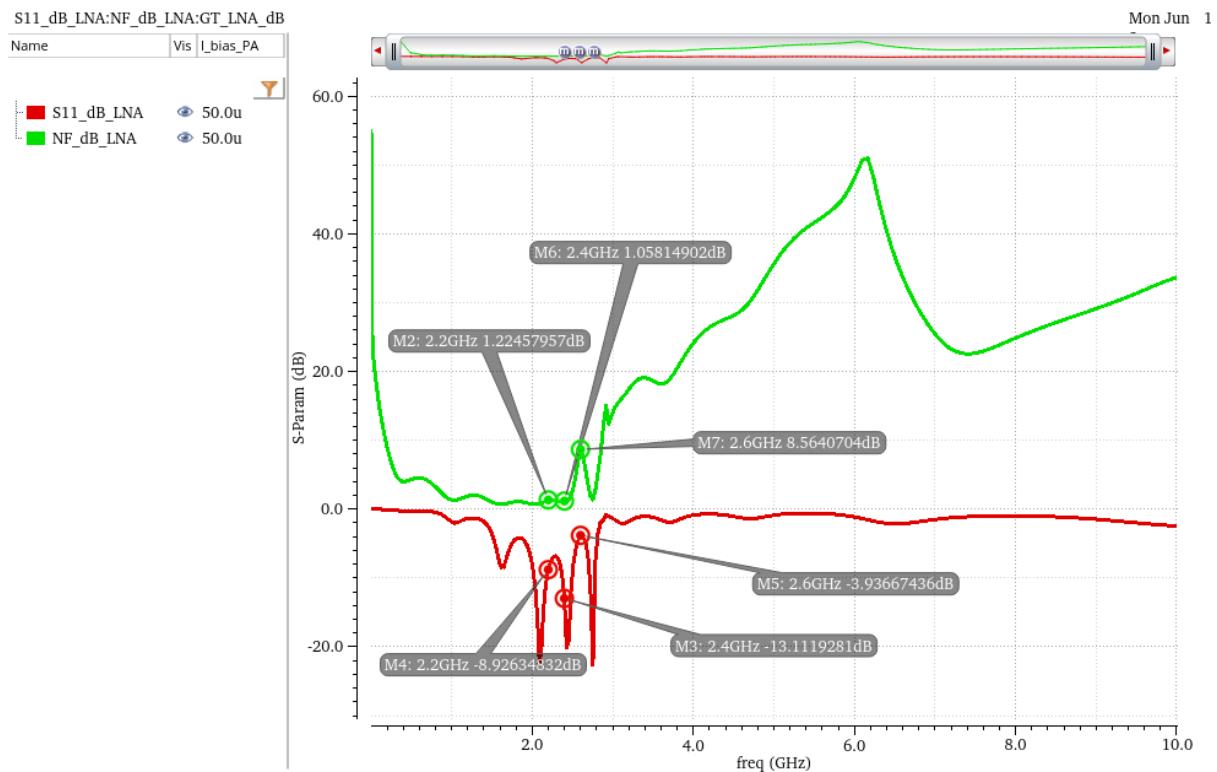


Figure 49: Low NF LNA S11 and NF simulations (TX On).

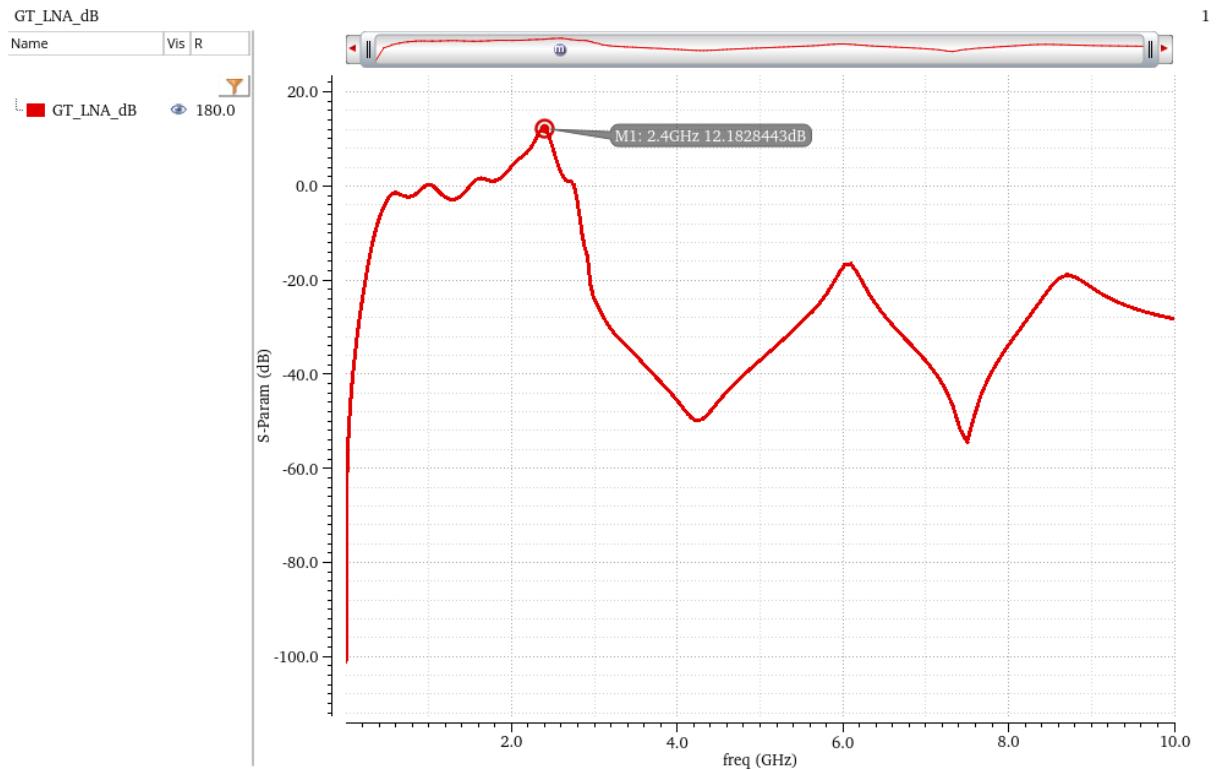


Figure 50: Low NF LNA G_T simulation.

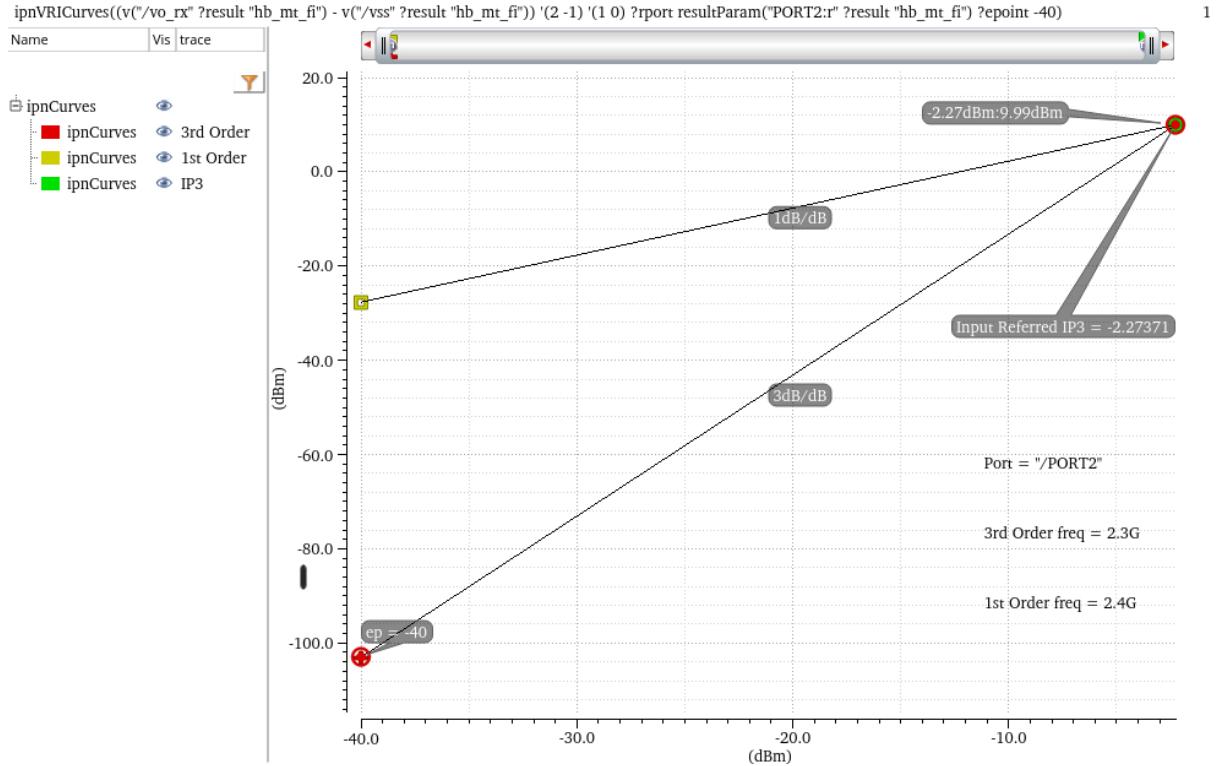


Figure 51: Low NF LNA IIP3 simulation.

The LNA's die area consumption is found in Tab 4, which only considers inductive and capacitive passives (resistors and active devices are not included).

Type	Label	Die Area	Percentage of Allowed Die Area
Inductor	L_D	$45,400 \mu m^2$	4.3%
	L_{match}	$71,800 \mu m^2$	6.8%
	Total	$117,000 \mu m^2$	11.1%
Capacitor	C_{in}	$4,900 \mu m^2$	0.5%
	C_B	$20,000 \mu m^2$	1.9%
	$C_{GS1,add}$	$3,600 \mu m^2$	0.3%
	$C_{1,add}$	$1,900 \mu m^2$	0.2%
	C_{out}	$10,000 \mu m^2$	1.0%
	Total	$41,000 \mu m^2$	3.9%
Total Used	-	$158,000 \mu m^2$	15%

Table 6: Low NF LNA die area summary.

5.6 Design Comparison

Tab. 7 compares the various LNA designs completed as a part of this project.

Metric	M2 Design	FOM Design	Low NF Design	Notes
S_{11}	-20.8 dB	-10.2 dB	-13.1 dB	At center frequency.
NF (alone)	2.6 dB	2.1 dB	0.93 dB	Max across frequency.
IIP3	-25 dBm	-9.9 dBm	-2.3 dBm	At center frequency.
G_T	22.4 dB	12.6 dB	12.2 dB	At center frequency.
P_{LNA}	2.1 mW	0.351 mW	1.56 mW	-
FOM_{LNA}	$38.4 \times 10^6 W^{-2}$	$149 \times 10^6 W^{-2}$	$6.81 \times 10^6 W^{-2}$	At center frequency.
Die Area	$628,000 \mu m^2$	$226,000 \mu m^2$	$158,000 \mu m^2$	-

Table 7: LNA design comparison.

From Tab. 7 it is seen that the FOM design, unsurprisingly, has a better FOM than the M2 and low NF designs, by a factor of 3.8 and 21.9 respectively. The FOM design is low power and moderate area, compared to the low NF design which is higher power and lower area. Notably the low NF design is high power due to the goal of implementing L_G solely with a bondwire. In other words, a simultaneously low power and low noise LNA is possible (which would boost the FOM dramatically), however in this particular design we also imposed the L_G constraint. Both Milestone 3 designs offer significant die area reduction compared to the Milestone 2 design because the inductors were laid out more efficiently.

6 TX & RX Coexistence

As discussed earlier, the LNA NF is not meeting specification when the PA is powered on, specifically in the high-frequency portion of the band (2.6 GHz). This is the coexistence problem, illustrated by Fig. 52, which must be addressed in frequency division duplexing (FDD) systems such as ours.

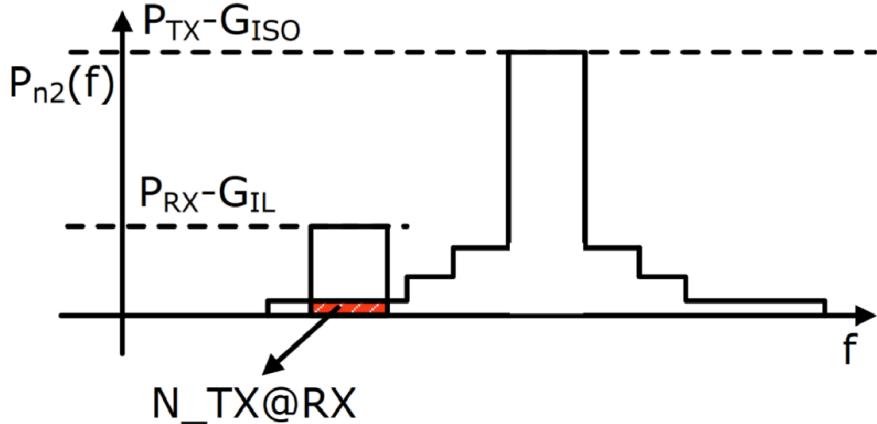


Figure 52: TX/RX coexistence problem: wideband noise from the PA output can directly couple to the LNA input through the TRX diplexer, leading to RX de-sensitivity via degraded LNA noise figure.

The diplexer's characteristics must be examined in order to see how much rejection the filter provides against the PA's broadband output noise. Fig. 53 shows the S-parameter response from the antenna port to the RX port and Fig. 54 shows the response from the RX port to the TX port.

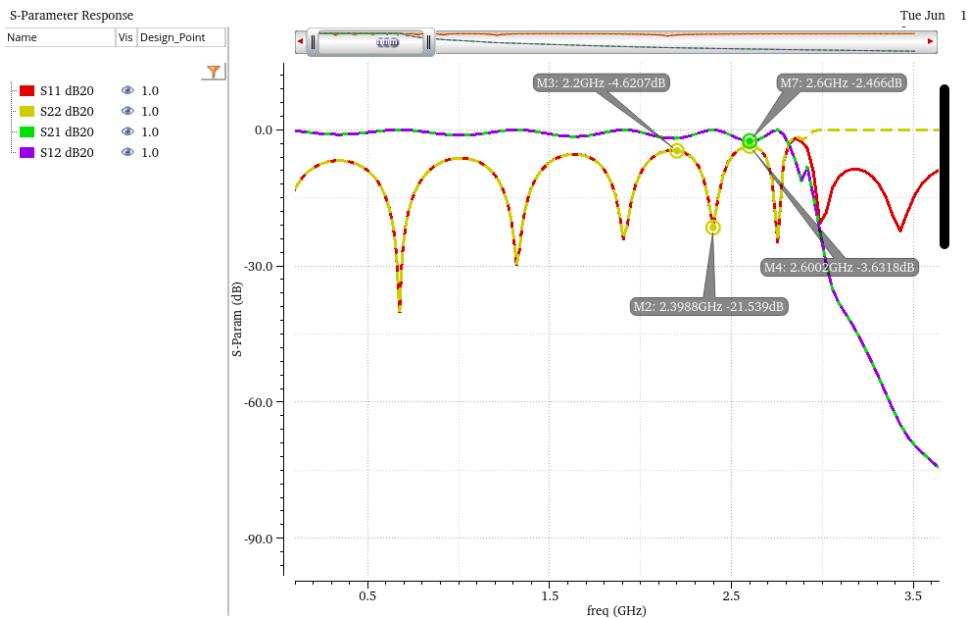


Figure 53: Diplexer S-parameter response from antenna (1) to RX (2).

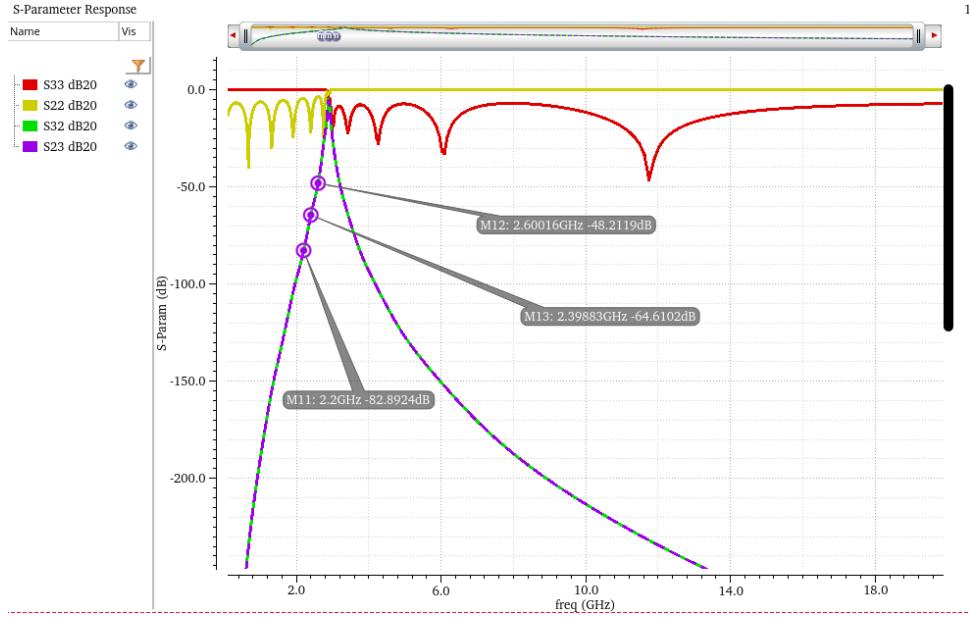


Figure 54: Diplexer S-parameter response from RX (2) to TX (3).

From Fig. 55, the baseline noise figure across the entire LNA operating band is within spec for 2.2 GHz and 2.4 GHz, but marginally exceeds the 3 dB requirement at 2.6 GHz. This can be attributed to the poor insertion loss of the diplexer at 2.6 GHz as it is close to the roll-off point of the circuit, as observed by the frequency response in Fig. 53. The insertion loss could be remedied by increasing the diplexer filter order, but this has other implications in terms of pre-LNA insertion loss, cost, and area footprint.

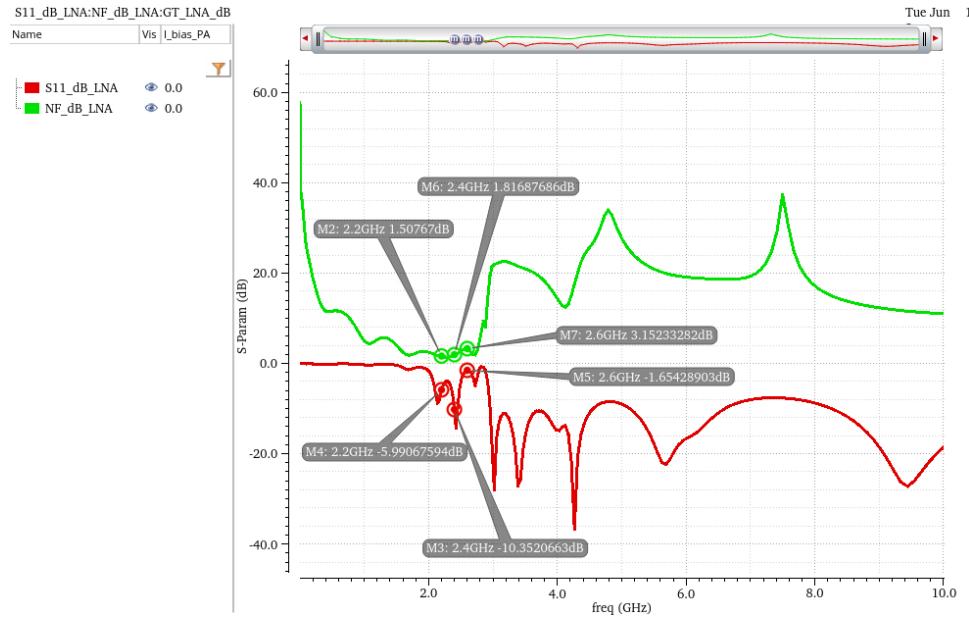


Figure 55: LNA S11 and NF (TX Off, no PA output filter).

With the PA on, the noise figure at 2.6 GHz degrades by 3.75 dB (as illustrated by Fig. 56), which is non-trivially out of spec. The degradation can be traced to the thermal noise arising from resistors contained at the input of the PA which is being amplified and directly appearing at the PA output across

a broad bandwidth. The PA circuit in this design still has a multi-GHz instantaneous bandwidth with high gain away from the nominal center frequency of 5.9 GHz. As such, the output PSD is broadband, and more rejection is needed to bring the 2.6 GHz NF level back into specification. We see in Fig. 54 that the diplexer provides 48.2 dB of isolation between the TX/RX paths at 2.6 GHz, while the isolation is significantly higher at 2.2 GHz and 2.4 GHz. Note that this noise is quiescent, and appears as soon as the PA is biased on. The degradation remains very similar in the cases where the PA is on but not driving any signal, and when the PA is driving the maximum possible input of 4 dBm.

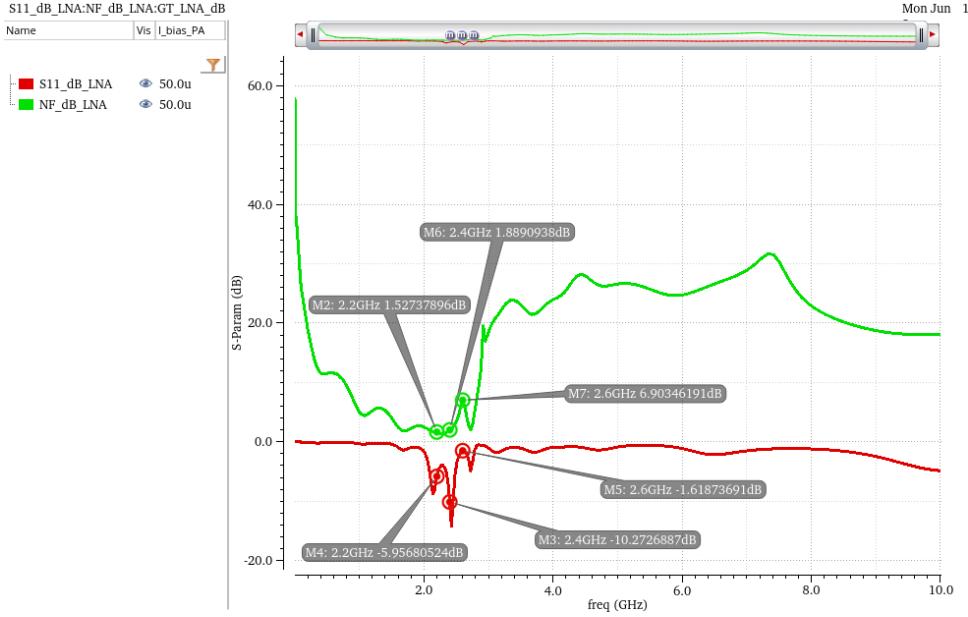


Figure 56: LNA S11 and NF (TX On, no PA output filter).

To model the required rejection needed to achieve TX/RX coexistence, we add a simple second-order high pass network to the PA output (input and output impedance of 50Ω) with a corner frequency of 4.0 GHz as shown in Fig. 57. This is a reasonable thing to model, since any dynamic channel-select matching network at the PA output (which is not included in the testbench) would naturally have a bandpass characteristic with a moderate amount of attenuation away from the center frequency of $f_0 = 5.9$ GHz. The extra attenuation could be realized with a dedicated filter path off-chip before the diplexer, or can leverage the attenuation provided by the dynamic channel select matching circuit.

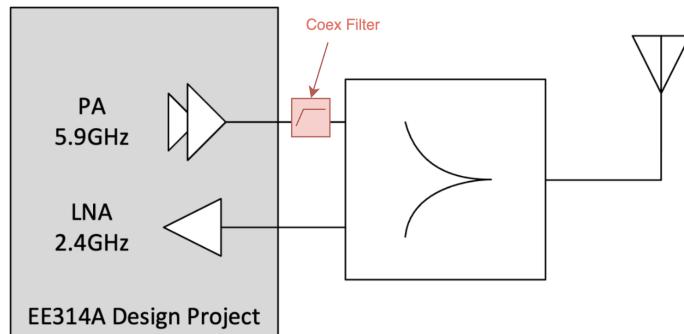


Figure 57: PA output with a simple HPF or BPF response provides modest rejection at 2.6 GHz from broadband output noise.

From Fig. 58, we see that adding the second-order high-pass filter to the output of the PA drastically improves the NF of the LNA in the high-frequency portion of the band (compared to the case without a filter, shown in Fig. 56), bringing it within the 4 dB specification and roughly in line with the TX Off results shown in Fig. 55. The added filter's frequency response is shown in Fig. 59.

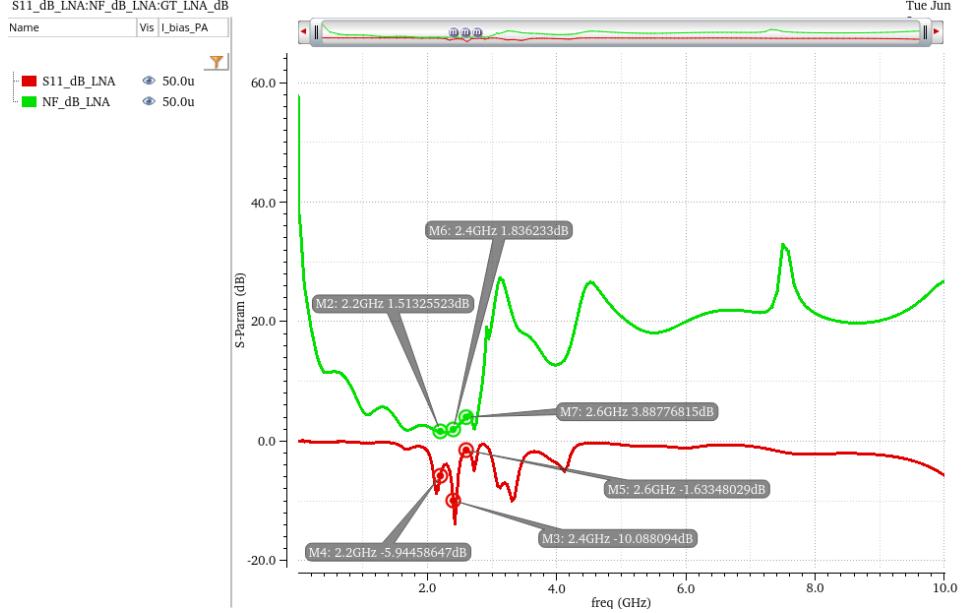


Figure 58: LNA S11 and NF (TX On, PA output filter).

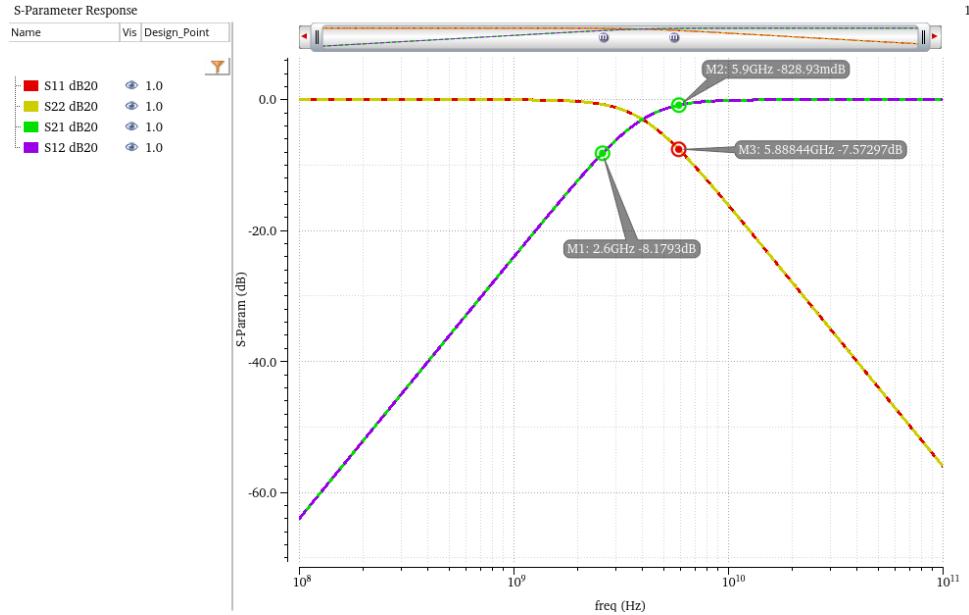


Figure 59: High-pass filter frequency response.

We see that to achieve the required NF performance, the PA output filter would need to provide roughly 8 dB of attenuation to meet the coexistence requirements. A simple adjustment of the PA output match can easily provide this rejection. For this configuration we see that S_{11} is at best -7.6 dB and S_{21} is at best -0.8 dB at the 5.9 GHz center frequency of the PA. If these values are desired to be improved, a higher order filter can be opted for at the cost of additional implementation complexity.

7 Chip Diagram and Configuration

Fig. 60 depicts a model of the QFN packaged chip pinout with the number of package pins and bondwires used in the testbench specified. The bondwire configuration is found in Tab. 8, the I/O resource summary in Tab. 9, and the die area decomposition in Tab. 10.

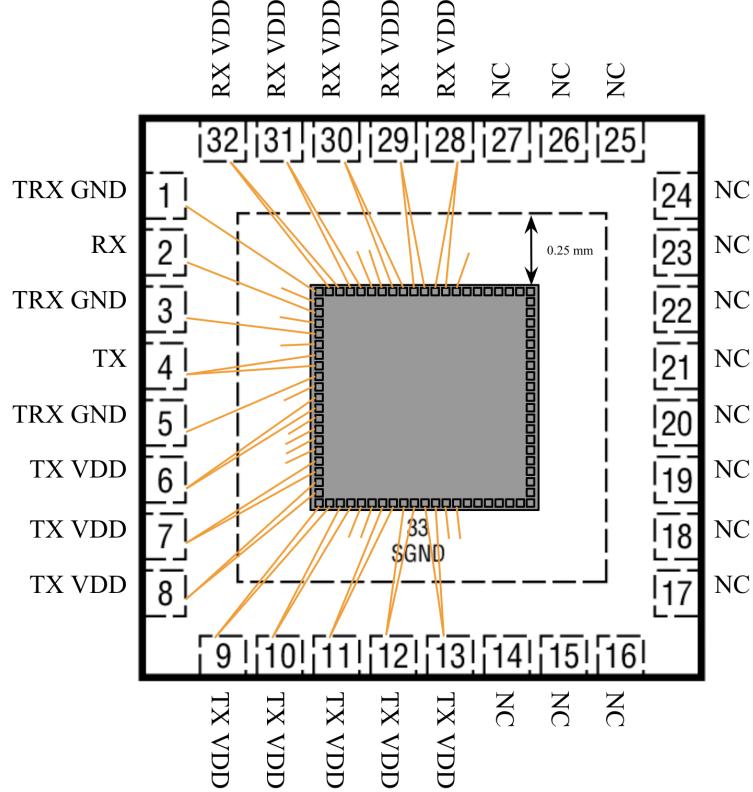


Figure 60: Chip diagram.

Note that the bondwire count for the PA VDD and GND are high and kept to minimum length in order to minimize the associated parasitic inductance on these nodes, which is crucial for PA stability and linearity.

Package Pin	Die Pad	Bondwire Length	n	Notes
RX	LNA_rx	3.5 mm	1	LNA input match.
TX	PA_tx	0.3 mm	2	-
TX VDD	PA_vdd	0.3 mm	16	-
RX VDD	LNA_vdd	0.3 mm	10	-
TRX GND	trx_gnd	0.3 mm	2	-
SGND (die paddle)	Vss	0.25 mm	15	-
TRX GND	LNA_ind_degen	1 mm	1	LNA degeneration inductor.

Table 8: Chip bondwire configuration.

Resource	Allowed	Used
Package Pins	31	19
Die Pads	80	47
Bondwires	80	47

Table 9: Chip I/O summary.

Category	Die Area	Percentage of Allowed Die Area	Percentage of Used Die Area
LNA Passives	226,000 μm^2	22%	36%
PA Passives	377,000 μm^2	36%	61%
Other Passives	20,000 μm^2	1%	3%
Total Passives	623,000 μm^2	59%	100%

Table 10: Die area summary; transformer & transistor area omitted.

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