A 10-Bit, 140 MS/s, 0.88 mW Fully-Differential Asynchronous SAR ADC in 90 nm CMOS

Nihar Ahire, *Student Member, IEEE*, Aiden Duncanson, *Student Member, IEEE*, and Austin Rothschild, *Student Member, IEEE*

***Abstract*—A 10-bit, 140 MS/s, fully-differential, asynchronous successive approximation register (SAR) analog-to-digital converter (ADC) in 90 nm CMOS is presented. The design utilizes top-plate sampling, a monotonic, split capacitor digital-to-analog (DAC) switching scheme, a small unit capacitance (2.5 fF), and a high-speed, multi-stage comparator to achieve a SNDR of 56.2 dB at Nyquist, consuming 0.88 mW of power and resulting in a figure of merit (FOM) of 4.49x10^{-20} W/Hz^2.**

***Index Terms*—Analog-to-digital converter, successive approximation register, low power, asynchronous.**

I. Introduction

THE successive approximation register (SAR) analog-to-digital converter (ADC) offers excellent power efficiency and minimal area overhead for applications requiring medium resolution (8 to 10 bits) and moderate operating speed [1]. The application considered in this work calls for an SNDR exceeding 55 dB at Nyquist rate inputs and a moderate sampling frequency, f_s, and thus is well suited to the SAR architecture.

The objective of this design is to achieve a high f_s, at a low average power consumption, P, accomplished by minimizing the FOM given by Eq. 1, while still meeting the SNDR requirement.

$$FOM = \frac{P}{f_s^2} \tag{1}$$

To reduce power consumption, top-plate sampling is used, thereby removing the need for the MSB capacitor and lowering the sampling capacitance by a factor of two. A monotonic, split capacitor switching scheme is employed to achieve symmetric switching and maintain a fairly constant common-mode voltage at the input of the comparator, while reducing switching power, inspired by [2] and [3]. The input sampling switch is bootstrapped in order to achieve high linearity and bandwidth. A high-speed triple-stage dynamic comparator is paired with asynchronous SAR logic to operate the ADC at a higher f_s than would otherwise be achievable with synchronous timing for a fixed metastability rate. Finally, a fully differential implementation is chosen for its strong common-mode noise rejection, reduced even order nonlinearity, and improved SNR to help meet the SNDR specification.

This paper is organized as follows. Section II describes the ADC sub-block design considerations, circuit realizations, and system level implications. Section III presents simulation results and achieved performance. Conclusions are given in Section IV.

The authors are with the Department of Electrical Engineering, Stanford University, Stanford, USA (e-mail: nihar30@stanford.edu; afduncan@stanford.edu; austinxr@stanford.edu).

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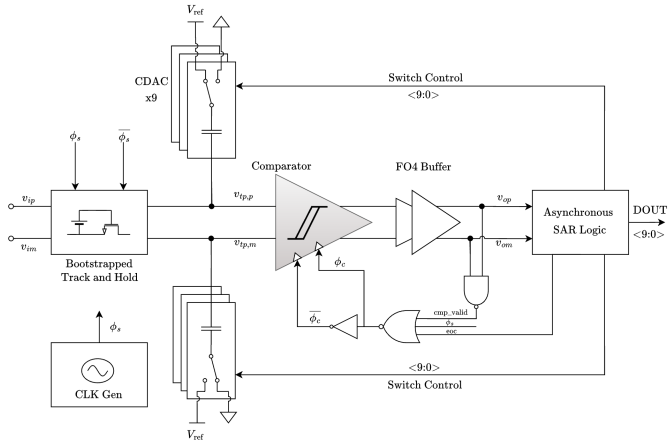


Fig. 1. Proposed asynchronous SAR ADC block diagram.

II. ADC Sub-Blocks

The fundamental functional blocks of this SAR ADC are the track and hold (T/H) circuit, the comparator, the capacitive DAC (CDAC), and the asynchronous SAR logic, as seen in Fig. 1. Each block's design considerations and tradeoffs are described in the following subsections.

A. Bootstrapped Track and Hold

The performance of a high-speed ADC is closely tied to the accuracy with which it can capture the input signal during sampling. To achieve this, ADCs rely heavily on the bootstrapped switch, which plays an important role in preserving signal fidelity, directly impacting both the maximum achievable sampling rate and resolution. The on-resistance of a transistor is dependent on its gate-to-source voltage, resulting in distortion of the input signal during sampling. If an NMOS is used as the sampling switch with the input signal driving the source and the gate connected to a clock signal, the on-resistance (R_{on}) is given by Eq. 2.

$$R_{\text{on}} = \frac{1}{\mu_n C_{\text{ox}} \dfrac{W_n}{L_n} \left(V_{Clk} - V_{in} - V_{tn}\right)} \tag{2}$$

Thus, R_{on} exhibits signal-dependent dynamics, increasing with larger V_{in}, resulting in distortion of the sampled signal. Using a transmission gate to remedy the situation is not

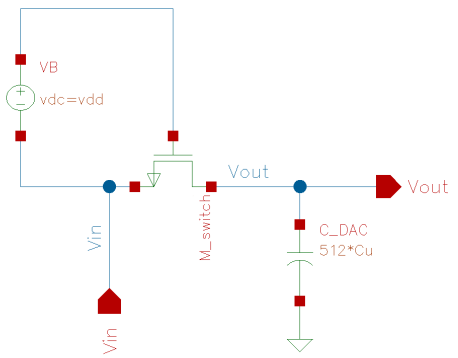


Fig. 2. Simple bootstrapped switch with a battery.

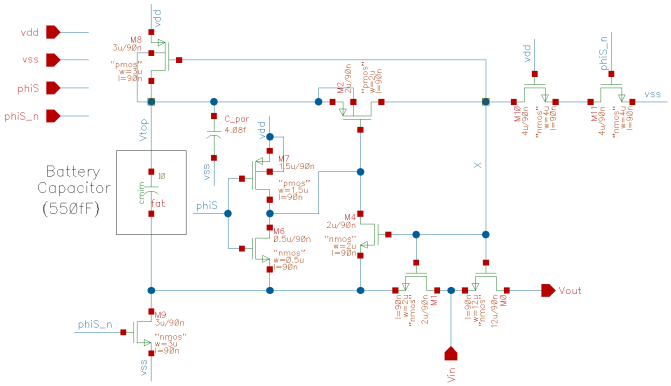


Fig. 3. Final bootstrapped switch schematic.

enough. Although the combined on-resistance, $R_{\text{on,total}}$, given by Eq. 3, appears to be independent of V_{in}, several non-ideal effects cause it to vary. These include mobility degradation due to the increasing vertical fields in the channel as V_{in} increases [4], short-channel effects, and the body effect.

$$R_{\text{on,total}} = \frac{1}{\mu_n C_{\text{ox}} \frac{W_n}{L_n} (V_{DD} - V_{tn} - |V_{tp}|)} \tag{3}$$

The simplest representation of a bootstrapped switch is shown in Fig. 2, where a battery is connected between the gate and source terminals of the NMOS, and the load capacitor represents the CDAC ($C_u = 2.5$ fF) that the switch must drive. This configuration helps maintain a constant V_{GS}, resulting in an on-resistance that remains nearly constant as V_{in} increases. However, in a practical track-and-hold circuit, the switch must be clocked such that it tracks V_{in} during the "track phase" ($\phi_S = 1$), and preserves the sampled voltage on the CDAC at the transition during the "hold phase" ($\phi_S = 0$). Additionally, the DC battery needs to be replaced by a capacitor in the non-ideal implementation.

1) Design Methodology: It can be seen from Fig. 2 that the NMOS's R_{on} and the CDAC form a low-pass filter. As a design target, a maximum input attenuation of 0.2 dB during sampling was targeted. To meet this requirement, R_{on} was calculated to be approximately 270 Ω, which corresponds to an NMOS width of 2 μm. This value was chosen as a starting point and the FFT was computed. It is important to monitor the odd harmonics in the FFT (the even harmonics are cancelled by the differential ADC architecture), since strong harmonics indicate distortion introduced during sampling. For an ideal 10-bit ADC, the theoretical maximum achievable SNR is approximately 62 dB. Therefore, the harmonic components must be significantly lower than -62 dB (at least 10 dB below this level), as this represents the theoretical quantization noise floor [5]. The final schematic with transistor and battery capacitor sizing is shown in Fig. 3.

Transistors M2 and M11 were added first, where M2 connects the positive terminal of the battery capacitor to the gate of M0 during the tracking phase, and M11 connects the gate of M0 to ground during the hold phase, turning it off. The parasitic capacitance at node X and $R_{\text{on},M2}$ form a low-pass filter; therefore, $R_{\text{on},M2}$ must be small enough to provide a sufficiently large bandwidth compared to the input signal frequency (small time constant). Hence, the width of M2 was chosen to be 2 μm. M11 must also be wide enough to pull node X to ground quickly; otherwise, the on-resistance of M0 increases slowly at the end of tracking, causing sampling distortion. However, M11 cannot be made excessively wide, as this would increase the parasitic capacitance at node X. So, the width of M11 was initially selected to be 2 μm. Later, M1 and M9 were added. M1 connects the negative battery terminal to the source of M0 during the tracking phase so that the bootstrapping action can occur, and M9 connects the negative battery terminal to ground during the hold phase. The gate of M1 needs to be bootstrapped because its on-resistance would otherwise vary significantly during sampling. M1 was sized to a width of 2 μm so that it does not load node X with excessive parasitic capacitance. M9 was sized to be 3 μm since it needs to be wide enough to pull the negative battery terminal to ground quickly.

Eventually, the battery was replaced with a capacitor, and M8 was added so that the top plate of the capacitor can be charged back up to V_{DD} during the hold phase. There are two important design considerations when sizing the battery capacitor (C_B). The first is that charge-sharing with the parasitic capacitance at node X can reduce the actual voltage at the gate of M0 to be lesser than V_{DD} [5]. Therefore, C_B must be large enough so that this voltage attenuation is not significant. The second consideration is that C_B must be charged back up to V_{DD} during the hold phase, so it cannot be too large [5]. After careful consideration C_B was sized at 550 fF (which is also feasible from a layout perspective), and the width of M8 was made 3 μm. It is important to note that the bulk of M8 is tied to its drain instead of V_{DD}, and similarly the bulk of M2 is tied to its source. If the bulks of these PMOS transistors were tied to V_{DD} instead, the parasitic pn-junctions in those devices could turn on since the top plate of the battery capacitor can rise above V_{DD}. C_{par} in Fig. 3 was added to model the well-to-substrate parasitic capacitance of M2 and M8.

It is important to reduce the device stress on some critical

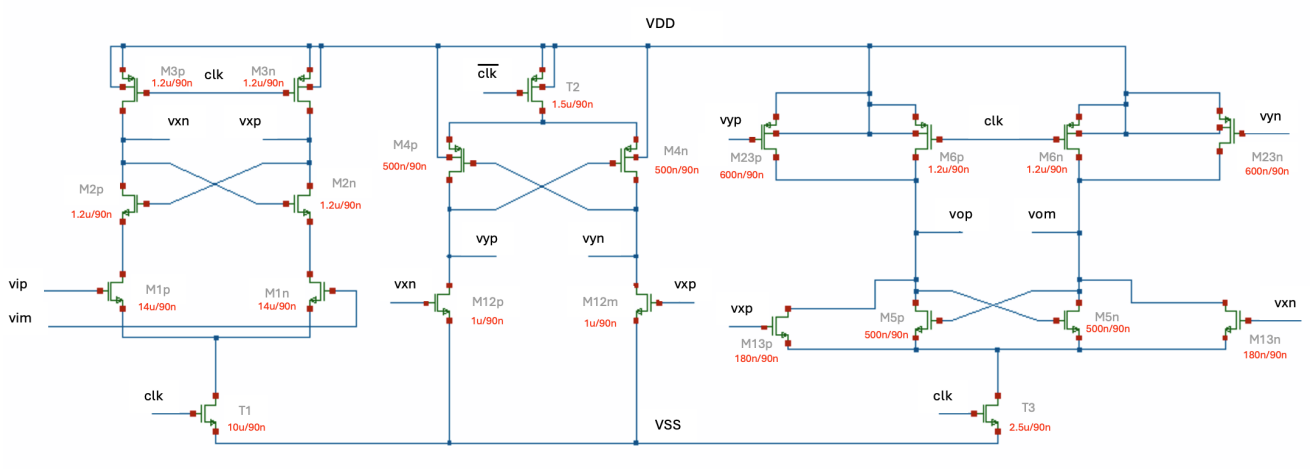


Fig. 4. Proposed triple-latch feedforward (TLFF) dynamic comparator implemented in this work. Stage 1 is optimized for high gain and low noise. Stage 2 is optimized for modest gain with minimal loading. Stage 3 is optimized for modest gain with fast regeneration.

transistors like M11 and M2 [5]. M10 was added as a cascode transistor as the V_{DS} of M11 by itself could cross V_{DD} during the track phase. M4, M6, and M7 were added to reduce the stress on M2 by ensuring that its gate voltage changes in accordance with V_{in}. At this point, FFT simulations showed that M0 needed to be wider because the body effect was causing its on-resistance to vary significantly across the tracking phase. Increasing the width of M0 to 12 μm from its initial value of 2 μm helped suppress this variation. Testing the bootstrapped switch at this point with a nyquist frequency input at the target sampling frequency of 140 MHz revealed an HD3 and HD5 of -99.9 dB and -112.8 dB respectively, indicating low sampling distortion.

B. Comparator

The proposed comparator implemented in this work is shown in Fig. 4 and uses the triple-latch feedforward (TLFF) dynamic topology inspired by [6], [7]. Its fully dynamic operation eliminates static current paths, resulting in high power efficiency. This architecture provides high gain by means of horizontal cascading as opposed to vertical cascading typical in multi-stage designs, removing headroom concerns imposed by vertical stacking and allowing for decoupled optimization of each stage's sizing. In high speed SAR ADCs, comparators with high gain are required in order to regenerate the hard-decision made during each new input sample.

Many dynamic designs make use of double-tail dynamic architectures, such as those in [8], [9]. However, these designs suffer from the resolution time of the comparator being a strong function of the input signal level. Additionally, they do not provide enough gain for a fixed power target in order to push to high enough sampling speeds that satisfy metastability requirements. The TLFF architecture provides a high gain sufficient for the hard decision at high speeds, along with a feedforward path that bypasses the need for easy decisions to traverse through the second stage, as this incurs unnecessary signal delay. This leads to a relatively constant delay as a function of the input v_{id}. Additionally, the TLFF minimizes the use of reset devices as is typical in dynamic comparators, instead re-purposing the amplifying transistors M12p/M12n as pull-down devices and M23p/M23n as pull-up devices when the comparator clock goes low, therefore minimizing capacitance on the signal path.

1) Design Methodology: The multi-stage nature of the TLFF allows for decoupled optimization of each stage in order to balance the performance across varying input levels while producing minimal input referred noise and having little power overhead. Here we describe how the regeneration time (delay), gain, and input referred noise are considered and subsequently computed.

The regeneration time of the TLFF is given as

$$\tau_{comp} = \tau_1 + \tau_{FF} \tag{4}$$

where $\tau_1 \approx C_X/g_{m2}$ is the time-constant of the first stage, and τ_{FF} is the signal-dependent feedforward path delay given as:

$$\tau_{FF} \approx \begin{cases} \tau_2\left(1+\frac{g_{m12}}{g_{m4}}\right)+\tau_3\left(1+\frac{g_{m23}}{g_{m5}}\right) & \text{Small } v_{in} \\ \tau_3\left(1+\frac{g_{m23}}{g_{m5}}\right) & \text{Large } v_{in} \end{cases} \tag{5}$$

where $\tau_2 \approx C_Y/g_{m4}$ and $\tau_3 \approx C_{\text{out}}/g_{m5}$. The delay of the second-stage is bypassed for large input signals (easy decisions) by the minimum sized feedforward devices M13p and M13n. The worst-case comparator delay occurs for small inputs (hard decisions) and sets the upper bound on the comparator frequency. The worst case comparator regeneration time is extracted using Fig. 5 as $\tau_{comp} \approx 10.04$ ps, with the original design target being less than 12 ps to allow for 200 MS/s synchronous operation, which would enable even higher asynchronous capability.

The cascaded gain of the TLFF is approximately the product of each stage's individual gain during their appropriate amplification times [10]:

$$A_v \approx \frac{g_{m1}V_{th1}}{I_{CM1}} \cdot \frac{g_{m12}V_{th12}}{I_{CM12}} \cdot \frac{g_{m23}V_{th23}}{I_{CM23}} \approx 27.75 \tag{6}$$

where g_m is the transconductance, V_{th} is the threshold voltage, and I_{CM} is the common-mode bias current during each of the respective gain stage's amplification windows. Since the amplifier is dynamic, these operating points are time-varying and must be extracted via transient analysis. This is done for the case of a small input signal after the comparator has been reset, with the transient waveforms in Fig. 6 used for operating point extraction. The cascaded gain of $A_v = 27.75$ is sufficiently high to regenerate signals close to the LSB when clocking the comparator between $1-2$ GHz. More gain is allocated to the first stage in order to achieve low input referred noise, at the expense of higher first-stage power.

An explicit expression for the total input-noise from the comparator is not readily available for this topology. Noting the analysis in [11], we attribute most of the input referred noise due to the first-stage, since the later stages noise contributions are attenuated by A_{v1}. Thus, we approximate the input referred noise following the approach used in the analysis of the StrongARM latch:

$$\sigma_n^2 = \frac{8kT\gamma}{C_{P,Q}} \cdot \frac{g_{m1}V_{\mathrm{TH1}}}{I_{\mathrm{CM1}}} \cdot \frac{1}{A_{v1}^2} \tag{7}$$

where $C_{P,Q}$ are the capacitance's at the drains of M1p and M1n. An initial sizing is chosen to achieve $\sigma_n \approx 0.6\ \mathrm{mV_{rms}}$, which would yield an SNR of 58.4 dB considering only comparator noise, quantization noise, and kT/C noise arising from the CDAC. This target provides sufficient margin for thermal noise introduced by other components, distortion tones, and increased noise folding at higher f_s. The true comparator input referred noise is extracted via a transient noise simulation with $FMAX = \frac{10}{2\pi\tau_{comp}} \approx 159$ GHz. The procedure outlined in [10] is used, whereby the comparator decisions in the presence of noise are recorded over 1000 independent simulation trials for four different differential input values of -1 mV, -200 μV, 200 μV, and 1 mV. The comparator output high probabilities on each input are then used to fit an error-function (ERF) response curve given by Eq. 8 below:

$$\begin{aligned} p(v_{din}) = \mathbb{E}[v_o] &= \frac{1}{\sqrt{2\pi}\sigma_n}\int_{-\infty}^{+\infty} v_o e^{-v_n^2/(2\sigma_n^2)}\, dv_n \\ &= \frac{1+\mathrm{erf}\left(\frac{v_{din}}{\sqrt{2}\sigma_n}\right)}{2} \end{aligned} \tag{8}$$

The ERF curve for the proposed design is shown in Fig. 7, with the extracted input referred noise voltage $\sigma_n \approx 0.57\ \mathrm{mV_{rms}}$.

2) Comparator Metastability: As noted in [12], the probability of a metastable comparator event scales as $P_{meta} \propto e^{-BN}$ for asynchronous SAR ADCs, as opposed to just e^{-N} which is the case for synchronous designs. With the comparator regeneration time for the hard decision and cascaded amplification gain known, the metastability rate of the asynchronous SAR ADC can be analytically verified:

$$P_{meta} = \frac{v_{id,min}}{\frac{1}{2}\cdot\frac{V_{FS}}{2^B}} = \frac{V_{DD}}{A_v}\cdot e^{-(B/(2f_c\tau))}\cdot\frac{2^{B+1}}{V_{FS}} \tag{9}$$

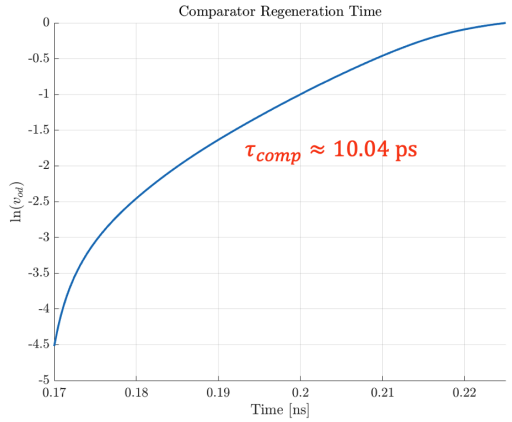


Fig. 5. Extracted worst-case comparator regeneration time for a differential input signal of $v_{id} = 100$ μV when loaded by the comparator's output buffer.

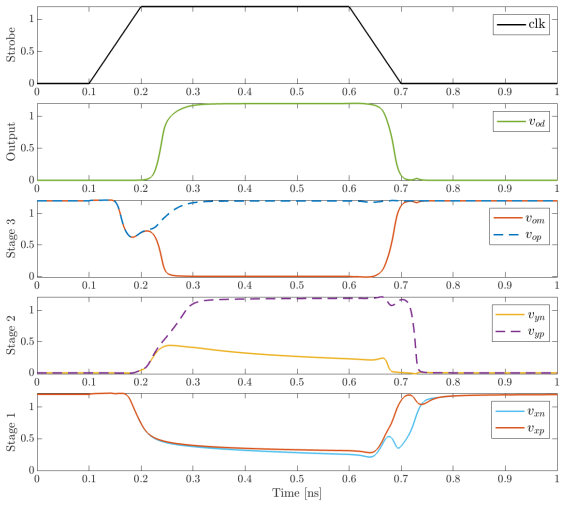


Fig. 6. Transient response of comparator node voltages (loaded by output buffer) with a fixed differential DC input of $v_{id} = 100$ μV and a common mode of $V_{\mathrm{CM}} = 0.5$ V.

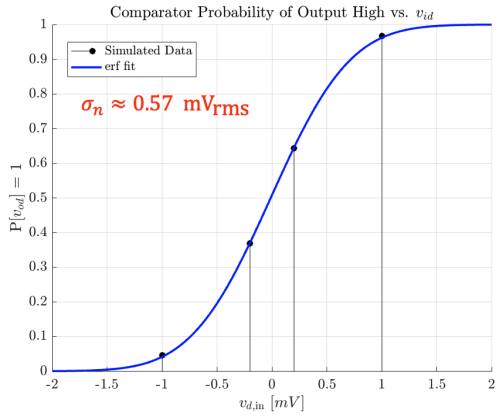


Fig. 7. Extraction of comparator input referred noise voltage by fitting of the error function (ERF).

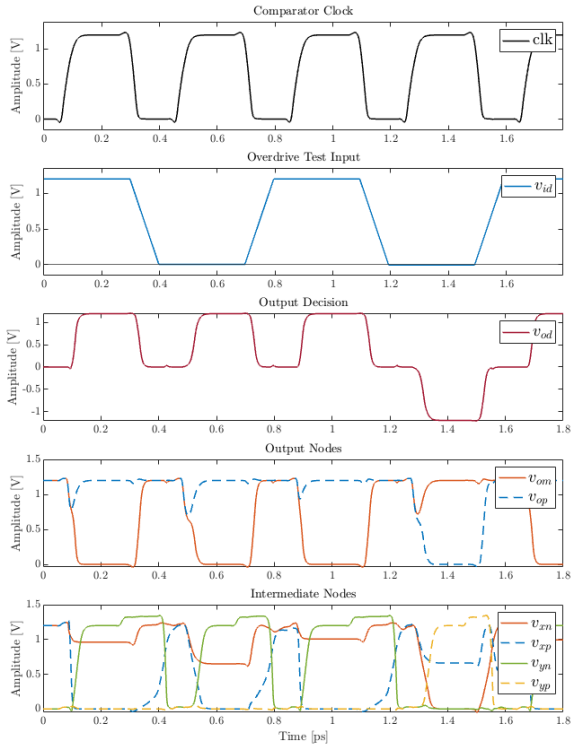


Fig. 8. Overdrive recovery test (ORT) of the proposed comparator when synchronously operated at $f_c = 1.68$ GHz (corresponding to $f_s = 140$ MHz). In the ORT, a maximum differential input of $v_{id} = V_{DD}$ is applied, followed by $v_{id} = +\text{LSB}$, $v_{id} = V_{DD}$, and finally $v_{id} = -\text{LSB}$ in sequential clock cycles.

Solving for f_c yields the maximum allowable comparator clock frequency such that $P_{meta} = 10^{-7}$:

$$f_c = -\frac{B}{2\tau} \cdot \left[\ln \left(\frac{P_{meta} \cdot A_v \cdot V_{FS}}{V_{DD} \cdot 2^{B+1}} \right) \right]^{-1} \approx 28.3 \text{ GHz} \quad (10)$$

Reserving two clock cycles for the sampler tracking time, the maximum theoretical sample rate is $f_{s,\max} \approx 2.36$ GHz. The implemented sample rate is substantially lower at $f_s = 140$ MHz, and is limited by SNDR performance of the entire SAR ADC.

3) Overdrive Recovery: To demonstrate the robustness of the proposed comparator, an overdrive recovery test (ORT) is executed at the sample rate of $f_s = 140$ MHz to test if the comparator successfully returns to its normal operating point after being driven far beyond its linear input range. The speed of a comparator is often limited by overdrive recovery, as this captures the nonlinear memory effects due to insufficient comparator resets, which may lead to wrong output decisions [13]. The ORT is performed using synchronous operation, as this conservatively stresses the performance of the comparator. As shown in Fig. 8, the proposed comparator successfully passes the ORT at the design sample rate of 140 MS/s.

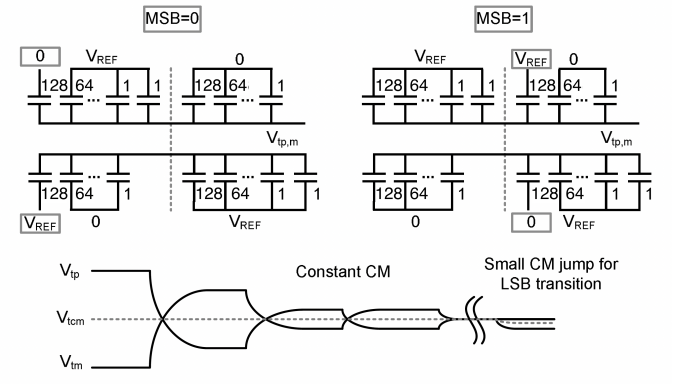


Fig. 9. DAC switching.

C. Capacitive DAC

The Capacitive DAC (CDAC) is implemented as a split capacitor array (two binary weighted arrays sharing the same top-plate node) so that the symmetric, monotonic switching scheme can be used, as described in [2]. Top-plate sampling allows for the first comparison to be setup immediately after the track and hold block has held onto the current sample. Accordingly, the MSB capacitance of the CDAC can be removed, so a 9-bit CDAC is used, yielding significant power savings. Note that an ADC resolution of 10 bits was selected so that a SNDR near 55 dB was achievable after degradation of the 62 dB SQNR by thermal noise and circuit nonlinearities. The monotonic switching scheme is chosen due to its further power savings. Finally, the split capacitor implementation, as illustrated by Fig. 9 (courtesy of [3]) keeps the common mode on the CDAC roughly constant, easing the Common Mode Rejection Ratio (CMRR) and headroom requirements of the comparator.

The capacitors are implemented with MIM-capacitors possessing a 1% top-plate parasitic capacitance to substrate and a 10% bottom-plate parasitic capacitance to substrate. Due to technology limitations, a C_{min} of 2.5 fF is the lower bound for the unit capacitance available for the design. The primary trade-off with the unit capacitor sizing (not considering mismatch) is between the CDAC power consumption and kT/C sampling noise. Larger capacitance consumes more power, however also reduces the sampling noise. Significant effort in making the comparator low-noise allowed for using C_{min}, thus saving power. It is important to note that if mismatch is a factor, as is typically the case, the unit capacitance may need to be increased or other system level approaches may need to be adopted to meet linearity requirements.

A V_{ref} of 1 V (near V_{DD} of 1.2 V) was chosen to help ease the thermal noise requirements of the ADC (which often has significant contribution from the comparator), as larger signal swing improves SNR. However, the tradeoff is that the larger swing necessitates system linearity over a wider range, which increases T/H design complexity and consumes more power. Though not relevant here, in practice V_{ref} is kept below V_{DD} by some margin to ease the headroom requirements of the amplifier that typically precedes the ADC.

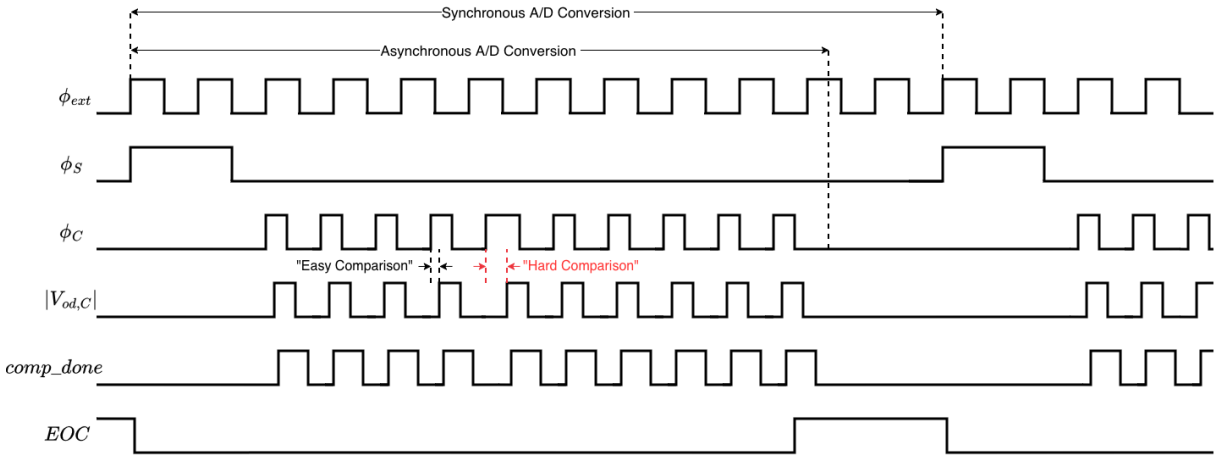


Fig. 10. Asynchronous conversion timing diagram with comparison to synchronous conversion.

For the chosen architecture, V_{FS} can be expressed as

$$V_{FS} = 2\left(V_{ref} \times \frac{C_{DAC}}{C_{DAC} + C_P}\right) \tag{11}$$

where C_{DAC} is the CDAC capacitance and C_P is the parasitic capacitance at the top-plate node. Contributions to C_P include parasitics from the T/H, MIM-cap top-plate, and the comparator input. Using Eq. 11, a V_{FS} of 1.95 V is found.

The CDAC switch connecting the bottom plate of each CDAC capacitor to either V_{ref} or V_{SS} is implemented as an inverter. The PMOS pulls the bottom-plate to V_{ref} and the NMOS to V_{SS} with the width sizing of each device chosen such that the CDAC settles (for either a connection to V_{ref} or V_{SS}) before the next comparison by the comparator. Minimum length devices are used to minimize the on-resistance. The primary tradeoff in the inverter sizing is that wider devices improve the DAC settling time during redistribution, but also increase the SAR logic load, and thus delay. As a result, an optimum sizing exists that minimizes the combined delay, noting that the optimum is shallow so extreme precision is not necessary [3].

D. Asynchronous SAR Logic

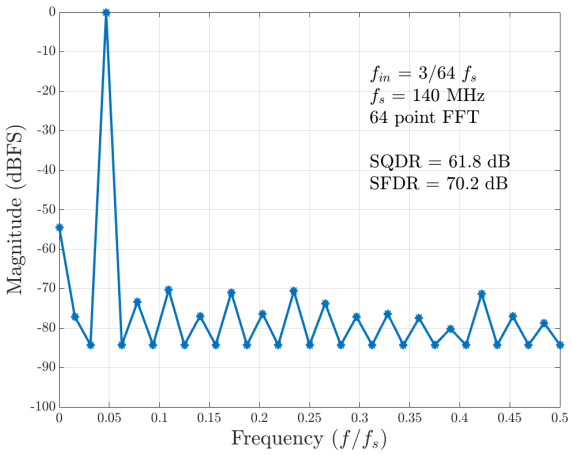
The primary motivation for operating the ADC asynchronously is that it allows for a significant increase in f_s for the same metastability probability requirement. Synchronous operation allocates sufficient time for the comparator to resolve a "hard comparison" for each comparison window, whether it is needed or not, since there is no easy way to know if a comparison will be difficult apriori. In contrast, the asynchronous approach allocates just the amount of time needed for the comparator to resolve. Since most comparisons within a conversion are "easy" and resolve quickly, substantial time savings accrue for asynchronous operation, enabling higher f_s operation. Fig. 10 shows a timing diagram containing critical waveforms for a typical ADC conversion with corresponding circuit nodes shown in Fig. 1.

In this ADC implementation the T/H clock, ϕ_s, is generated as 1.5 clock periods of an external clock, ϕ_{ext}, which itself runs at a frequency 12 times greater than f_s. This was chosen to reduce the ADC timing design complexity. However, in practice, many asynchronous designs only use the rising edge of an ADC conversion sampling clock running at f_s to save power and simplify external clock generation [14]. In such cases, delay lines are often used to generate the pulse needed during the track phase of the conversion.

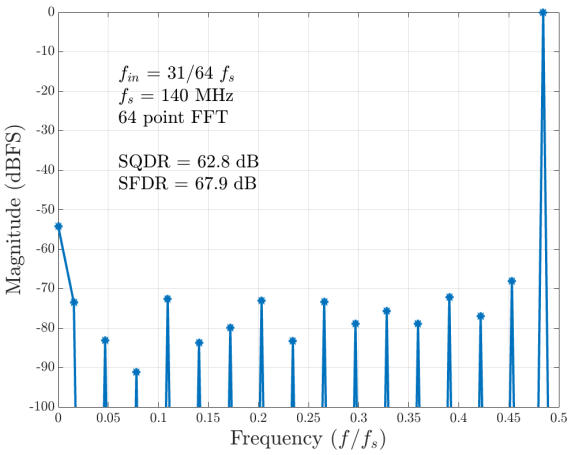
Once ϕ_s goes low, after the propagation delay of the three input NOR gate in Fig. 1, the comparator clock, ϕ_c, goes high. This causes the comparator to evaluate its input, and after sufficient regeneration time and the propagation delay through the comparator output buffer, a resolved, digital signal is presented to the SAR logic and the NAND gate. After the propagation delay through the NAND gate, the $comp\_done$ signal goes high, forcing ϕ_c to go low and enabling the SAR logic to begin switching the next capacitor as required to setup the next comparison in the binary search process. Because ϕ_c is low, the comparator resets causing both of its outputs to go high. After associated gate delays, $comp\_done$ goes low, which creates a rising edge of ϕ_c and completes the process of generating one comparator clock pulse.

Notably, this clock generation is self-sustaining and will continue even after the ten comparisons have occurred unless intervened. Thus, after the final comparison of the conversion, the SAR logic generates an End-of-Conversion signal, EOC, that forces ϕ_c to stay low until the next ADC conversion. When ϕ_s goes high, EOC is reset to low to prepare for the next conversion, however ϕ_s also forces ϕ_c low so that the comparator does not start comparing until after the T/H has held onto the sample.

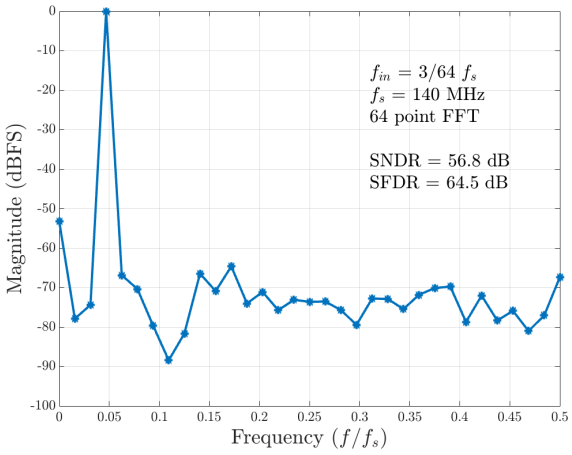
Despite asynchronous operation being faster than synchronous, there are still limitations on the timing generation. As just described, the generation of ϕ_c depends on the propagation delays of gates in the loop, and the regeneration and reset durations of the comparator. Even if the CDAC could settle immediately after switching, the delays of gates in the loop pose a fundamental limitation on the maximum f_s that can be synthesized. After optimizing the gates and comparator buffer to minimize delay, we achieved a maximum f_s of 140 MHz. The T/H and CDAC switches were accordingly sized



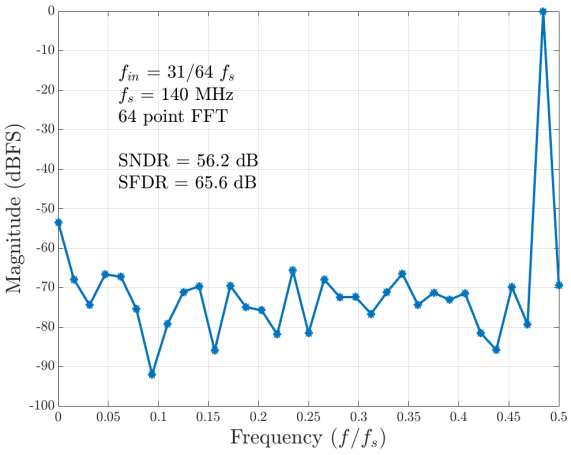
(a) Low-frequency input (noiseless)



(b) Nyquist input (noiseless)



(c) Low-frequency input (with noise)



(d) Nyquist input (with noise)

Fig. 11. Measured output spectrum, SQDR/SNDR, and SFDR from transient simulations. Top row: noiseless simulations. Bottom row: simulations with noise.

to ensure sufficient settling of the CDAC to meet the SNDR specification.

An important consideration in a design that would be fabricated is the robustness of the timing generation across process, voltage, and temperature (PVT). Since the generation of ϕ_c depends on gate delays which can vary substantially across PVT, it becomes more involved to ensure that the CDAC has enough time to settle and that ten comparisons will occur before the next ADC sample.

III. Simulation Results

The design described in the previous section was implemented in Cadence Virtuoso and simulated under multiple test conditions to evaluate the ADC performance. Fig. 11 shows the measured output spectrum of transient simulations of the ADC operating at a f_s of 140 MHz and for a full-scale input signal at low frequency and near Nyquist with and without noise. SNDRs of 56.8 dB and 56.2 dB and SFDRs of 64.5 dB and 65.6 dB were achieved for low-frequency and Nyquist input signals respectively, indicating that the design meets the SNDR specification. See Appendix A for the testbench used.

TABLE I
Power Breakdown by ADC Sub-Block

ADC Sub-Block	Average Power (μW)	Percent of Total (%)
T/H	25	2.8
CDAC	181	20.6
Comparator + Buffer	310	35.2
SAR Logic + Timing	364	41.4
Total	880	100

The average power of each ADC sub-block is given by Table I. Each average power was obtained by determining the average current from the supply for the sub-block for 30 ADC conversions, then multiplying it by the supply voltage. The input signal was full-scale and just below Nyquist frequency, with f_s set at 140 MHz. It is seen that the T/H's power consumption is very minor, the contribution of the CDAC is moderate, while the comparator and SAR logic and timing blocks consume the majority of the power.

TABLE II
SPECIFICATIONS ACHIEVED

Specification	Achieved Result
Technology (nm)	90
Supply Voltage (V)	1.2
V_{ref} (V)	1
Full Scale Range (V)	1.95
Input CM Voltage (V)	0.50
Unit Capacitance (fF)	2.5
Sampling Capacitance (pF)	1.28
Resolution (bits)	10
f_s (MS/s)	140
SNDR at LF (dB)	56.8
SNDR at Nyq (dB)	56.2
SFDR at Nyq (dB)	65.6
ENOB	9.04
Average Power (μW)	880
FOM (W/Hz^2)	$4.49x10^{-20}$
FOM_W (fJ/con-step)	12
FOM_S (dB)	165
Metastability Rate	$< 10^{-7}$

IV. CONCLUSION

This work presented the complete design and validation of a fully-differential asynchronous SAR ADC in 90 nm CMOS technology. A high-linearity bootstrapped track and hold stage, followed by a high-speed triple-stage dynamic comparator were optimized to enable high sampling rates at moderate power consumption. Asynchronous SAR logic was implemented in order to realize the highest possible sampling speeds for a target metastability rate of 10^{-7}. Table II consolidates the key specifications achieved by the design. Notably, this work attains a 140 MS/s operating speed at a power consumption of 0.88 mW, yielding a FOM of $4.49x10^{-20}$ W/Hz^2 and a SNDR of 56.2 dB at Nyquist. While this design is a good starting point, component mismatch, circuit robustness across PVT, and other "real world" non-idealities should be examined closely to ensure that the ADC continues to meet performance specifications.

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Nihar Ahire received the B.E. degree in electrical and electronics engineering from the Birla Institute of Technology and Science, Pilani, India, in 2024. He is currently pursuing the M.S. degree in electrical engineering at Stanford University, Stanford, USA, with a focus on analog and mixed-signal IC design.

Aiden Duncanson received the B.A. degree in physics from Colby College, Waterville, USA in 2023 and the B.E. degree in electrical engineering from Dartmouth College, Hanover, USA in 2024. He is currently an M.S. student at Stanford University, Stanford, USA in the department of electrical engineering where he studies analog mixed-signal integrated circuit design.

Austin Rothschild received the B.S. degree in electrical engineering from Santa Clara University, Santa Clara, USA in 2021. He is currently pursuing an M.S. in electrical engineering at Stanford University, Stanford, USA, where he is focusing on high-speed analog circuits for wireless and wireline applications. Prior to joining Stanford, he was a Senior RF Design Engineer at Tesla, Inc. in Palo Alto, CA from 2021-2024.

APPENDIX A
TESTBENCHES, BLOCK-LEVEL SCHEMATICS, AND MISCELLANEOUS CIRCUITS

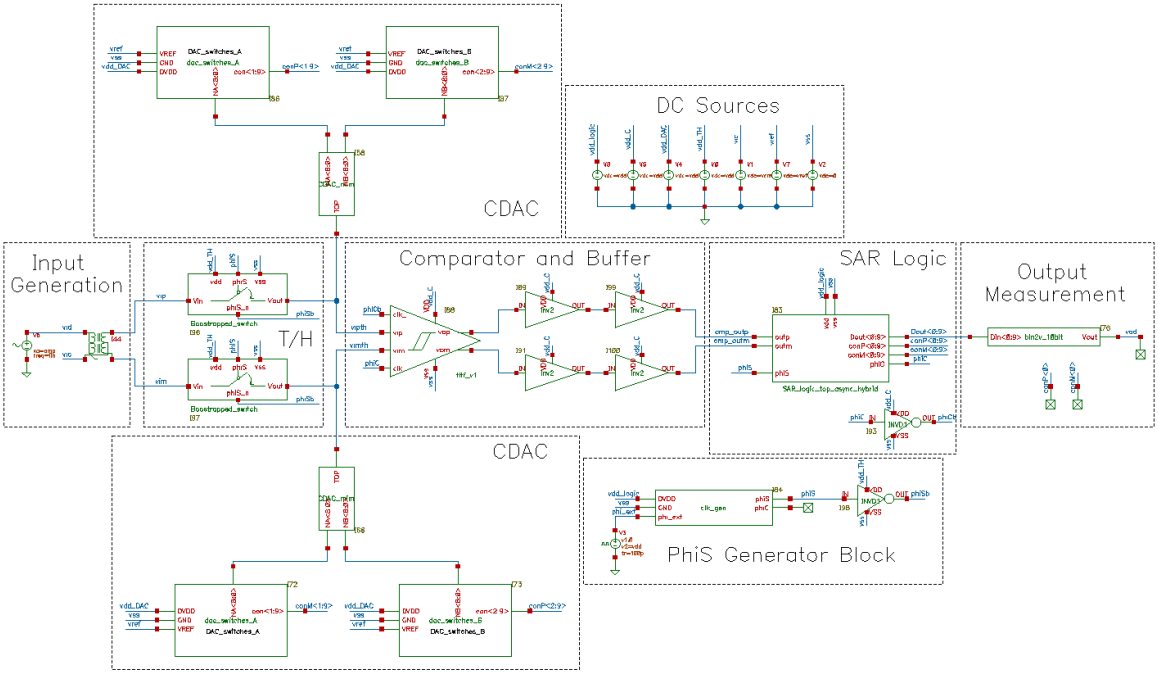

Fig. 12. Testbench used for testing the ADC. Separate voltage sources, all at V_{DD}, are used to measure the power each sub-block consumes more easily.

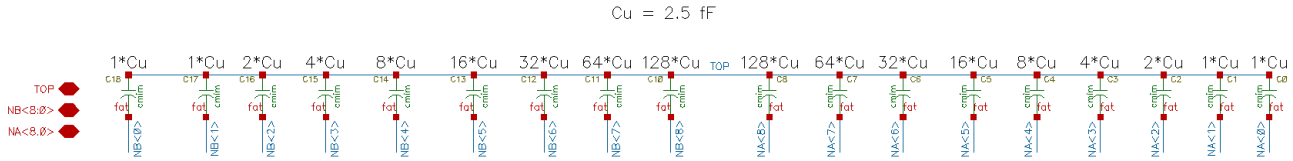

Fig. 13. CDAC sampling capacitance implemented with MIM capacitors and as a split capacitor array with sizing shown.

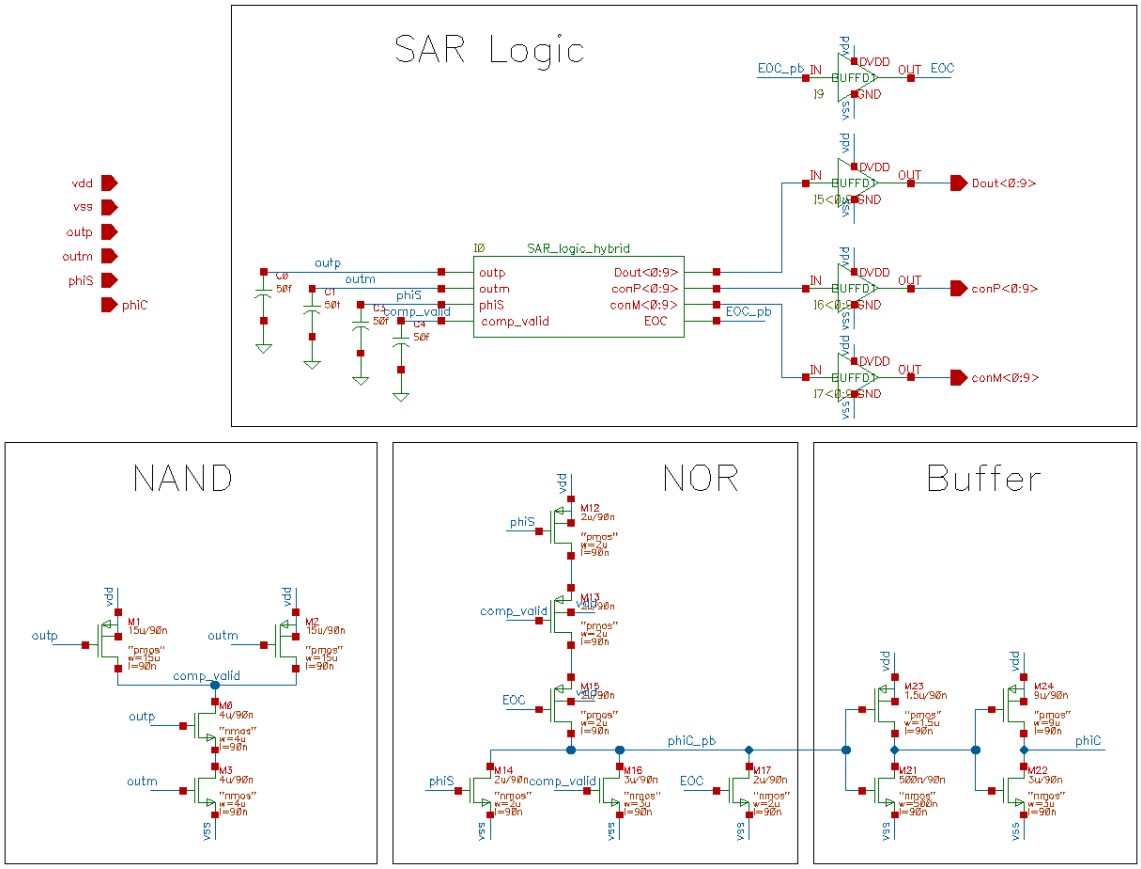

Fig. 14. SAR logic Verilog-A wrapper and asynchronous clock generator for the comparator.

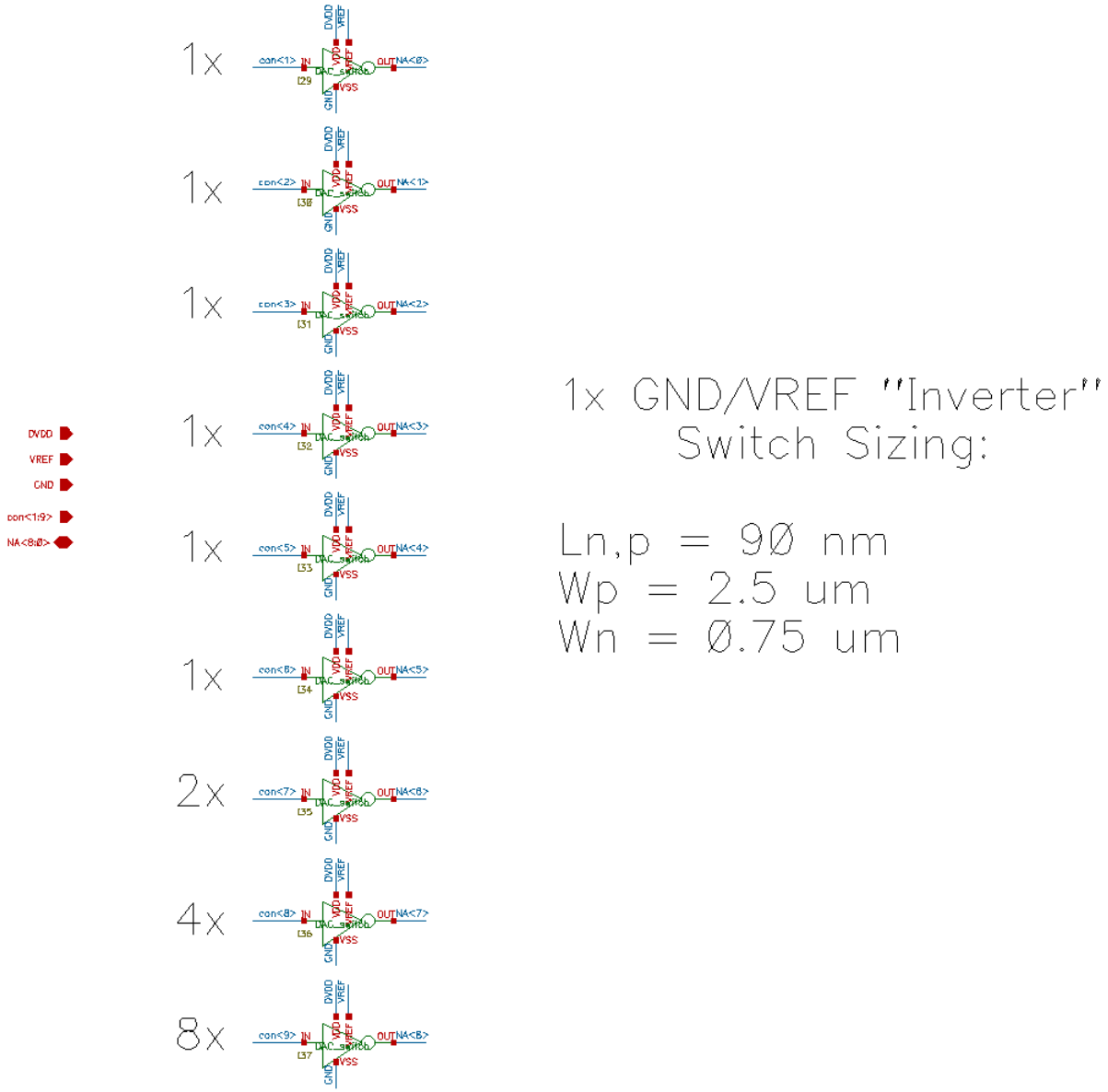

Fig. 15. Modified DAC_switches_A schematic.

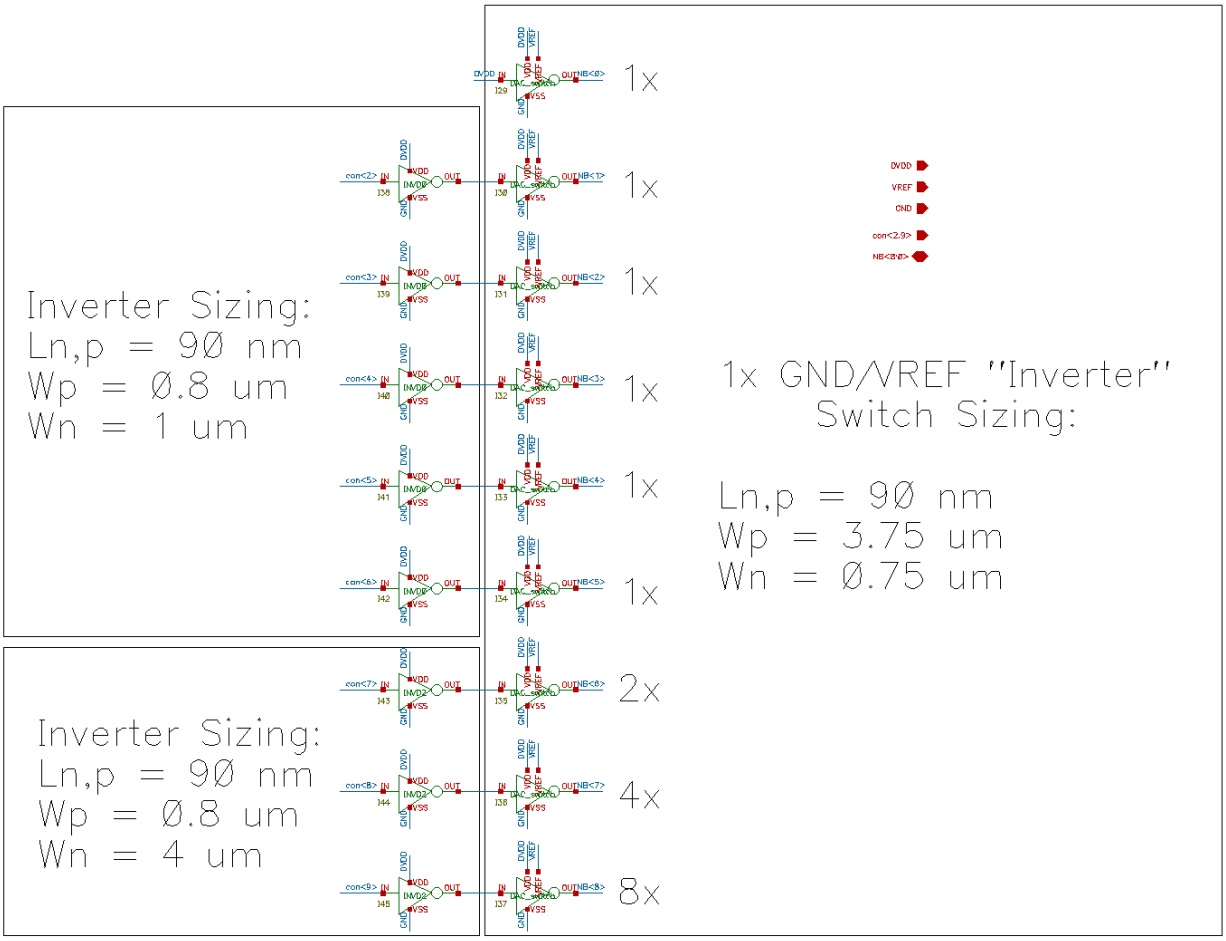

Fig. 16. Modified DAC_switches_B schematic.

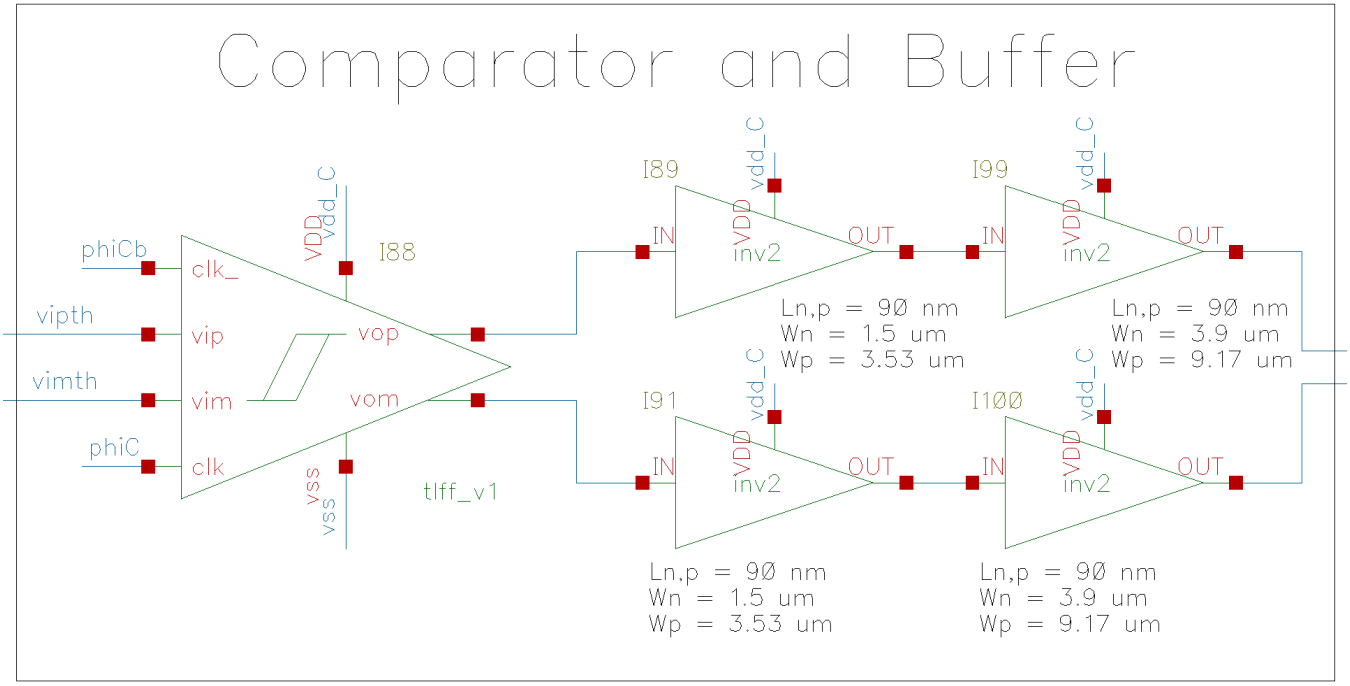

Fig. 17. Comparator output buffer device sizing.

APPENDIX B
SAR LOGIC MODIFIED VERILOG-A CODE

```
//  VerilogA for SAR logic asynchronous

`include "constants.vams"
`include "disciplines.vams"

module SAR_logic_hybrid(phiS, outp, outm, comp_valid, EOC, Dout, conP, conM) ;

        output [0:9] Dout;
        output [0:9] conP;
        output [0:9] conM;
        output EOC;

        input phiS, outp, outm, comp_valid;

        electrical [0:9] Dout;
        electrical [0:9] conP;
        electrical [0:9] conM;
        electrical phiS, outp, outm, EOC, comp_valid;

        parameter integer bits = 10;
        parameter real tL = 80p from [0:inf); // models logic delay, do not change
        parameter real vh = 1.2;
        parameter real vl = 0.0;
        parameter real tt = 50p from [0:inf); // transition time, do not change

        real adc_out[0:bits-1], dac_controlP[0:bits-1], dac_controlM[0:bits-1],
           EOC_int;

        integer i, index, state;
        genvar j;

        analog begin

        @(cross(V(phiS)-0.5*vh, +1)) begin
                index = bits-1;
                state = 0;
                EOC_int = vl;
                for(i=bits-1; i>=0; i= i-1) begin
                        dac_controlP[i] = vl;
                        dac_controlM[i] = vl;
                        adc_out[i] = vl;
                end
        end

        @(cross(V(phiS)-0.5*vh, -1)) begin
                state = 1;
        end

        @(cross(V(comp_valid)-0.5*vh, +1)) begin
                if (index >=0 && state==1) begin
                        if((V(outp)-V(outm)) > 0.9*vh) begin
                 adc_out[index] = vh;
                                dac_controlP[index] = vh;
                                dac_controlM[index] = vl;
                        end
```

```
            if((V(outp)-V(outm)) < -0.9*vh) begin
                adc_out[index] = vl;
                                dac_controlP[index] = vl;
                dac_controlM[index] = vh;
                        end
                        if (index == 0) begin
                                EOC_int = vh;
                        end
            index = index-1;
        end
        end

        // transitions outputs as needed
        for (j=0; j<bits; j=j+1) begin
            V(conP[j]) <+ transition(dac_controlP[j], tL, tt);
            V(conM[j]) <+ transition(dac_controlM[j], tL, tt);
            V(Dout[j]) <+ transition(adc_out[j], tL, tt);
        end

        V(EOC) <+ transition(EOC_int, tL, tt);

end
endmodule
```