International Journal of Pure and Applied Mathematics
Volume 118 No. 20 2018, 3875-3879
ISSN: 1314-3395 (on-line version)
url: http://www.ijpam.eu
Special Issue

ijpam.eu

LDPC Decoder's Error Performance over AWGN Channel using Min-Sum Algorithm

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***Abstract*— Low Density Parity Check (LDPC) code meets the desired Shannon limit performance for extended code lengths and binary fields. LDPC codes offer noteworthy error correction performance and they also increase the design space for communication systems. LDPC codes can offer a close proximity to Shannon Limit performance, when execution complexity and latency are not system boundaries, by using large code lengths and ever-increasing the number of iterations in the decoding process. In this paper, using 16-Quadrature Amplitude Modulation (QAM) modulation technique an LDPC decoder is simulated. It further provides the error performance of LDPC decoder over AWGN channel with Min-Sum algorithm (MSA) and their effects on Bit Error Rate (BER) versus Signal to Noise Ratio graph (SNR).**

Keywords: Low-Density Parity-Check (LDPC) codes, Min-Sum Algorithm (MSA), Signal to Noise Ratio (SNR), Bit Error Rate (BER), 16-Quadrature Amplitude Modulation (16-QAM), and AWGN.

I. INTRODUCTION

Low Density Parity-Check (LDPC) codes are recognized as they are the most powerful forward error correction codes, whose bit-error-rate (BER) performance is very near to the Shannon limit. LDPC codes are proved to have better performance and quite a lot of advantages over other error correction codes such as Hamming codes, Turbo codes, Reed-Solomon and Reed-Muller codes. LDPC codes are broadly used in many applications such as Terrestrial television broadcasting system, digital satellite and Digital Video Broadcasting. Though the decoding algorithm in LDPC is modest, but as we go on increasing the block length LDPC matrix becomes larger, and it is time consuming to physically connect and test the connections. As a result, an automated high level design methodology is presented to surmount it. This methodology is being used in designing and implementing LDPC decoders on FPGAs. A testing strategy is also been developed to test the designed decoders at various levels of its abstraction. The challenging parameter in designing of a fully parallel LDPC decoder is its complexity between its nodes inside the decoder. As we go on increasing the block length it becomes almost difficult and time taking to physically connect and check the interconnections.

In this paper an automated high-level design approach is introduced. We are using MATLAB Simulink for modeling the LDPC decoder .The designing and testing of LDPC decoder is done using high-level modeling tool. The paper is organized as follows. Section II presents the previous work done in Min-Sum algorithm. Section III explains Min Sum Algorithm. Design methodology for developing LDPC decoder in MATLAB Simulink is given in section IV. Simulation results are covered in Section V and VI draws conclusion to the paper.

II. PREVIOUS WORK

LDPC decoder uses various Message passing algorithm for decoding information, among them Min-Sum algorithm is broadly categorized as shown in figure 1. The overall top-level diagram is shown in figure 2, which indicates the flow of information from transmission to its reception. The bits to be sent are generated as k×G where the message of k bits gets multiplied by G-matrix also called as generator matrix. LDPC codes have code rate which is represented by k/n. Here k is the number of original bits in the message and n is the total encoded information.

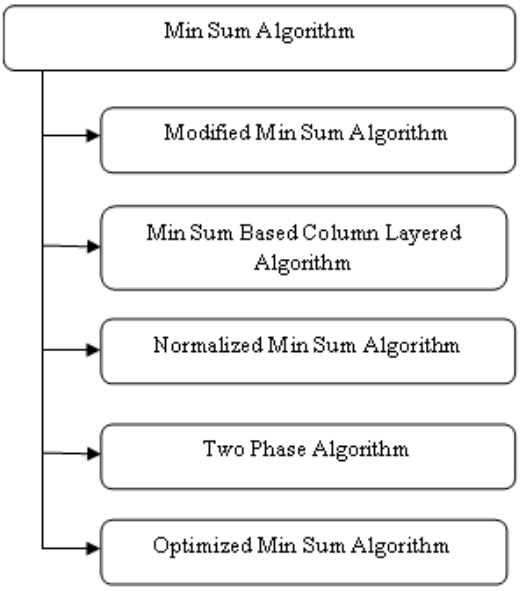

Fig. 1.Versions of Min-Sum Algorithm

The n bits are directed by a transmitter over an AWGN (Additive White Gaussian Noise) channel, at receiving end decoder decodes the n-bits using message passing algorithm to obtain original k bits. The LDPC Codes are represented by Tanner Graphs. The sparse parity check matrix is as shown in Figure 4 and its corresponding tanner graph is as shown in Figure 3.

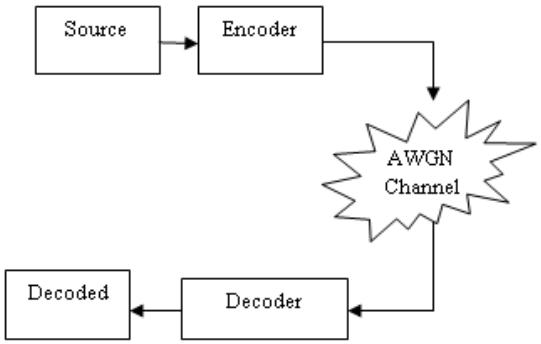

Fig. 2. Top level block diagram

LDPC codes can be denoted by an M x N matrix, typically called H-matrix. The H matrix contains generally zeros and a small number of 1's [1], [2]. It is also represented by a graph called tanner or bipartite graph as shown in Fig. 3.Because of exceptional BER, LDPC codes are comprehensively used in standards such as 10Gigabit Ethernet, Wi-MAX, Digital video broadcasting (DVB-S2) and anticipated to be part of many forthcoming standards [3].

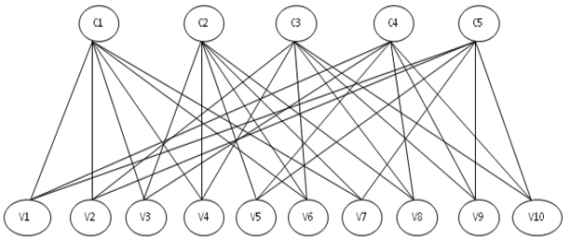

Fig. 3. Tanner graph

$$\begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

Fig. 4. Parity check matrix

The Min-Sum algorithm (MSA) [4] is the modified version of the Sum-Product algorithm (SPA) [4]. Min-Sum algorithm has a simplified operation which reduces the complexity of the algorithm. The check node operation is simplified [4]. Min-Sum algorithm is helpful in designing of semi-parallel architecture this saves the hardware resources while implementing on FPGA [5]. The advantage of fully parallel architecture is high throughput and it does not need memory to store results .Thus, fully parallel architecture is also power efficient. But partially parallel architectures have comparatively lower throughput. However, the decoding circuit is much smaller and area efficient [5]. Error correction algorithms are often realized in hardware for fast processing to meet the real-time needs of communication systems. Though, traditional hardware implementation of LDPC decoders need large amount of resources. Due to the complex interconnections among the variable and check nodes of LDPC decoders, it is very time consuming to use earliest hardware description language (HDL) based approach to design LDPC decoders [6]. So it is possible to use assisting tools in this development. In order to test and validate the design simple MATLAB application can be used for higher block length [7].It is very difficult to simulate and test the whole design in HDL especially when the block length of the design becomes large. Due to this, for validation purpose the complete design will be implemented in MATLAB [8]. As shown in Fig.5 the simulation of LDPC decoder is done in MATLAB Simulink using MATLAB script. Simulink model of LDPC decoder can be analyzed using MATLAB script.

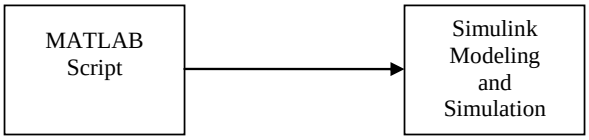

Fig. 5. Simulink co-simulation

III. Min Sum Algorithm

The LDPC encoder encodes an input binary message k into n-bit LDPC codeword. At the decoder end min-sum algorithm is used as message passing algorithm. Decoder performs iterations for parity check. Likewise, Check node (CN) and Variable node (VN) are updated as shown in step2 and step3. LLR's (Log Likelihood Ratio) are exchanged as messages between CN and VN. The LLR of VN is performed by step 4. The options for Decision type are Hard and Soft decision. When you set this parameter to hard decision, the output is decoded bits. Figure 6 explains the flow.

Step 1: $HX^T = 0$

Step 2: $L_{m\to n}(x_n) \approx \prod_{n'\in N(m)\backslash n} sign(Z_{n'\to m}(x_{n'}))$

$$(\min_{n'\in N(m)\backslash n}(|Z_{n'\to m}(x_{n'})|))$$

Step 3: $Z_{n\to m}(x_n) = L(x_n \mid y_n) + \sum_{m'\in M(n)\backslash m} L_{m'\to n}(x_n)$

Step4: $Z_n(x_n) = L(x_n \mid y_n) + \sum_{m' \in M(n)} L_{m' \to n}(x_n)$

Step5: Hard Decision

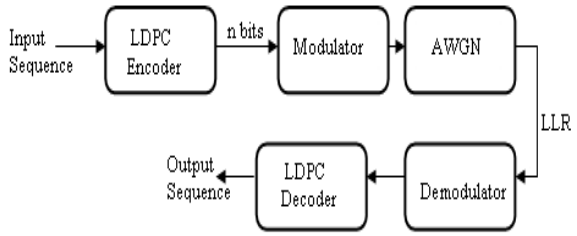

Fig. 6. Min-Sum Algorithm flow

IV. DESIGN METHODOLOGY

Efficient implementation of higher Block length LDPC decoder is a time consuming process to overcome, it we have designed LDPC encoder and decoder in MATLAB Simulink. Using blocks in Simulink library, where we provided streams of data in matrix form of block length (32400, 64800) using Bernoulli Binary packet source which provides less number of 1's and more 0's.

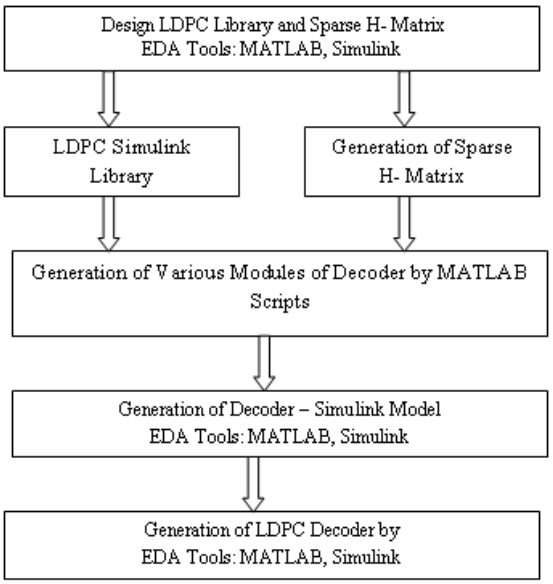

Fig. 7. Design Flow

The encoded data from LDPC encoder further is provided to 16-QAM modulator which provides high speed transmission of data i.e. 4 bits per symbol. Channel selected here is AWGN (Additive White Gaussian Noise) with 11dB SNR for error free signal at the output.Fig.7 shows the precise design flow for designing and simulating a (32400, 64800) block length LDPC decoder. The testing method for generating the MATLAB script is as shown in figure 8. For various values of Signal to Noise Ratio (SNR) we get respective Bit Error Rate (BER) using the above given testing flow. It provides a platform for evaluating the LDPC codes performance near to Shannon limit.

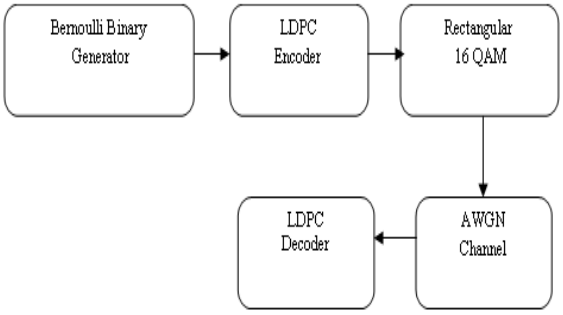

Fig. 8. Testing Flow

V. MATLAB IMPLEMENTATION

As the model starts simulating, a constellation window appears on the command window showing a scatter plot of 1 received data. For every received data at the LDPC decoder, bit error rate, channel SNR and packet error rate is continuously updated. You need to go on increasing SNR to get an error-free output signal and less noisy plot.

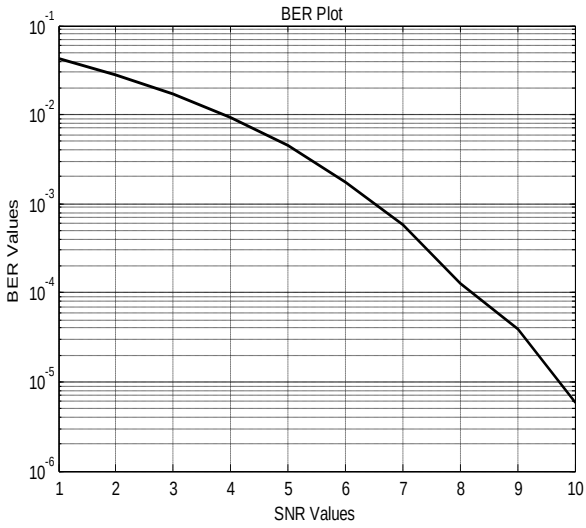

Fig. 9. Simulation result for 16-QAM modulation scheme over AWGN channel for (32400, 64800).

The higher value of SNR the better is the BER. Eb/No is easily selectable typically in the range of -5 to 20 dB. For -5 dB you will receive an erroneous data and for 20 dB the data received is error-free. Fig. 9 demonstrates Simulation plot for 16-QAM modulation scheme over AWGN channel for block length (32400, 64800) and SNR ranging from 1-11 dB and Fig. 10 illustrates the Received constellation for the same.

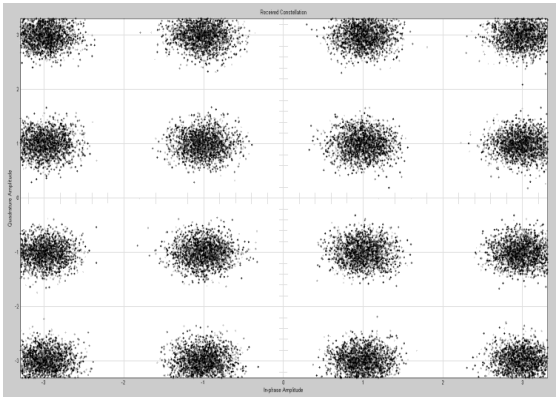

Fig. 10. Received constellation for 16-QAM modulation scheme over AWGN channel for (32400, 64800).

VI. CONCLUSION

In this paper, a brief overview of Min Sum Algorithm based LDPC decoder is presented. Among various message passing algorithms, one of the vital algorithms is Min Sum which provides suitability for implementation of Decoder with less area. Also the Bit Error Rate calculated for 16-QAM is from 10^{-1} to 10^{-6} for SNR 1 to 11dB. The high level methodology has helped in designing LDPC decoder for 16-QAM modulation scheme for wireless network.

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