1)

2)
$$50000 + 75x = 450,000 + 42x$$
$$33x = 400,000$$
$$\$ 12121.21$$

3) Clock
4) Mod port
5) S interpritation

6)

T	A	B	C	D	E	F	
0	0	?	C	?	20	?	
15	0	T	6	?	15	1	C <= 1 to 6
15	5	?	6	?	15	1	A := A+5
16	5	?	6	?	20	1	E: A+5
15+Δ	5	?	6	?	20	6	f <= CA+5
19	5	23	6	?	20	6	B <= E+3
25	5	23	6	8	20	6	D <= C+2

7) false
8) true
9) fan out
10) 'event

11)
```
interface serial (input bit clk);
    logic TxD, RxD, RTS, CTS, DSR, DTR, DCD, RI;

    clocking cb (negedge clk);
        output TxD, RTS, DTR;
        input RxD, CTS, DSR, DCD, RI;
    endclocking
endinterface
```

12) embedded

13) random

14)
```
architecture behave of euclid is
    type state_type is (idle, load, calc, finish)
    registers X (15:0), Y (15:0)
begin
    X <= X,
```

16) True

17) Generic

18) false

T	A	B	C	D	E	F		
0	0	1	1		20			
15	0	1	6		15	1	ti= 6	
15	1		6		15	1	A=1	
15	6							

21	A	1/8
	B	1/8
	C	1/8
	D	1/8
	E	0
	F	1/6
	G	1/6
	H	1/6
	I	1/6
	J	1/6
	K	1/6
	L	1/6
	M	1/6
	N	1/6
	O	1/6
	P	1/6