The University of Alabama in Huntsville Electrical & Computer Engineering CPE 426/526 February 10, 2021 Combinational Modeling

Due February 17, 2021

Cryptographic applications commonly require circular shifts. Whereas these shifts can be accomplished using a shift register, combinational shifting is required to complete these operations in a reasonable amount of time. Design an 8 bit barrel shifter that has 8 data inputs and 8 data outputs, and 3 control inputs that determine the shift amount (0-7). An additional enable input controls whether the outputs are tri-state or not. Use the truth table below as the functionality and use the entity declaration given.

en	s2	s1	s0		c7	с6	с5	с4	с3	c2	c1	c 0
0	0	0	0	-	a7	a6	a5	a4	a3	a2	a1	a0
0	0	0	1	ć	a0	a7	a6	a5	a4	a3	a2	a1
0	0	1	0	ė	a1	a0	a7	a6	a5	a4	a3	a2
0	0	1	1	ć	a2	a1	a0	a7	a6	a5	a4	a3
0	1	0	0	ć	a3	a2	a1	a0	a7	a6	a5	a4
0	1	0	1	ė	a4	a3	a2	a1	a0	a7	a6	a5
0	1	1	0	ć	a5	a4	a3	a2	a1	a0	a7	a6
0	1	1	1	ć	a6	a5	a4	a3	a2	a1	a0	a7
1	0	0	0		Z	Z	Z	Z	Z	Z	Z	Z
1	0	0	1		Z	Z	Z	Z	Z	Z	Z	Z
1	0	1	0		Z	Z	Z	Z	Z	Z	Z	Z
1	0	1	1		Z	Z	Z	Z	Z	Z	Z	Z
1	1	0	0		Z	Z	Z	Z	Z	Z	Z	Z
1	1	0	1		Z	Z	Z	Z	Z	Z	Z	Z
1	1	1	0		Z	Z	Z	Z	Z	Z	Z	Z
1	1	1	1		Z	Z	Z	Z	Z	Z	Z	Z

Use the following entity

```
entity barrel is
  port (a : in std_logic_vector (7 downto 0);
        s : in std_logic (2 downto 0;
        en : in std_logic;
        c : out std_logic_vector (7 downto 0));
end entity barrel;
```

Develop a behavioral architecture for the system.

Perform the following steps

- a. Modify the test bench given in homework #1 to test this circuit.
- b. Compile all of the files
- c. Simulate to verify correctness.

Turn in all VHDL files.