FINAL EXAM

EE315- FALL 2017

NAME________________________________

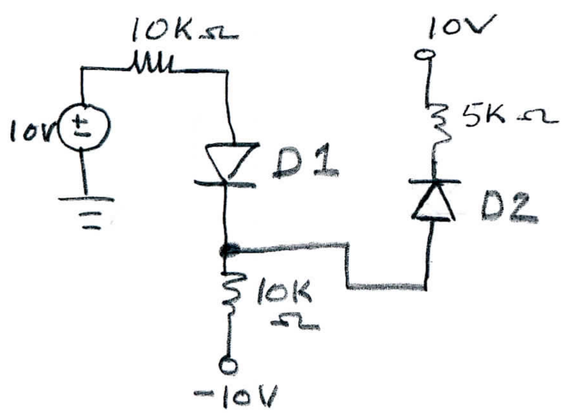
DO ALL YOUR WORK ON THIS EXAM.USE THE BACK SIDES OF EXAM PAPER IF NECESSARY BUT POINT ME WHERE YOU DID THAT.

- **YOUR EQUATION CHEAT SHEET MUST BE TURNED IN WITH EXAM .**
- **NO CELL PHONE CALCULATORS ALLOWED. OTHER CALCULATORS OK.**
- **No laptop computers or abacuses**
- **CLOSED BOOK/CLOSED NOTES**
- **EACH PROBLEM WORTH 10 POINTS**

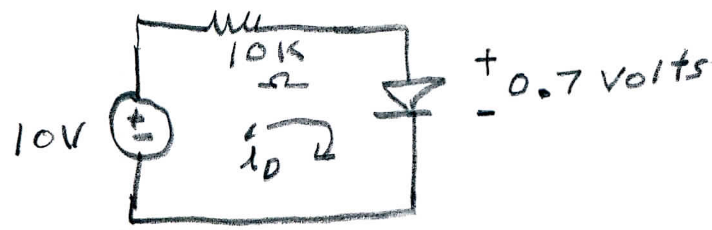
Actually, in order to become a first rate professional engineer, it helps to start studying really late for all your exams. Then, you begin to eventually learn how to manage your time and tackle emergencies.

Unknown originator.

1. (no part credit- no credit for guessing) My good classmate friend who graduated from the Loachapoka University School of Engineering tells me that diodes D1 and D2 in the circuit below are both Forward Biased. (the circuit is to be used as a critical part of a heart pacemaker). Is my friend correct, yes or no?



2. **Using the exponential equation for silicon semiconductor diode find Is, the reverse saturation current for the diode. Given that Vd as shown is 0.7 volts and assume room temperature.**

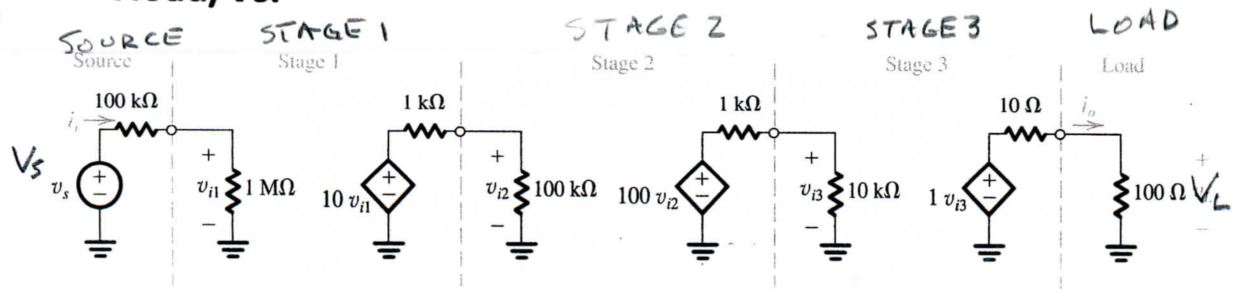


Recall

$$i_D = I_S e^{V_D/V_T}$$

3. **For the cascade amplifier circuit below, the voltage of the source, Vs, is 1 millivolt. Compute the overall voltage gain, Vload/Vs.**

[10] (a)



(5) [b] From your Answer in Part (a) compute the voltage at the LOAD, V_L ?

4. (a) If voltage gain ,Vout/Vin, is 2000 volts/volt, What is the gain in decibels?

(b) if current gain ,Iout/Iin, is 1200 amps/amp, what is the gain expressed in decibels?

(c) Compute the power gain from parts (a) and (b) above.

5. Design a "weighted summer" operational amplifier (assume idea op amp) that will sum the following equation for me:

$V(t) = 5\,V1 - 10\,V2 + 8\,V3$ where V1,V2, and V3 are the unknown voltages (variables).

Watch your "signs" , <u>you may</u> have to use "inverting" op amps to accomplish the task. Before you freak out, this is almost exactly done for you in the textbook, page 72, also mostly done in a class lecture.

6. You are a brand new engineering employee at my multi-million dollar technical company (but unfortunately, a non-profit) and I have a job for you. Show me what you got:

Your task is to design an integrating op amp that will integrate the following time function: $f(t) = 3t$

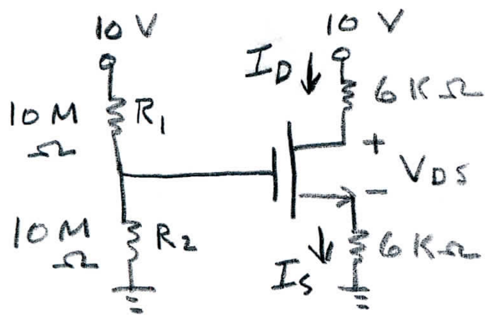
Again, watch your "signs"; you may have to use an inverter op amp.

7. **Given the circuit below. Find the voltage Vds and Drain current Id.**

Given: Vt= 1 volt, threshold voltage

Kn prime (W/L) = 1 milliamp/Vsquared

Assume lambda=0 which we have done in our problems anyway.



8. Given an nMOSFET with Cox= 4.32 femtoFarads/micron squared and kn prime = 194 microamps/Volt squared

W= 8 um

L= 0.4um

Threshold voltage Vt = 0.7 Volts

The drain current, Id= 100 microamps

<u>I want to operate this MOSFET in the SATURATION REGION!</u>

(a) Find Vgs

(b) Find Vov

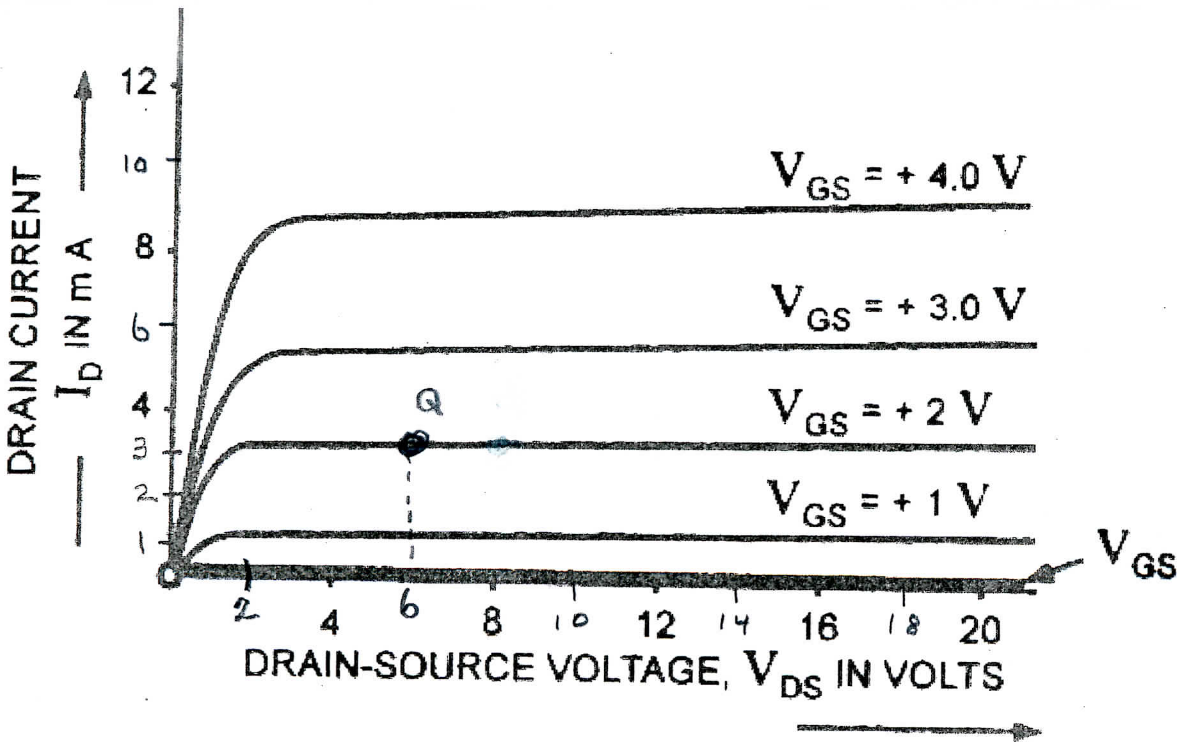
9. Given the following operating characteristics for the nMOSFET below AND the desired operating Q point.

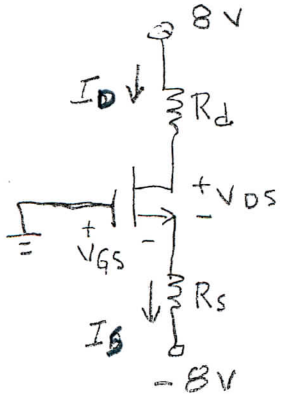
(a) Sketch the "design space" on the operating characteristics below:

Id,max= 12 milliamps, Vds,max= 18 Volts, Pd max=24 milliwatts

(b) Derive the equation for the Load Line. AND PLOT it ON the Chart

(c) Find values for Rs and Rd for operation at the Q point..

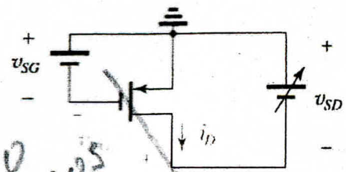


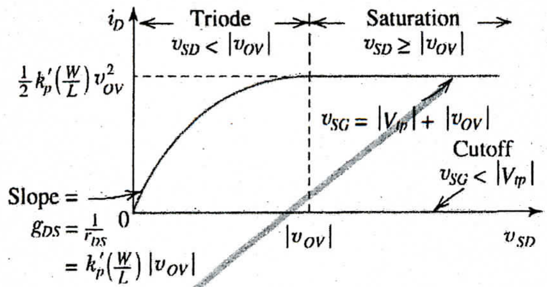


REFERENCE MATERIAL

NO PMOS on EXAM!!

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor





- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

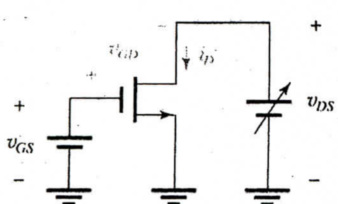
Then

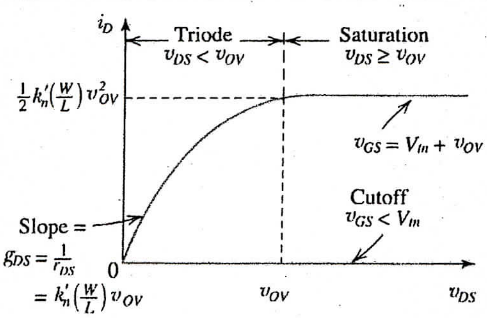
$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 6.2 Summary of the BJT Current–Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right)e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right)e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1-\alpha)i_E = \frac{i_E}{\beta+1}$$

$$i_C = \beta i_B \qquad i_E = (\beta+1)i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

V_T = thermal voltage = $\frac{kT}{q} \simeq 25$ mV at room temperature