The University of Alabama in Huntsville
Electrical & Computer Engineering
CPE 426/526
February 26, 2021
Sequential Modeling and Synthesis

Due March 5, 2021

Design an FSM circuit for control of lights used to start a race, which works as follows.

Inputs: Reset
Start
Clock

Outputs: Red
Yellow
Green

- Only one light can be on at any time.
- The Reset signal forces the circuit into a state in which the red light is turned on.
- When the Start signal is activated, the red light stays on for at least one second, then the yellow light is turned on.
- The yellow light stays turned on one second and then the green light is turned on.
- The green light stays on for at least three seconds and then the red light is turned on and the circuit returns to its reset state.
- The input clock runs at 10 MHz.

(a) Write a behavioral VHDL model of a clock divider that takes the 10 MHz clock and derives from it a 1 Hz clock.
(b) Write a behavioral VHDL model of the FSM.
(c) Write a testbench that reads input values from a text file (provided by me) to exercise the model. This testbench needs to incorporate your clock divider circuit and your finite state machine. It will respond to the slow clock and the text file will have inputs applied at every second.
(d) Simulate to verify the correctness of your model.
(e) Synthesize your design and write out .vho and .sdo files.
(f) Simulate the output from synthesis to verify the synthesized version.

Turn in your VHDL source files (both .vhd and .vho) and your SDF files.