LABORATORY # 09 and 10

Operating Characteristics of JFETs

Purpose

The concept of the junction field effect transistor (JFET) is introduced. Understanding the configuration and states of JFETs will aid in the understanding of MOSFETs which will be introduced in later labs. Both NPN and PNP constructions are considered. Constants and variables relating to JFETs are discussed and utilized to convey a full understanding of the material. JFETs have high input impedance and low output noise. These features make JFETs ideal for small signal amplification. Unlike BJTs current can flow from drain to source or vice versa equally.

Theoretical Background

Construction - A JFET is constructed with four parts: a gate region, a body region, a drain region and a source region. The body is referred to as the channel if voltage in the gate is field affected. This puts the JFET into active mode allowing current to flow through the body. For an N-channel JFET the body is a P-type material, while the drain and source are both N-type. For a P-channel JFET the body is N-type, the drain and source are both P-type. For ideal operation the material used to make the gate has no effect. Since the gate has no junctions, it can be modeled as a capacitor.

Operation - Current flows through the body/channel region if the transistor is in linear operating mode. To get the JFET into linear operating mode you must appropriately bias the gate. The gate bias creates a channel through the body allowing current to flow. The voltage needed on the gate to put a JFET into linear operating mode is known as the threshold voltage. This gate voltage can be kept close to the threshold voltage relative to the source-drain voltage in order to make the JFET act as a current controlled device. Thus, the current can be maintained regardless of the drain to source voltage.

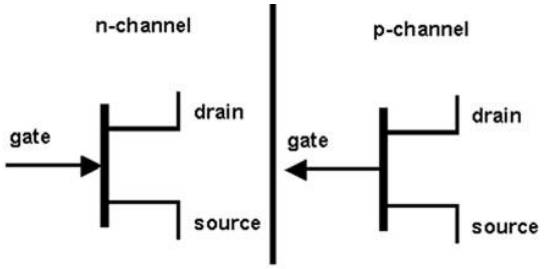

Figure 9.1 Symbolic representation

Terms

The terminals of JFETs use “D” to represent the drain, “S” to represent the source, “G” to represent the gate, and “B” to represent the body. The three operating states are known as Ohmic (linear), Saturation, and pinch-off. The threshold voltage (V_{TH}) is used to represent the minimum value of the voltage required between the gate and source (V_{GS}) in order to allow current to pass through the body. The pinch off voltage (V_P) is the voltage beyond which the source current is constant (JFET is in saturation). V_P is defined when the gate to source voltage is zero.

Output characteristic V-I curves of a typical JFET:

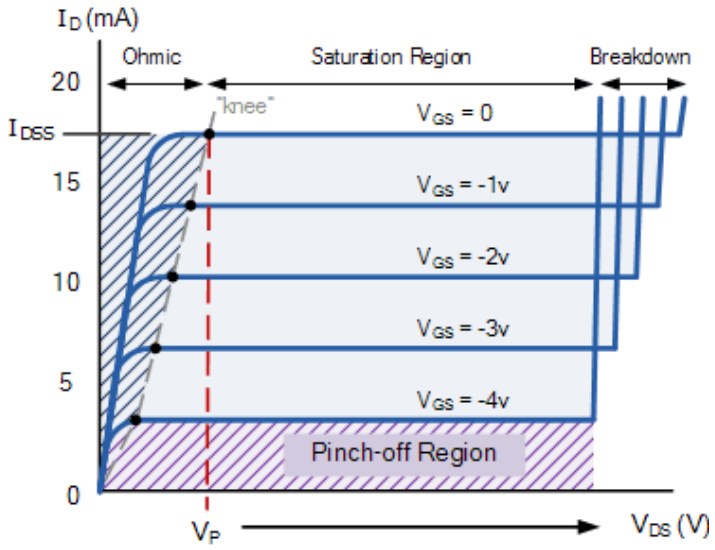

Figure 9.2 Drain Characteristics

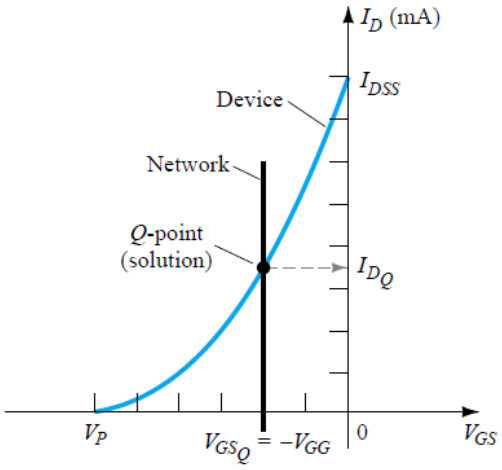

Figure 9.3 Transfer Characteristics

Circuit

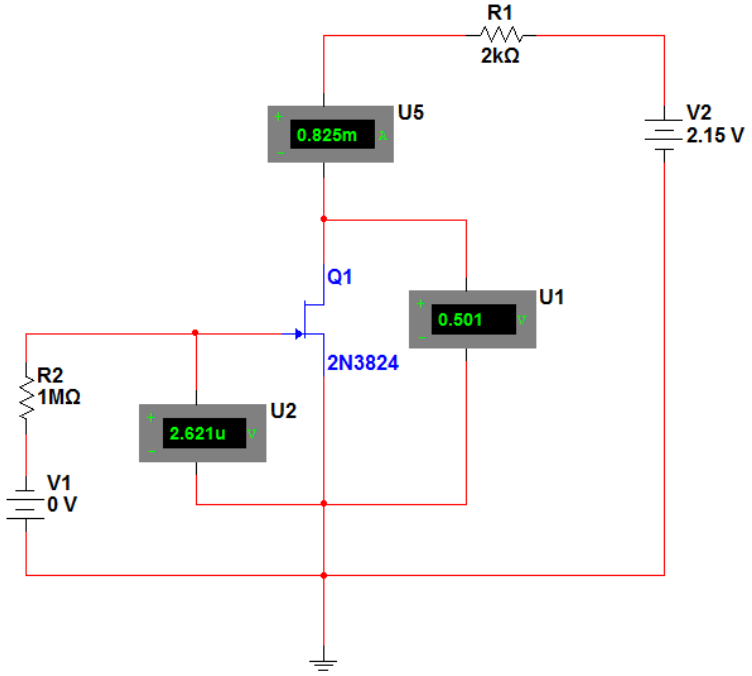

Figure 9.4 JFET (2N3824) circuit

Tables:

Table 9.1

Drain Characteristic (NPN 2N3824)			
	V_{GS} = 0 V	**V_{GS} = -0.5 V**	**V_{GS} = -1 V**
V_{DS} (V)	**I_d (mA)**	**I_d (mA)**	**I_d (mA)**
0			
0.5			
1			
2			
4			
8			
12			
16			
20			

Table 9.2

	V_{DS} = 6V
V_{GS} (V)	I_d (mA)
0	
-0.5	
-1	
-1.5	
-2	

Procedure

1) Construct the circuit provided in Fig 9.4 and use the n-channel JFET 2N3824 in Multisim and 2N3819 in lab.

2) Obtain data to produce drain characteristic curves:
   a) Measure I_d for the values of V_{DS} indicated in Table 9.1 (note: you need to adjust V_2 in order to set V_{DS} to the values in the table. Thus, V_2 does not equal V_{DS}). While you do this adjust the value of V_1 as needed to keep V_{GS} = 0V.
   b) Repeat with V_{GS} = -0.5V and -1.0V
   c) Plot the data you recorded in Table 9.1. Your results should look like Fig 9.2. Based on your plot, estimate V_P and V_{TH}. Mark V_P on your plot.

3) Obtain data to produce a transfer characteristic plot
   a) Set V_2 so that V_{DS} = 6V
   b) Adjust the value of V_1 to obtain the values of V_{GS} in Table 9.2. For each V_{GS} measure I_d. Your final value for I_d should be 0 mA. If you do not get I_d = 0 mA (or very close to it) then continue decreasing V_{GS} below -2V until I_d reaches 0 mA.
   c) Plot your results and estimate V_P. Mark V_P on your plot. Compare your estimation of V_P in your drain and transfer characteristic analyses.

Reference:

Electronic Devices and Circuit Theory, 7th Ed. by Robert Boylestad and Louis Nashelsky.

Small Signal Amplification with JFETs (Lab 10)

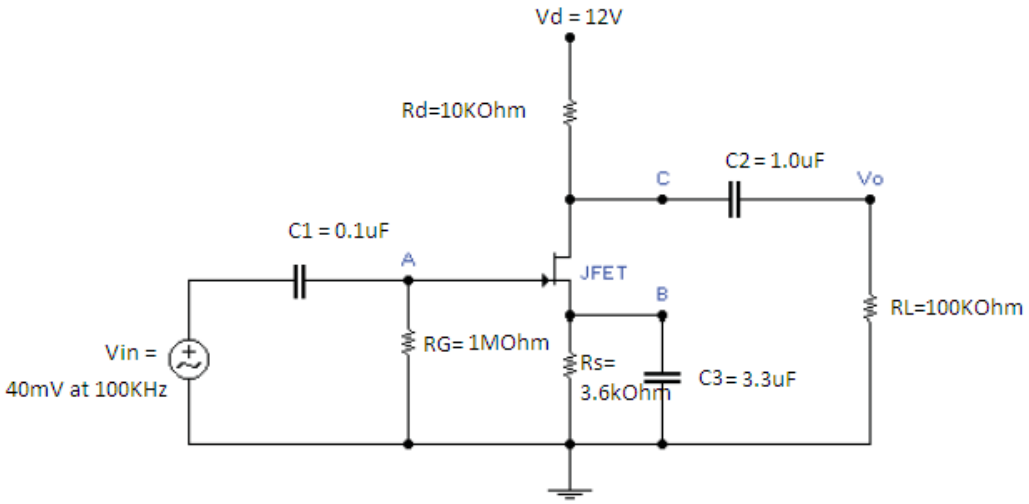

Figure 10.1

Procedure:

1 Build the circuit as shown in Fig. 10.1 in Multisim. Apply a small sinusoidal signal (Vpp=40mV) at the given frequency range (See table 10.1) using JFET 2N3824 (2N3819 in lab).

2 Based on your Table 10.1 results, plot voltage gain as a function of frequency and calculate the bandwidth. Identify the high and low cutoff frequencies. Note: plot frequency on a log scale.

   a. In the lab the frequency generator has a maximum output frequency of 3 MHz and a minimum output voltage greater than 40 mV peak-to-peak. However, the 2N3819 that you will use in the lab has a much smaller bandwidth than the 2N3824 that you will simulate.

   b. For the lab apply the minimum amplitude allowed by your frequency generator. Create your own table similar to Table 10.1 but with a maximum frequency of 3 MHz. Make sure you collect enough data points to plot the frequency response of the circuit in Fig. 10.1.

3 Comment on the phase relationship between the input and output waveforms

4 Compare and discuss your experimental and simulation results.

Table 10.1

Frequency (Hz)	Vout (mV)	Gain
30		
45		
60		
100		
200		
500		
1000		
10000 (10 kHz)		
100000 (100 kHz)		
500000		
1000000 (1MHz)		
1500000		
2000000		
3000000		
4000000		
5000000		
7000000		
10000000 (10MHz)		
11000000		
12000000		
15000000		
16000000		