Electric Circuits & Electronics Design Lab EE 316-08

Lab 4: Digital to Analog Convertors

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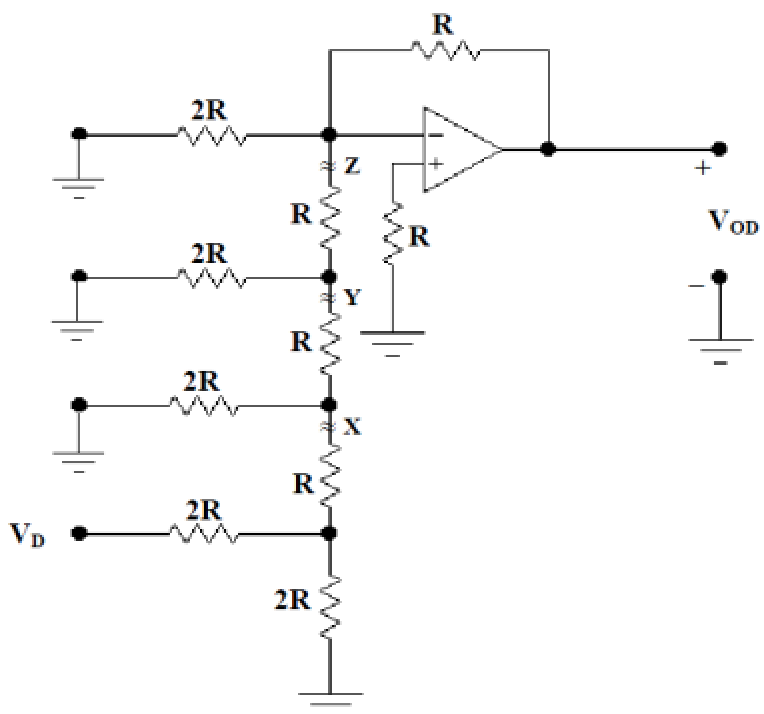
Introduction

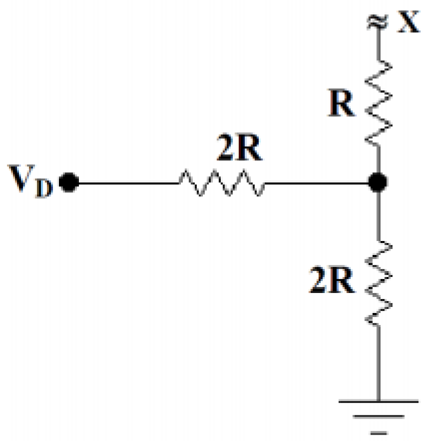
In this lab, we discuss how to create a digital to analog convertor with an op-amp. In the theoretical analysis section, we will discuss how the digital to analog converter works. In the simulation section we will look at the simulation results. In the results and discussion section I will discuss the results.

Theory

The digital to analog convertor takes a digital signal and converts it to the analog equivalent. We do this by using a resistive binary ladder. The structure for this is shown below.



The ladder is connected to the negative terminal of the op-amp. Resistor R is grounded on one end and connected to the positive terminal on another end. At each of the breakpoints the circuit can be reduced to the circuit below.



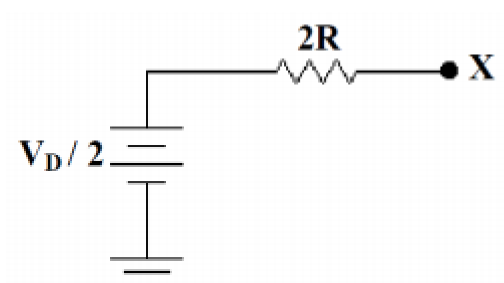
The Thevenin voltage is derived below.

$$RTH = 2R||2R + R = 2R$$

$$V_{TH} = \frac{V_D}{2R+2R}2R$$

$$= \frac{V_D}{2}$$

The Thevenin schematic is shown below.



This was performed at breakpoint x, but it can be done at the other breakpoints as well. Vd will just be divided by 4, and then 8, and then 16, respectively. Vout can be written as follows.

$$V_O = V_{OA} + V_{OB} + V_{OC} + V_{OD}$$

$$V_O = -(\frac{V_A}{2} + \frac{V_B}{4} + \frac{V_C}{8} + \frac{V_D}{16})$$

Va contributes the most output voltage, so it represents the most significant bit. Vd represents the least significant bit. The table below shows the results of the hand calculations. The hand calculations are shown in the appendix.

	V_A	V_B	V_C	V_D	V_O (V)
0	0	0	0	0	0.00
1	0	0	0	1	-0.3125
2	0	0	1	0	-0.625
3	0	0	1	1	-0.9375
4	0	1	0	0	-1.25
5	0	1	0	1	-1.5625
6	0	1	1	0	-1.875
7	0	1	1	1	-2.1875
8	1	0	0	0	-2.5
9	1	0	0	1	-2.8125
10	1	0	1	0	-3.125
11	1	0	1	1	-3.4375
12	1	1	0	0	-3.75
13	1	1	0	1	-4.0625
14	1	1	1	0	-4.375

15	1	1	1	1	-4.6875

The number of steps in a system is given by is given by 2^n-1. The step size is shown below.

$$Step\_Size = \frac{V_{IN}}{2^N}$$

The maximum output voltage is given by the below equation.

$$Max\_Output = Num\_Steps \times Step\_Size$$

The resolution is:

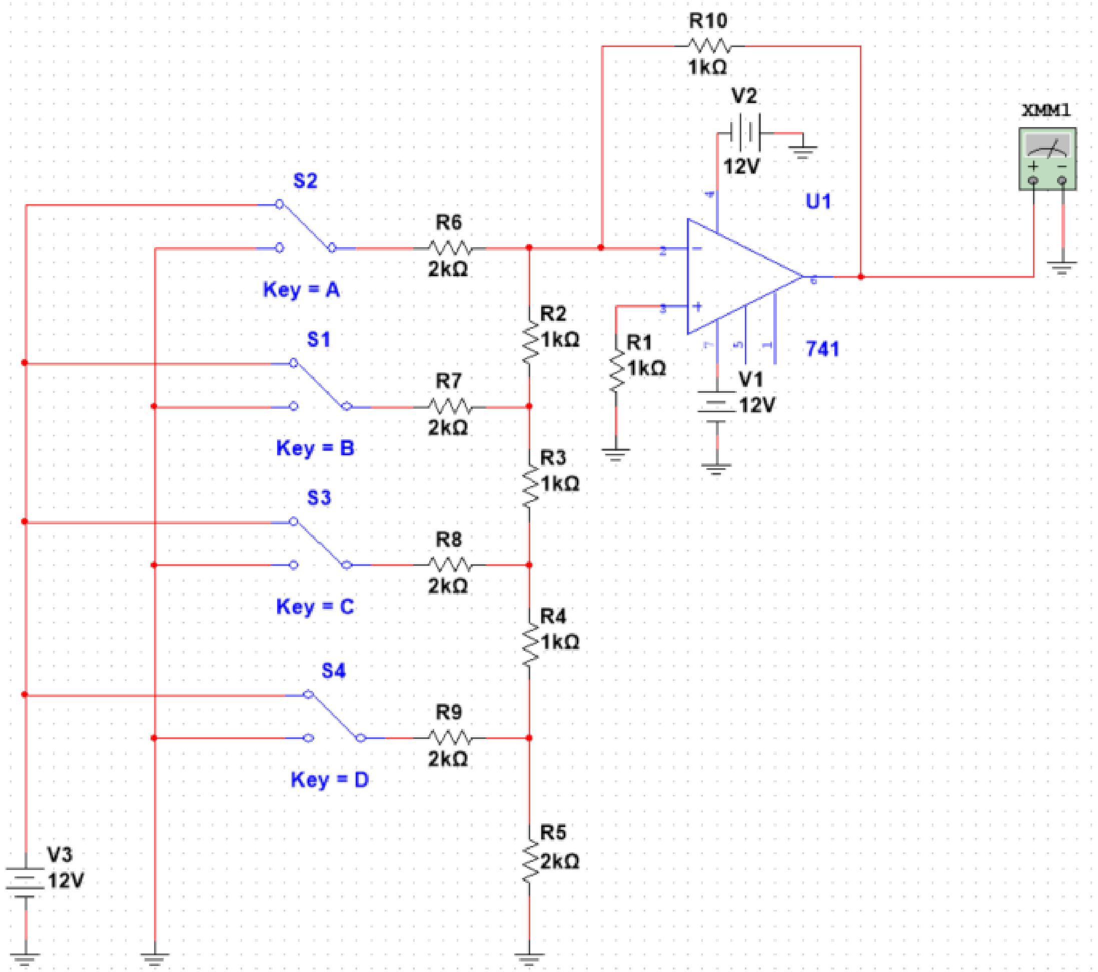
$$\mathrm{Res} = \frac{Step\_Size}{2}$$

The precent error is:

$$Percent\_Error = \frac{V_{O\_Expected} - V_{O\_Measured}}{V_{O\_Expected}} \times 100\%$$

Simulations

For this part of the lab, we used Multisim to implement a DAC.



The simulation results are shown below.

Input State					Simulation
	V_A	V_B	V_C	V_D	V_O (V)
0	0	0	0	0	0.002
1	0	0	0	1	-0.310

2	0	0	1	0	-0.623
3	0	0	1	1	-0.935
4	0	1	0	0	-1.248
5	0	1	0	1	-1.56
6	0	1	1	0	-1.975
7	0	1	1	1	-2.185
8	1	0	0	0	-2.498
9	1	0	0	1	-2.81
10	1	0	1	0	-3.123
11	1	0	1	1	-3.435
12	1	1	0	0	-3.748
13	1	1	0	1	-4.06
14	1	1	1	0	-4.373
15	1	1	1	1	-4.685

Results and Discussion

The results of the simulation were remarkably similar to the hand calculations. If this experiment were performed again in the real world, then some more variance could be expected. This would be due to tolerances in the parts used as well as the instruments that are used to take measurements.

Conclusion

The purpose of this lab was to introduce us to the digital to analog convertors. We used a resistor ladder that was connected to an op-amp. We performed theoretical hand calculations. We then verified these calculations with a simulator. The theoretical values closely matched the simulated values, thus they are verified.

Appendix

in	equation	out (V)
0000	$0+0+0+0$	0
0001	$-(0+0+0+5/16)$	-.3125
0010	$-(0+0+5/8+0)$	-.625
0011	$-(0+0+5/8+5/16)$	-.9375
0100	$-(0+5/4+0+0)$	-1.25
0101	$-(0+5/4+0+5/16)$	-1.5625
0110	$-(0+5/4+5/8)$	-1.875
0111	$-(5/4+5/8+5/16)$	-2.1875
1000	$-5/2$	-2.5
1001	$-(5/2+5/16)$	-2.8125
1010	$-(5/2+5/8)$	-3.125
1011	$-(5/2+5/8+5/16)$	-3.4375
1100	$-(5/2+5/4)$	-3.75
1101	$-(5/2+5/4+5/16)$	-4.0625
1110	$-(5/2+5/4+5/8)$	-4.375
1111	$-(5/2+5/4+5/8+5/16)$	-4.6875