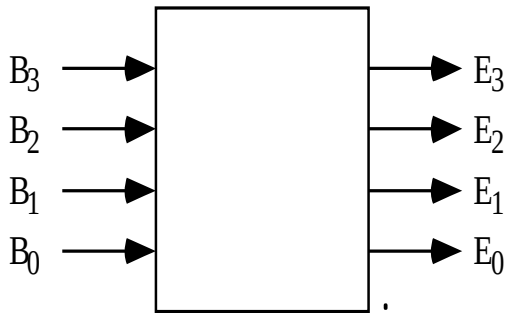
The University of Alabama in Huntsville
Electrical & Computer Engineering
CPE 426/526
January 16 2020
Simulating Multiple Architectures

Due February 2, 2021

Consider a code converter circuit that converts BCD 84-2-1 to BCD 8421.



$B_3B_2B_1B_0$	$E_3E_2E_1E_0$
0 0 0 0	0 0 0 0
0 0 0 1	1 1 1 1
0 0 1 0	1 1 1 1
0 0 1 1	1 1 1 1
0 1 0 0	0 1 0 0
0 1 0 1	0 0 1 1
0 1 1 0	0 0 1 0
0 1 1 1	0 0 0 1
1 0 0 0	1 0 0 0
1 0 0 1	0 1 1 1
1 0 1 0	0 1 1 0
1 0 1 1	0 1 0 1
1 1 0 0	1 1 1 1
1 1 0 1	1 1 1 1
1 1 1 0	1 1 1 1
1 1 1 1	1 0 0 1

$B_3B_2B_1B_0$ represents the 4-bit BCD 84-2-1 input and $E_3E_2E_1E_0$ represents the 4-bit BCD 8421 output. For invalid BCD 84-2-1 inputs, all 1s are output as an error indication. You will find a zip file in Canvas that contains the following:

a. A VHDL entity declaration for the converter.
b. An algorithmic behavioral architectural body for the converter.
c. A data flow behavioral architectural body for the converter.
d. A structural architectural body for the converter.
e. A test bench entity that ties the entity to a pulse generator that generates all possible combinations of the inputs.
f. Three configuration files
   i. Test bench for the behavioral architecture
   ii. Test bench for the dataflow architecture
   iii. Test bench for the structural architecture

These files are also available at ece.uah.edu/~gaede/cpe526/homework_files/hw1
Perform the following steps

a. Create a project in modelsim which has all these files
b. Compile all of the files
c. Simulate all three configurations to verify correctness.
d. Save your wave and list files.

Turn in your wave and list files making a zip file and then uploading it to the drop box in Canvas.