CPE434/534 2021

Exam 1

Undergraduates: answer 1-5

Graduates: answer questions 1-6.

Name (printed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_name (signed) \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1 **.Fragmentation and Page Sizes**: (15 points)

Many modern Intel processors support multiple page sizes such as 4KB and 2MB pages.

1. What is the difference between external fragmentation and internal fragmentation?
2. What is the impact of page size on fragmentation?

The page table approach to memory management emerged at a time when machine’s address space vastly exceeded the size of physical memory. While the address space has gotten larger and larger physical memory has also gotten larger to the extent that overhead from paging small pages has gotten excessive. One solution to this problem has been to have different size pages. For example, the modern Intel processor can have 4 KB and 2MB pages. With large pages the number of TLB misses and page faults go down

1. One approach to choosing page sizes might be to let the user decide. Windows does in fact have a system call (VirtualAlloc) that lets you choose different page sizes for a specific allocation. Another approach would be to have the operating system make measurements and change the page size accordingly (remember, the user logical address space would not change). Propose an algorithm similar to the working set algorithm for dynamically choosing the page size. Describe in as much detail as possible. About 1 page.

2.  **Page Tables (15 points)**

An engineer has been hired to design a multilevel page table system for a machine with 32 bit addresses. Vaguely recalling from class a three level page table design, they choose a three level page table with field widths for each portion of the virtual address is 5, 6, and 7 bits respectively

For the following questions SHOW ALL WORK

1. for the smallest program possible, consisting of one page of text and heap starting at address 0 and one page of stack starting at the highest address (0xff...f) what is the size of the page table structure in bytes.
2. is this a good architecture. (yes or no) Explain your answer.
3. for the largest program possible, consisting of all pages starting at address 0 and 5+6+7 bits) running to the highest address possible (0xff...f) what is the size of the index structure in bytes.

3. **Scheduling** (15 points)

1. Given the following processes and execution times

Process Time

P1 13

P2 5

P3 23

P4 3

P5 31

P6 3

P7 14

Calculate the completion time for each task for round robin, first come first served and shortest job first scheduling algorithms? Assume that a quantum of 5 is being used when a quantum of time is necessary. SHOW ALL WORK

4- TLB (15 points)

1. Assuming a three level page table, a tlb hit time of 10 ns, a main memory access time of 50 ns, a hit rate of 95%, what is the average memory access time? SHOW ALL WORK
2. What cache hit rate do you need for an average access time of 90ns

1. What cache hit rate do you need for an average access time of 150n

5. **Synchronization (15 points)**

1. What is a critical section and what is it used for?
2. Explain what counting semapores, mutex semaphores, and synchronization semaphores are and give an example of their use.
3. Do you need synchronization capabilities like semaphores if you only have a single core processor? Explain your answer

6. **GRADUATE STUDENTS ONLY**

As discussed in question 1, many computers now allow you to change the page size for your operating system. Based on your reading of the literature (not your text) can a host and guest operating system have different page sizes. Explain your answer and include your references.