## EXTENDED EVALUATION REPORT

This report presents an extension of the experiments conducted in Sec. VI, based on the system settings described in Sec. VI-A. The extension includes four main aspects: (i) an increased number of tasks in TacleBench (from 12 to 36); (ii) comparison of the total WCET with inter-core cache interference; (iii) a detailed comparison of each evaluated task; and (iv) additional experiments using Papabench.

**Extended Evaluation.** First, Tab. IX presents an extended version of the inter-core cache interference estimations comparison for tasks in TacleBench. The number of tasks being examined is extended from 12 tasks to 36 tasks, where each task is analysed under 12 interfering tasks. Compared to the state-of-the-art (*i.e.*, the analysis labelled with "Zhang2022" [4]), the proposed analysis reduces the inter-core cache interference estimations by 52.31% on average for all 36 tasks. In the table, the tasks are organised into three groups based on their L2 cache behaviours:

- Tasks that can incur evictions on the L2 cache due to the interfering task. For such tasks (26 out of 36 tasks), the proposed analysis outperforms Zhang2022 [4] by reducing the inter-core cache interference estimations by 72.43% on average.
- Tasks that always hit the L1 cache except the first miss, *i.e.*, all data required by the task can be fitted in the L1 cache. For such tasks (3 out of the 36 tasks), they would not incur additional delay on the L2 cache due to the interfering task. In this case, both competing methods return an inter-task interference of zero.
- Tasks that always miss the L2 cache, based on the intra-core cache analysis without considering any inter-core interference. Hence, for these tasks (7 out of 36 tasks), both methods yield the same inter-core cache interference of zero.

**Comparison of WCET Estimations.** Second, Tab. X shows the comparison of the total WCET of 36 tasks under Zhang2022 [4] and the proposed analysis. The tasks are organised by the same approach as described above. From the results, we observed that for certain tasks (*e.g.*, `huff_dec`), the inter-core cache interference is indeed negligible to the total WCET, *i.e.*, the reduction in the inter-core cache interference estimations barely affect the total WCET estimations. However, the results also show there are 17 tasks in which the inter-core cache interference is non-trivial to the WCET, where our analysis can lead to reduced WCET estimations. Compared to [4], our analysis reduces the total WCET estimations by 12.38% on average for tasks in the first group and 8.94% on average for all evaluated tasks, respectively. This observation illustrates the reviewer's point on the inter-core cache interference of some tasks, but it also justifies the effectiveness of the proposed analysis in a general case.

**Detailed Comparison of Each Evaluated Task.** Third, Fig. 8 to 43 present the absolute value of the inter-core cache interference and the total WCET estimations of the 36 tasks under different interfering tasks. The results highlight the portion of the inter-core cache interference in the total WCET of each task, which validates the results presented above and the effectiveness of the proposed analysis.

TABLE VIII: FLY-BY-WIRE and AUTOPILOT Tasks with Frequencies

| Tasks in AUTOPILOT | Tasks in FLY-BY-WIRE |
|---|---|
| altitude_control_task | check_failsafe_task |
| climb_control_task | check_mega128_values_task |
| link_fbw_send | **send_data_to_autopilot_task** |
| stabilisation_task | servo_transmit |
| **radio_control_task** | test_ppm_task |

**Evaluation of Papabench.** Finally, the tasks in Papabench are analysed using the proposed analysis and Zhang2022. The Papabench produces two executable files (Fly-By-Wire and Autopilot), representing two applications running on two processors. Each application invokes a set of different tasks, as shown in Tab. VIII. However, we observe that most tasks (8 out of 10) in Papabench can always hit the L1 cache (except the first miss). For these tasks, both competing methods return an inter-core cache interference of zero with an identical WCET, and hence, their results are omitted.

The task `radio_control_task` (in AUTOPILOT) and task `send_data_to_autopilot_task` (in FLY-BY-WIRE) would incur L2 cache evictions due to interfering tasks. Fig. 44 presents the inter-core cache interference and the total WCET for `radio_control_task` when being executed under the interference from each of the five tasks in FLY-BY-WIRE. Fig. 45 shows the results of `send_data_to_autopilot_task` under the interference of each task in Autopilot. As observed, for task `radio_control_task`, the proposed analysis outperforms Zhang2022 by reducing the inter-core cache interference and total WCET estimations by 87.1% and 7.56%, respectively. For task `send_data_to_autopilot_task`, the proposed analysis outperforms Zhang2022 by reducing the inter-core cache interference and total WCET estimations by 62.42% and 2.78%, respectively.

TABLE IX: Ratio of the inter-core cache interference of proposed analysis to Zhang2022 *(binaryS: binarysearch; insertS: insertsort)*.

| Classification | Benchmark | adpcm_dec | binaryS | cover | fir2dim | fmref | huff_dec | iir | insertS | jfdctint | ndes | st | statemate | **Avg.** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tasks that incur evictions on the L2 cache due to the interfering task | adpcm_dec | 0.48 | 0.31 | 0.28 | 0.07 | 0.06 | 0.10 | 0.19 | 0.21 | 0.38 | 0.11 | 0.04 | 0.70 | 0.24 |
| | binarysearch | 1.0 | 0.01 | 0.33 | 0.03 | 0.07 | 0.07 | 1.0 | 1.0 | 0.17 | 0.06 | 0.05 | 0.25 | 0.34 |
| | fir2dim | 0.24 | 0.06 | 0.53 | 0.05 | 0.07 | 0.09 | 0.04 | 0.06 | 0.10 | 0.12 | 0.02 | 0.70 | 0.17 |
| | fmref | 0.15 | 0.01 | 0.23 | 0.02 | 0.10 | 0.10 | 0.01 | 0.01 | 0.02 | 0.02 | 0.02 | 0.20 | 0.07 |
| | huff_dec | 0.12 | 1.0 | 1.0 | 0.01 | 0.09 | 0.11 | 0.01 | 0.01 | 0.01 | 0.08 | 0.01 | 0.25 | 0.22 |
| | iir | 1.0 | 1.0 | 0.20 | 0.14 | 0.08 | 0.14 | 0.08 | 0.06 | 0.24 | 0.11 | 0.03 | 0.33 | 0.29 |
| | insertsort | 0.23 | 0.01 | 0.25 | 0.14 | 0.01 | 0.07 | 0.01 | 0.33 | 0.06 | 0.14 | 0.05 | 0.40 | 0.14 |
| | jfdctint | 0.81 | 0.19 | 0.39 | 0.11 | 0.11 | 0.16 | 0.22 | 0.25 | 0.13 | 0.16 | 0.06 | 0.64 | 0.27 |
| | ndes | 0.30 | 0.21 | 0.43 | 0.11 | 0.10 | 0.23 | 0.01 | 0.01 | 0.22 | 0.15 | 0.03 | 0.60 | 0.20 |
| | st | 0.92 | 0.04 | 0.51 | 0.15 | 0.20 | 0.34 | 0.01 | 0.34 | 0.27 | 0.27 | 0.01 | 0.82 | 0.32 |
| | statemate | 0.12 | 0.03 | 0.18 | 0.03 | 0.07 | 0.07 | 0.01 | 0.01 | 0.05 | 0.09 | 0.05 | 0.70 | 0.12 |
| | audiobeam | 0.61 | 0.13 | 0.40 | 0.18 | 0.07 | 0.14 | 1.0 | 1.0 | 0.50 | 0.11 | 0.08 | 1.0 | 0.43 |
| | cjpeg_transupp | 0.46 | 0.12 | 0.75 | 0.42 | 0.16 | 0.47 | 0.18 | 0.02 | 0.42 | 0.48 | 0.23 | 1.0 | 0.39 |
| | dijkstra | 1.0 | 1.0 | 0.03 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 0.92 |
| | g723_enc | 0.20 | 0.01 | 0.18 | 0.05 | 0.05 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 0.62 |
| | gsm_dec | 0.62 | 0.01 | 0.25 | 0.01 | 0.08 | 0.07 | 0.02 | 0.01 | 0.02 | 0.09 | 0.01 | 1.0 | 0.18 |
| | gsm_enc | 0.57 | 0.10 | 0.24 | 0.09 | 0.05 | 0.10 | 0.01 | 0.01 | 0.17 | 0.12 | 0.08 | 0.50 | 0.17 |
| | h264_dec | 0.12 | 0.01 | 0.08 | 0.01 | 0.03 | 0.06 | 0.01 | 0.01 | 0.04 | 0.04 | 0.01 | 0.39 | 0.07 |
| | lift | 0.01 | 0.01 | 0.07 | 0.01 | 0.08 | 0.08 | 0.01 | 0.02 | 0.05 | 0.04 | 0.01 | 0.25 | 0.05 |
| | md5 | 1.0 | 1.0 | 0.07 | 0.01 | 0.11 | 0.12 | 0.01 | 0.01 | 0.01 | 0.01 | 0.04 | 0.09 | 0.20 |
| | minver | 0.52 | 0.16 | 0.23 | 0.06 | 0.02 | 0.05 | 0.15 | 0.10 | 0.15 | 0.16 | 0.05 | 0.41 | 0.17 |
| | petrinet | 1.0 | 0.01 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 0.92 |
| | pm | 0.05 | 0.01 | 0.02 | 0.01 | 0.11 | 0.05 | 0.01 | 0.01 | 0.01 | 0.02 | 0.01 | 0.11 | 0.03 |
| | powerwindow | 0.01 | 0.01 | 0.05 | 0.01 | 0.06 | 0.09 | 0.01 | 0.01 | 0.01 | 0.02 | 0.01 | 0.29 | 0.04 |
| | prime | 0.92 | 0.13 | 0.41 | 0.14 | 0.14 | 0.19 | 0.28 | 0.26 | 0.34 | 0.22 | 0.06 | 0.76 | 0.32 |
| | sha | 0.67 | 0.01 | 0.14 | 0.10 | 0.06 | 0.14 | 0.01 | 0.01 | 1.0 | 0.15 | 0.12 | 1.0 | 0.28 |
| Tasks that always hit the L1 cache except the first miss | bsort | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | cover | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | complex_updates | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| Tasks that cannot hit the L2 cache according to the intra-core cache analysis | cjpeg_wrbmp | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | countnegative | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | fft | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | filterbank | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | lms | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | ludcmp | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | matrix1 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |

TABLE X: Ratio of total WCET of proposed analysis to Zhang2022 *(binaryS: binarysearch; insertS: insertsort)*. $1.0^* \approx 1$ means the situation where the proposed analysis tightens the inter-core cache interference compared to [4], however, such interference is negligible to the total WCET.

| Classification | Benchmark | adpcm_dec | binaryS | cover | fir2dim | fmref | huff_dec | iir | insertS | jfdctint | ndes | st | statemate | **Avg.** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Tasks that incur evictions on the L2 cache due to the interfering task | adpcm_dec | 0.93 | 0.93 | 0.85 | 0.50 | 0.46 | 0.61 | 0.93 | 0.93 | 0.90 | 0.63 | 0.50 | 0.97 | 0.76 |
| | binarysearch | 1.0 | 0.98 | 0.96 | 0.60 | 0.76 | 0.76 | 1.0 | 1.0 | 0.96 | 0.75 | 0.71 | 0.94 | 0.87 |
| | fir2dim | 0.97 | 0.99 | 0.99 | 0.80 | 0.85 | 0.88 | 0.99 | 0.96 | 0.98 | 0.90 | 0.90 | 0.99 | 0.93 |
| | fmref | 0.99 | 0.96 | 0.97 | 0.92 | 0.76 | 0.79 | 0.96 | 0.91 | 0.89 | 0.39 | 0.56 | 0.95 | 0.84 |
| | huff_dec | 1.0* | 1.0 | 1.0 | 0.99 | 0.99 | 0.97 | 0.99 | 1.0* | 0.98 | 0.97 | 0.90 | 0.99 | 0.98 |
| | iir | 1.0 | 1.0 | 0.81 | 0.91 | 0.85 | 0.91 | 0.94 | 0.85 | 0.89 | 0.73 | 0.49 | 0.92 | 0.86 |
| | insertsort | 0.86 | 0.80 | 0.96 | 0.96 | 0.41 | 0.90 | 0.70 | 0.98 | 0.96 | 0.91 | 0.80 | 0.98 | 0.85 |
| | jfdctint | 0.97 | 0.74 | 0.75 | 0.45 | 0.48 | 0.46 | 0.86 | 0.87 | 0.72 | 0.49 | 0.32 | 0.90 | 0.67 |
| | ndes | 0.92 | 0.96 | 0.93 | 0.78 | 0.61 | 0.84 | 0.91 | 0.72 | 0.93 | 0.74 | 0.56 | 0.96 | 0.82 |
| | st | 1.0* | 0.99 | 0.99 | 0.96 | 0.96 | 0.98 | 0.99 | 0.99 | 0.98 | 0.97 | 0.93 | 1.0* | 0.98 |
| | statemate | 0.28 | 0.97 | 0.73 | 0.07 | 0.63 | 0.10 | 0.92 | 0.82 | 0.88 | 0.67 | 0.67 | 0.98 | 0.64 |
| | audiobeam | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0 | 1.0 | 1.0* | 1.0* | 1.0* | 1.0 | 0.83 |
| | cjpeg_transupp | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0 | 1.0* |
| | dijkstra | 1.0 | 1.0 | 1.0* | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0* |
| | g723_enc | 1.0* | 1.0* | 1.0* | 0.99 | 0.99 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0* |
| | gsm_dec | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0 | 1.0* |
| | gsm_enc | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* |
| | h264_dec | 0.74 | 0.52 | 0.93 | 0.11 | 0.81 | 0.21 | 0.96 | 0.96 | 0.96 | 0.29 | 0.80 | 0.98 | 0.69 |
| | lift | 0.88 | 0.95 | 0.82 | 0.63 | 0.92 | 0.86 | 0.91 | 0.96 | 0.98 | 0.68 | 0.44 | 0.94 | 0.83 |
| | md5 | 1.0 | 1.0 | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* |
| | minver | 0.97 | 0.94 | 0.78 | 0.65 | 0.33 | 0.40 | 0.97 | 0.93 | 0.85 | 0.70 | 0.50 | 0.90 | 0.74 |
| | petrinet | 1.0 | 1.0* | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0* |
| | pm | 1.0* | 1.0* | 1.0* | 0.99 | 1.0* | 0.99 | 1.0* | 1.0* | 1.0* | 0.99 | 0.99 | 1.0* | 1.0* |
| | powerwindow | 0.89 | 0.89 | 0.74 | 0.44 | 0.50 | 0.53 | 0.83 | 0.95 | 0.80 | 0.50 | 0.32 | 0.91 | 0.69 |
| | prime | 0.99 | 0.73 | 0.90 | 0.77 | 0.31 | 0.74 | 0.94 | 0.94 | 0.92 | 0.77 | 0.62 | 0.97 | 0.80 |
| | sha | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0* | 1.0 | 1.0* | 1.0* | 1.0 | 1.0* |
| Tasks that always hit the L1 cache except the first miss | bsort | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | cover | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | complex_updates | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| Tasks that cannot hit the L2 cache according to the intra-core cache analysis | cjpeg_wrbmp | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | countnegative | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | fft | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | filterbank | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | lms | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | ludcmp | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |
| | matrix1 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |

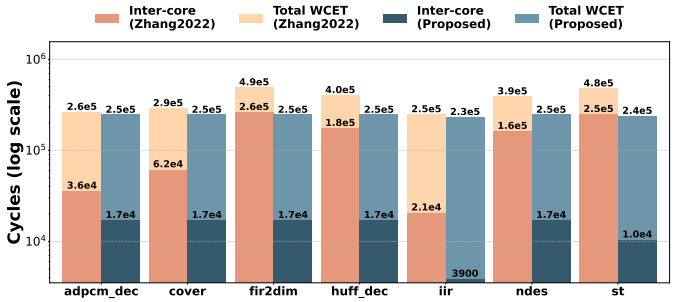


Fig. 8: Inter-core cache interference and total WCET of `adpcm_dec` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

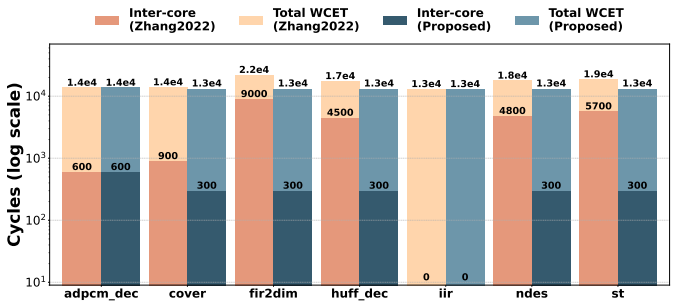


Fig. 9: Inter-core cache interference and total WCET of `binarysearch` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

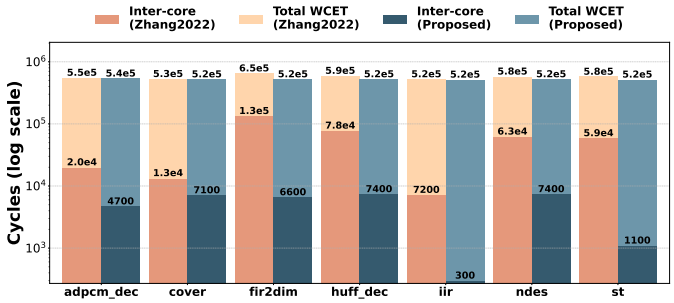


Fig. 10: Inter-core cache interference and total WCET of `fir2dim` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

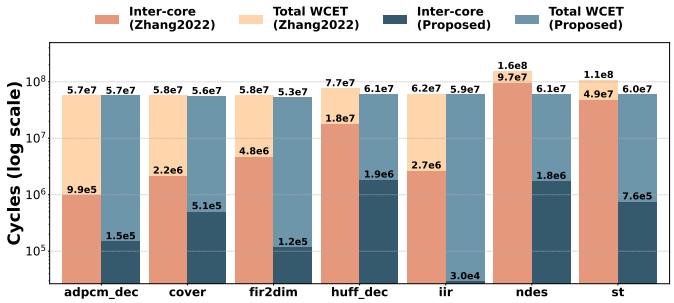


Fig. 11: Inter-core cache interference and total WCET of `fmref` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

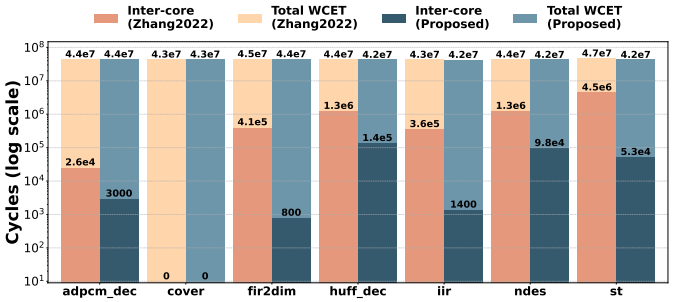


Fig. 12: Inter-core cache interference and total WCET of `huff_dec` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

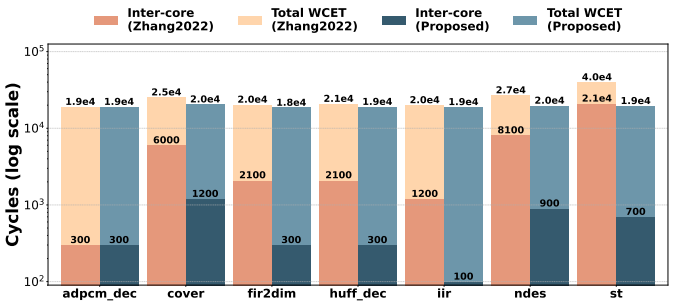


Fig. 13: Inter-core cache interference and total WCET of `iir` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

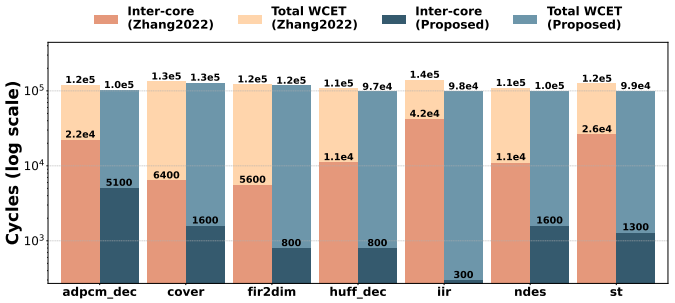


Fig. 14: Inter-core cache interference and total WCET of `insertsort` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

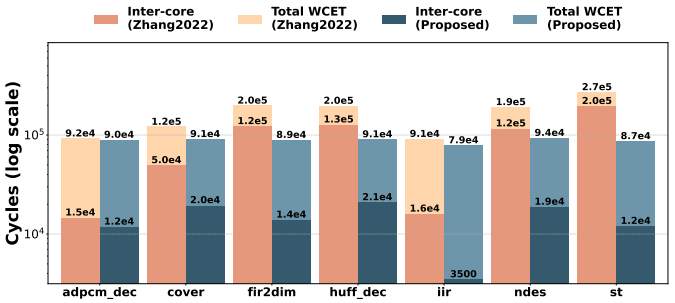


Fig. 15: Inter-core cache interference and total WCET of `jfdctint` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

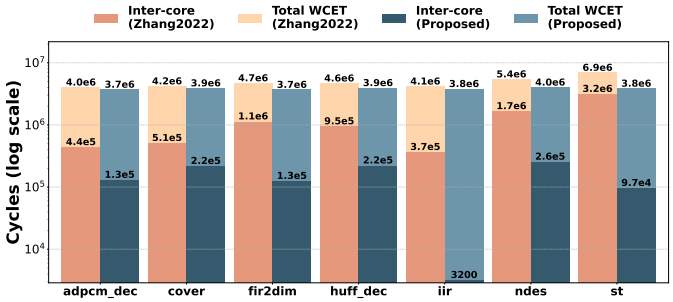


Fig. 16: Inter-core cache interference and total WCET of `ndes` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

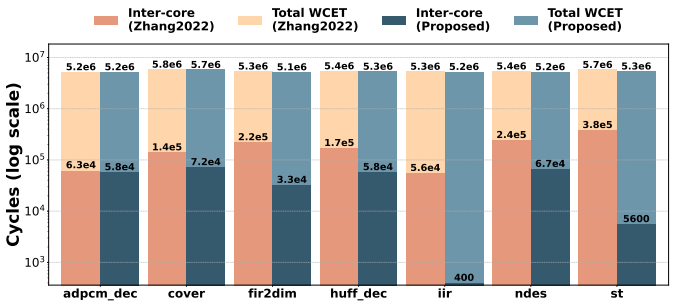


Fig. 17: Inter-core cache interference and total WCET of `st` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

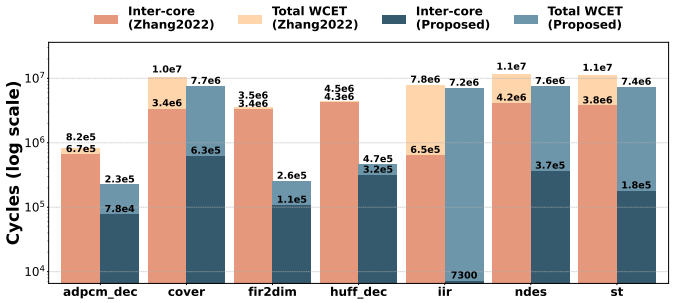


Fig. 18: Inter-core cache interference and total WCET of `statemate` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

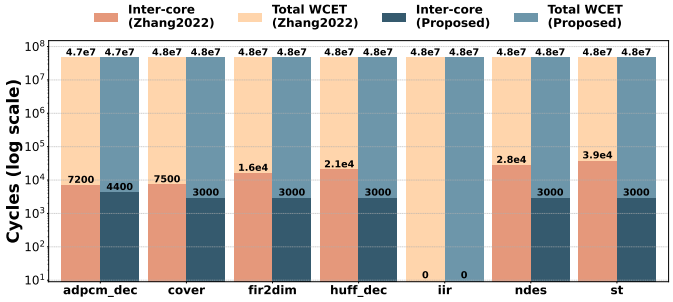


Fig. 19: Inter-core cache interference and total WCET of `audiobeam` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

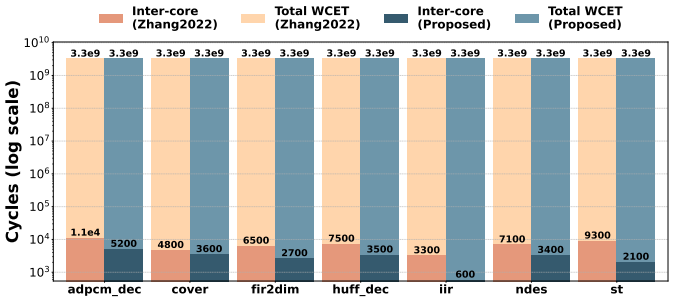


Fig. 20: Inter-core cache interference and total WCET of `cjpeg_transupp` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

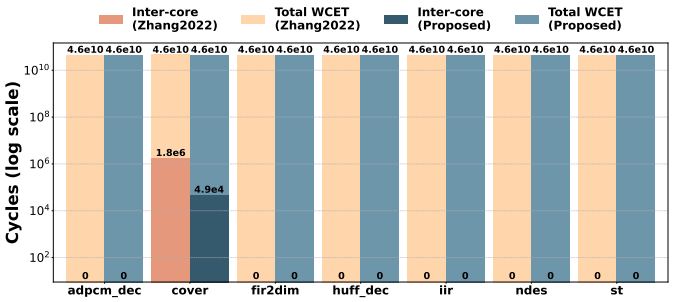


Fig. 21: Inter-core cache interference and total WCET of `dijkstra` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

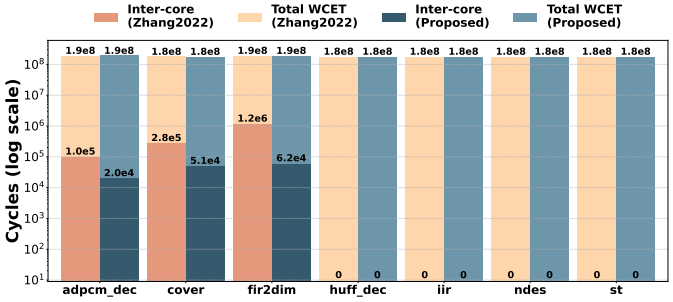


Fig. 22: Inter-core cache interference and total WCET of `g723_enc` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

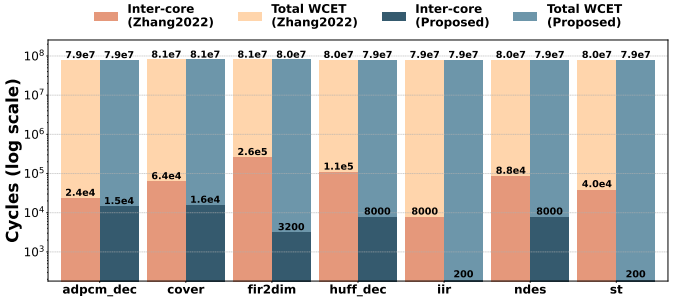


Fig. 23: Inter-core cache interference and total WCET of `gsm_dec` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

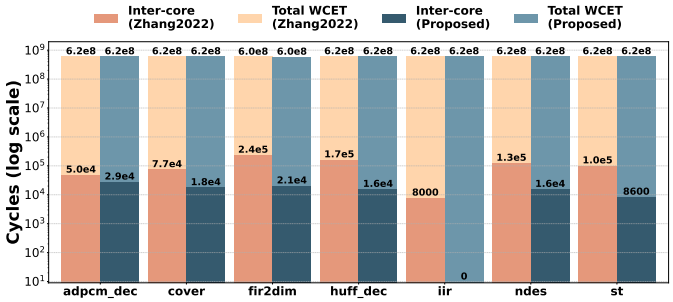


Fig. 24: Inter-core cache interference and total WCET of `gsm_enc` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

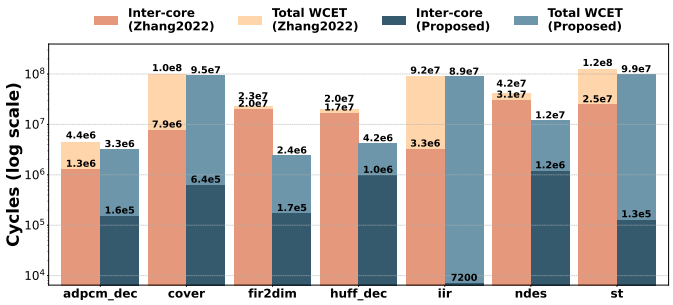


Fig. 25: Inter-core cache interference and total WCET of `h264_dec` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

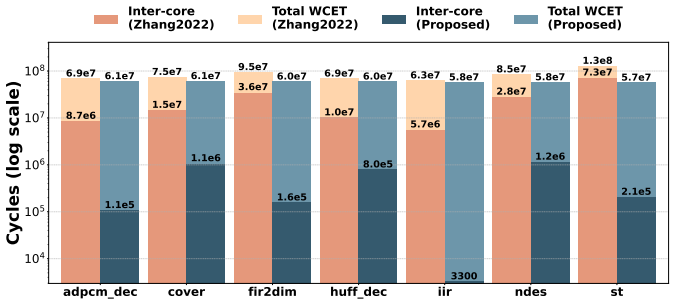


Fig. 26: Inter-core cache interference and total WCET of `lift` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

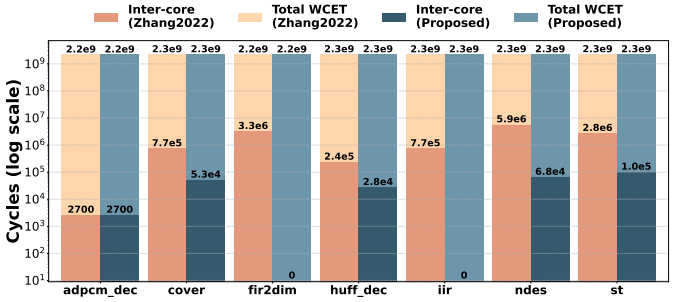


Fig. 27: Inter-core cache interference and total WCET of `md5` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

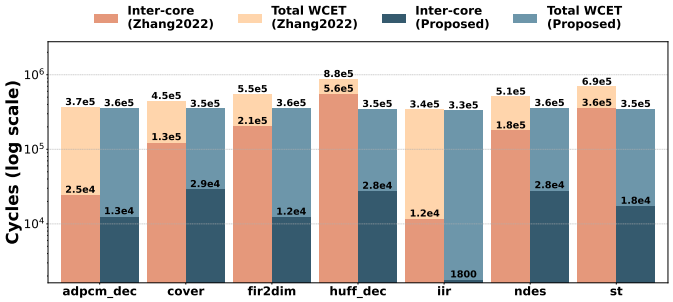


Fig. 28: Inter-core cache interference and total WCET of `minver` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

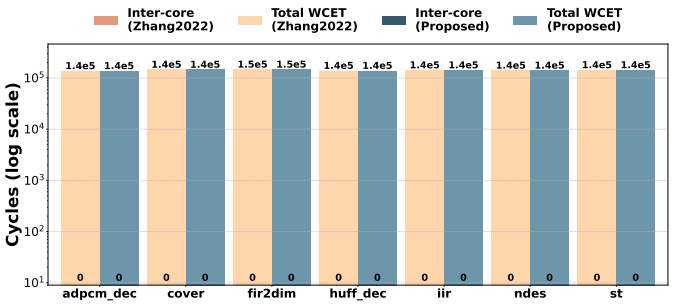


Fig. 29: Inter-core cache interference and total WCET of `petrinet` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

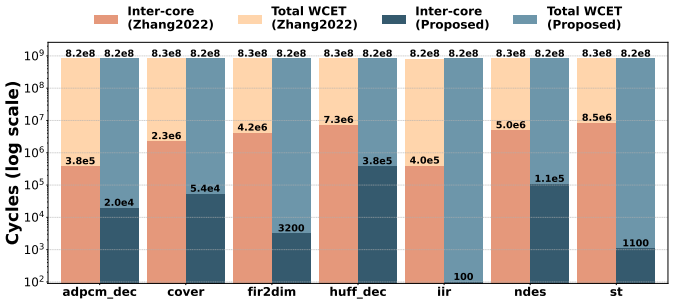


Fig. 30: Inter-core cache interference and total WCET of `pm` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

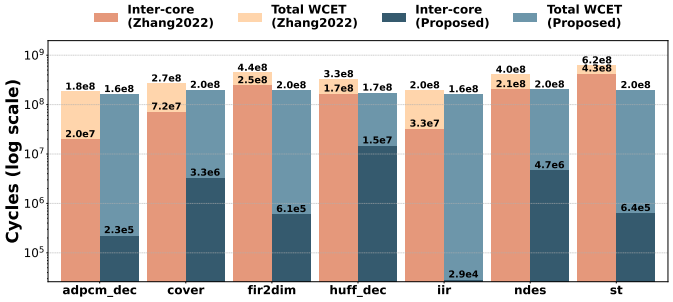


Fig. 31: Inter-core cache interference and total WCET of `powerwindow` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

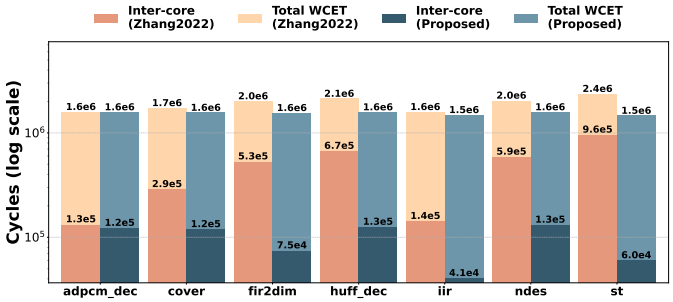


Fig. 32: Inter-core cache interference and total WCET of `prime` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

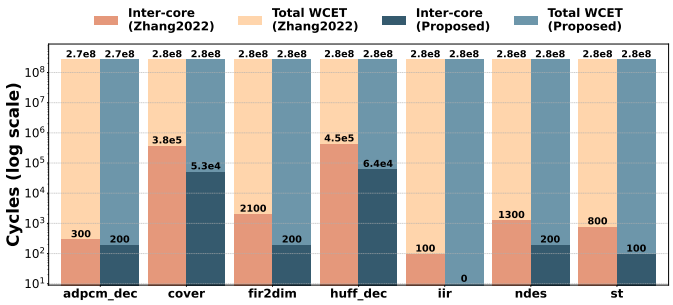


Fig. 33: Inter-core cache interference and total WCET of `sha` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

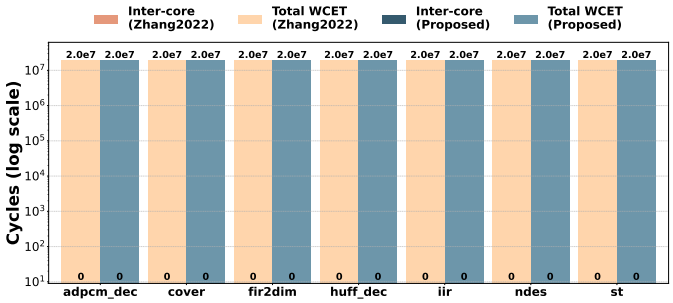


Fig. 34: Inter-core cache interference and total WCET of `bsort` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

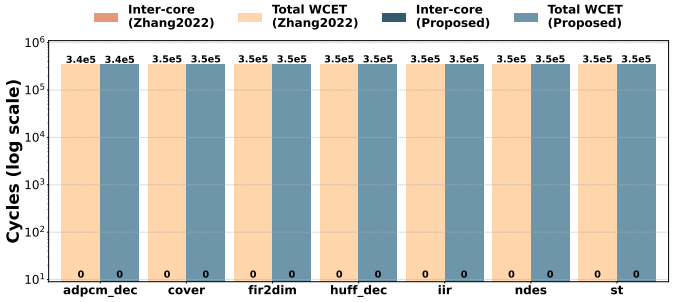


Fig. 35: Inter-core cache interference and total WCET of `cover` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

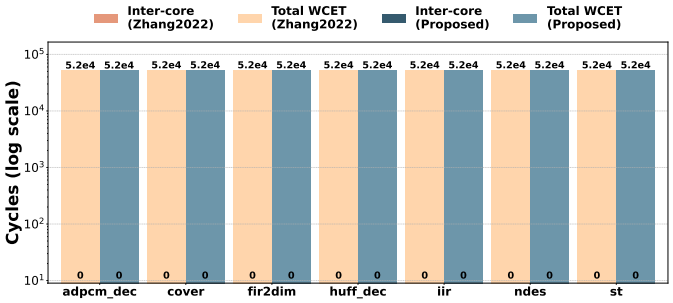


Fig. 36: Timing estimations of `complex_updates` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core interference; light colours: WCET).*

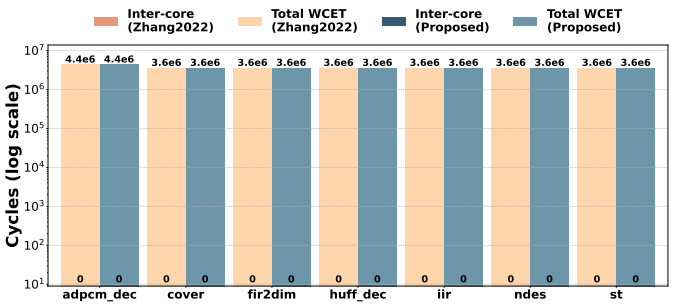


Fig. 37: Inter-core cache interference and total WCET of `cjpeg_wrbmp` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

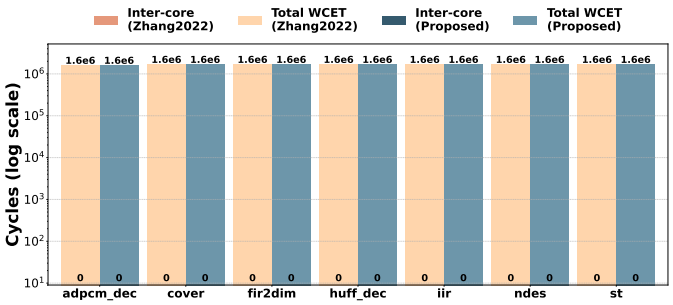


Fig. 38: Inter-core cache interference and total WCET of `countnegative` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

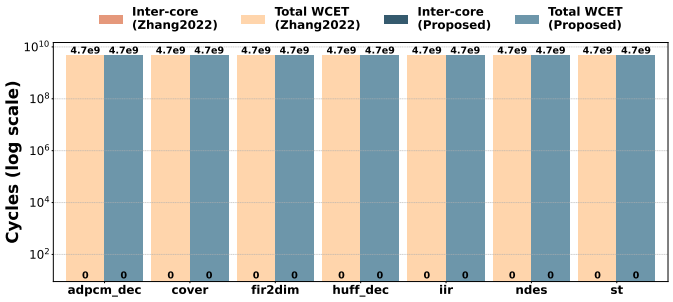


Fig. 39: Inter-core cache interference and total WCET of `fft` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

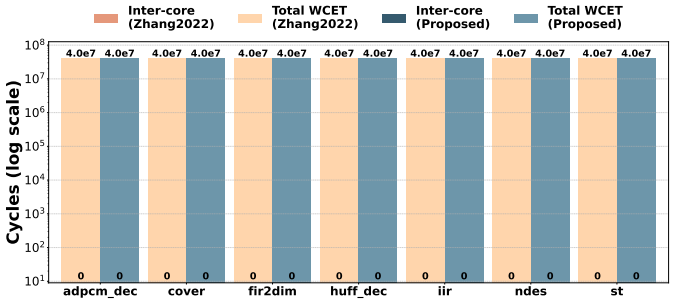


Fig. 40: Inter-core cache interference and total WCET of `filterbank` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

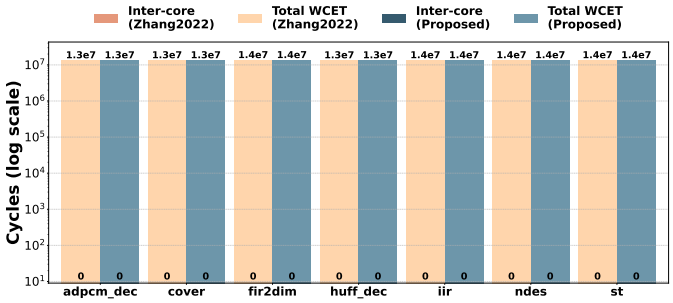


Fig. 41: Inter-core cache interference and total WCET of `lms` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

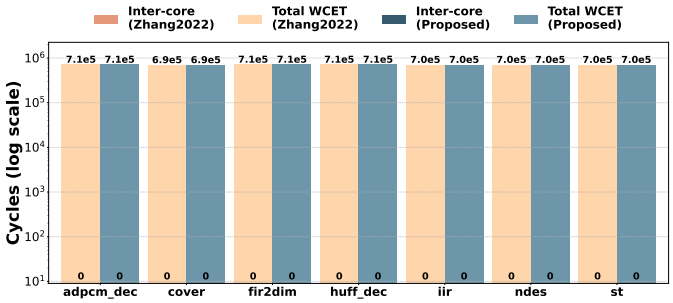


Fig. 42: Inter-core cache interference and total WCET of `ludcmp` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

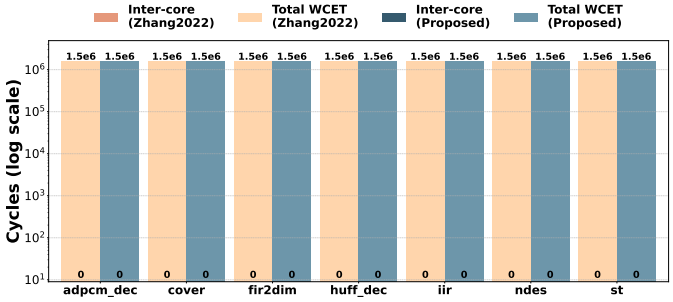


Fig. 43: Inter-core cache interference and total WCET of `matrix1` with $\kappa = 2$ *(y-axis: interfering task; dark colours: inter-core cache interference; light colours: WCET).*

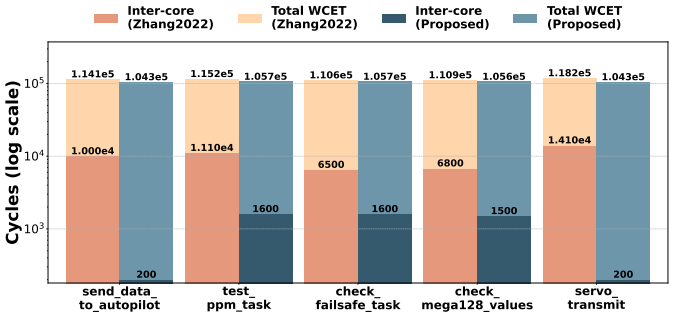


Fig. 44: Inter-core cache interference and WCET of the PapaBench task `radio_control_task` (AUTOPILOT) with $\kappa = 2$ *(y-axis: interfering task in FLY-BY-WIRE program; dark colours: inter-core cache interference; light colours: WCET).*

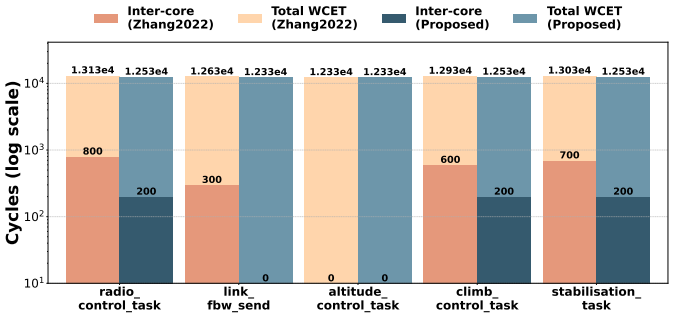


Fig. 45: Inter-core cache interference and total WCET of the PapaBench task `send_data_to_autopilot_task` (FLY-BY-WIRE) with $\kappa = 2$ *(y-axis: interfering task in AUTOPILOT program; dark colours: inter-core cache interference; light colours: WCET).*