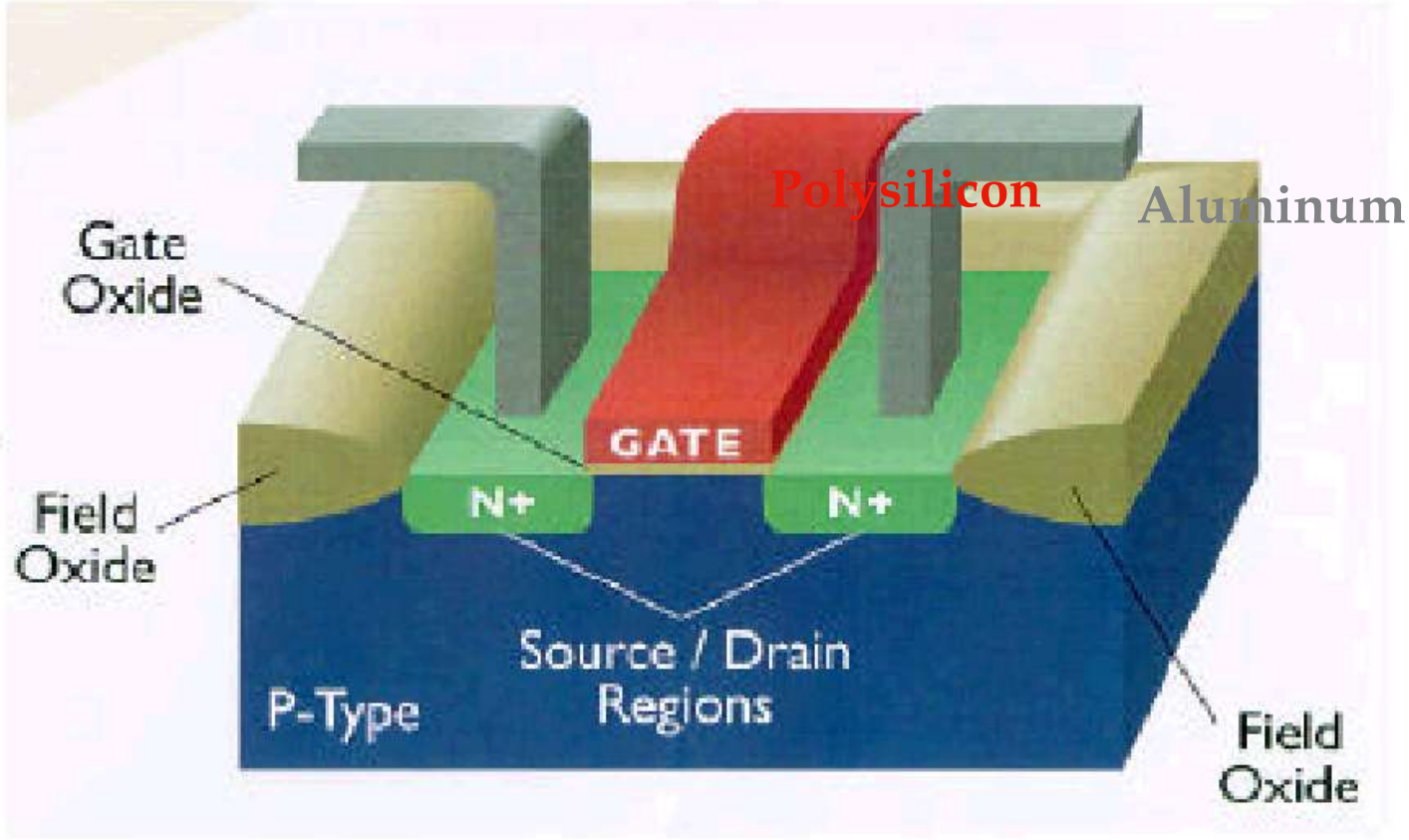
The MOS Transistor

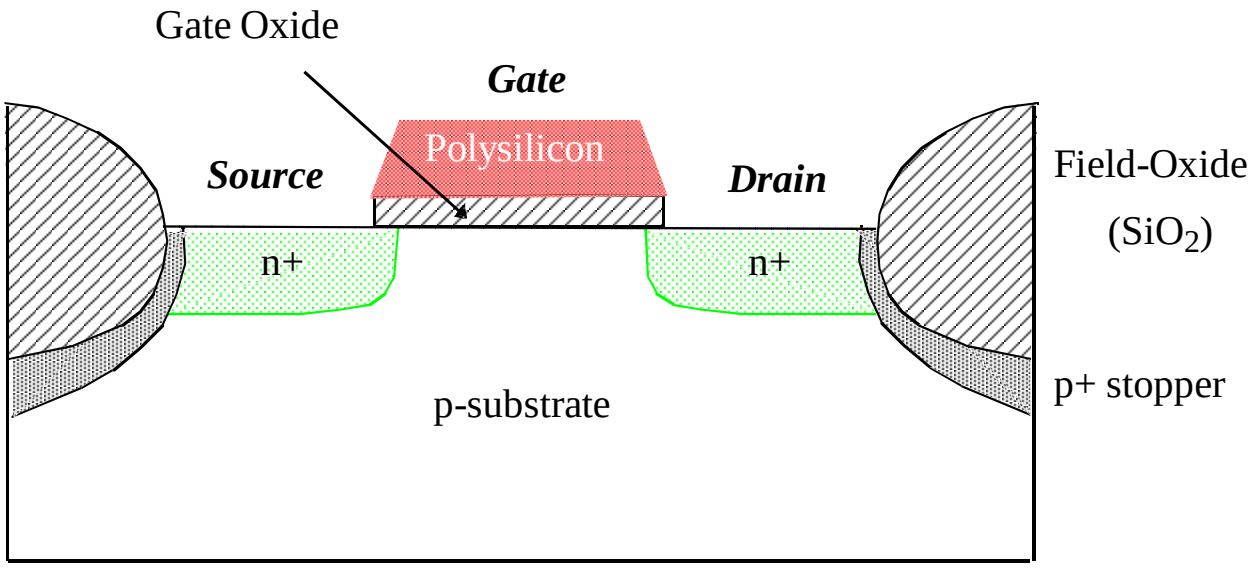


JFET – **J**unction **F**ield **E**ffect **T**ransistor

MOSFET - **M**etal **O**xide **S**emiconductor Field Effect Transistor

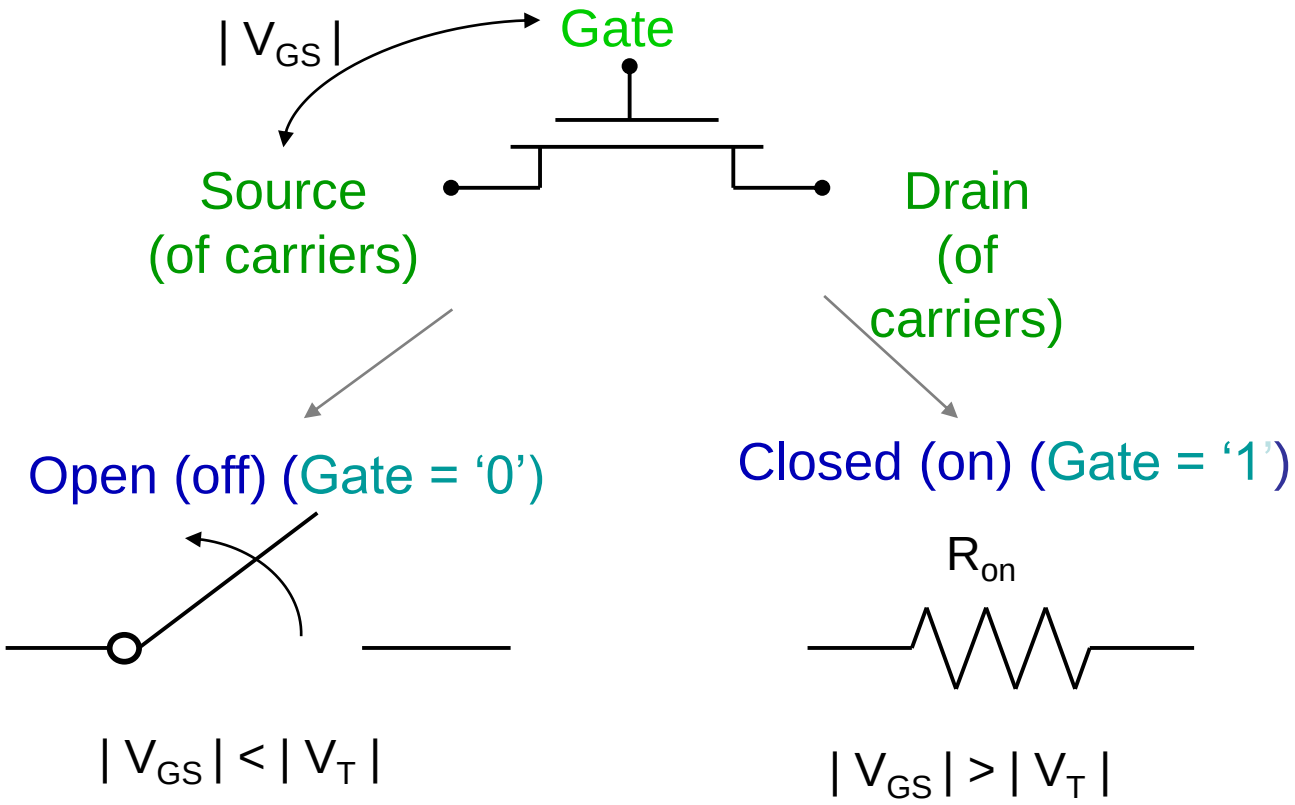
n-channel MOSFET (nMOS) & p-channel MOSFET (pMOS)

The MOS Transistor

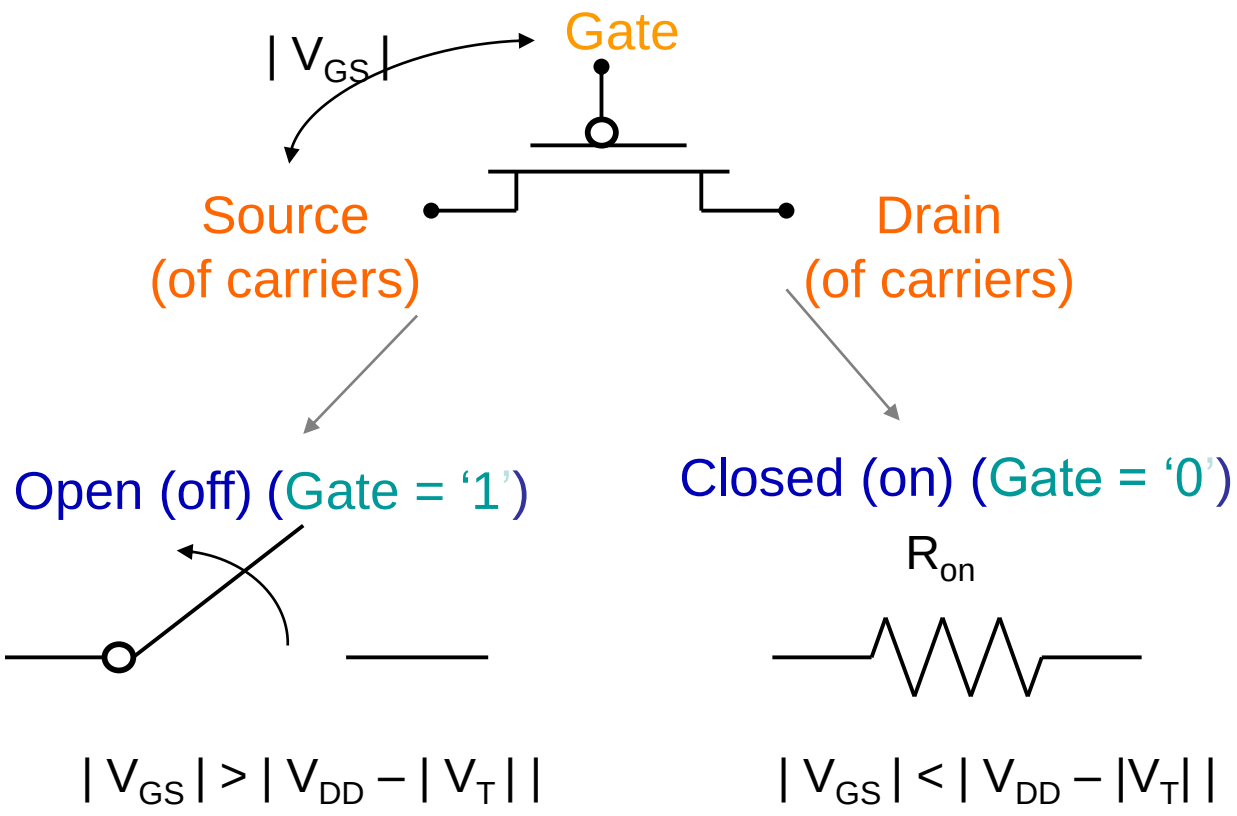


CROSS-SECTION of NMOS Transistor

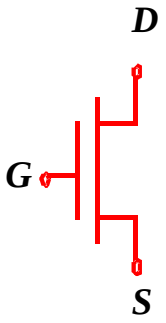
Switch Model of NMOS Transistor



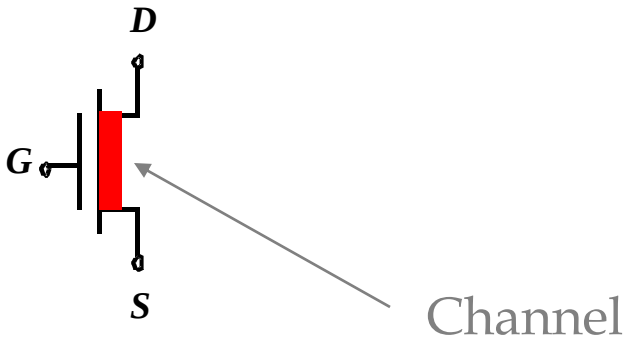
Switch Model of PMOS Transistor



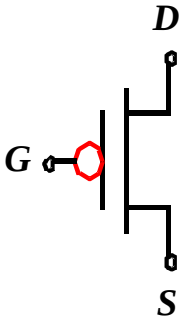
MOS transistors Symbols



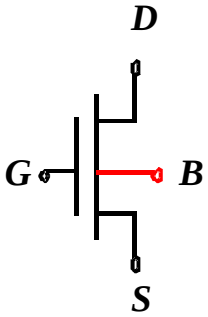
NMOS Enhancement



NMOS Depletion

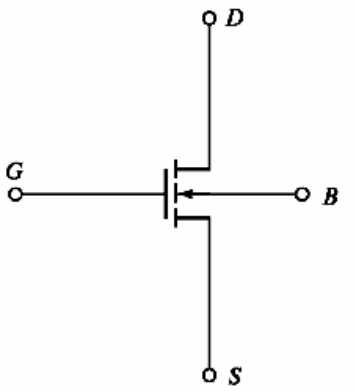


PMOS Enhancement



NMOS with Bulk Contact

JFET and MOSFET Transistorsor



Symbol

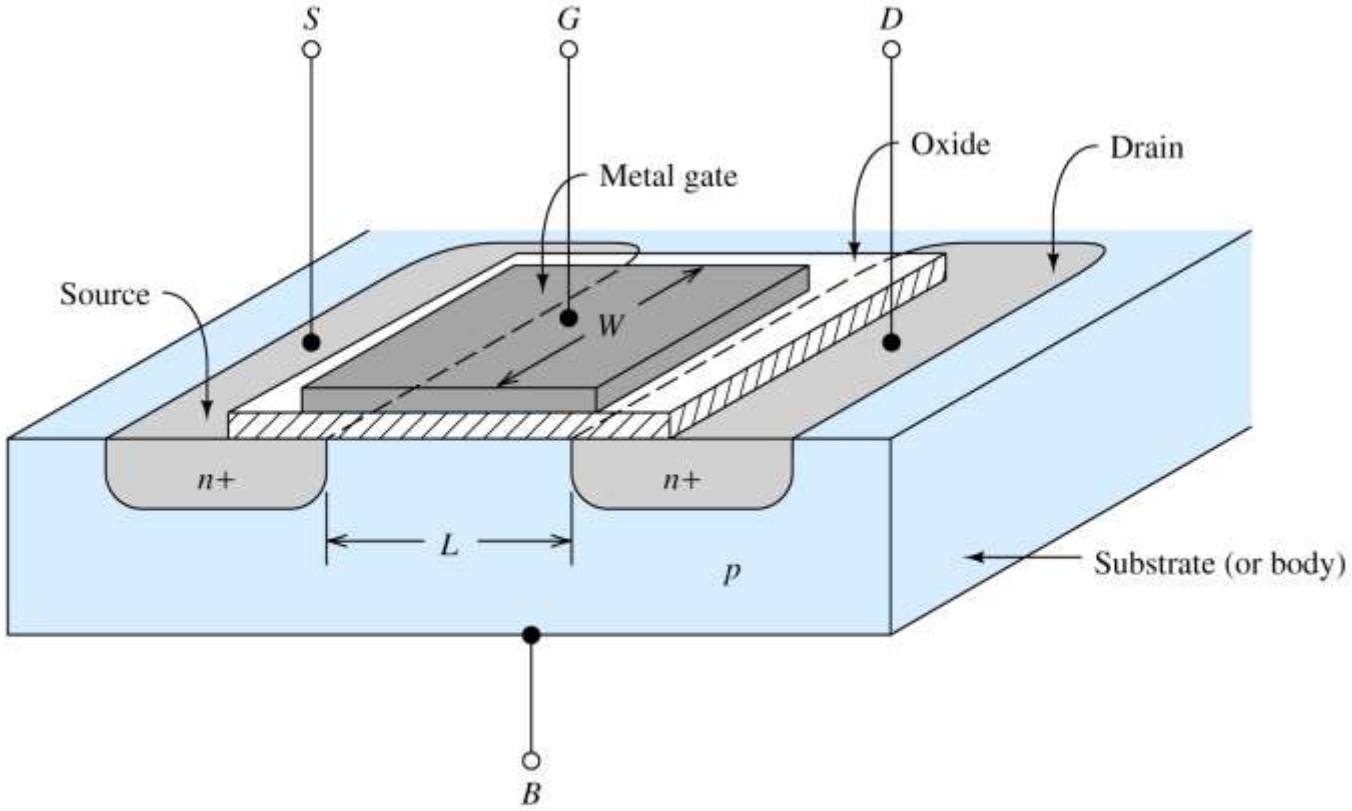


Figure 12.1 n-channel enhancement MOSFET showing channel length L and channel width W.

L = 0.5-10 μm
W = 0.5-500 μm

SiO_2 Thickness = 0.02-0.1 μm

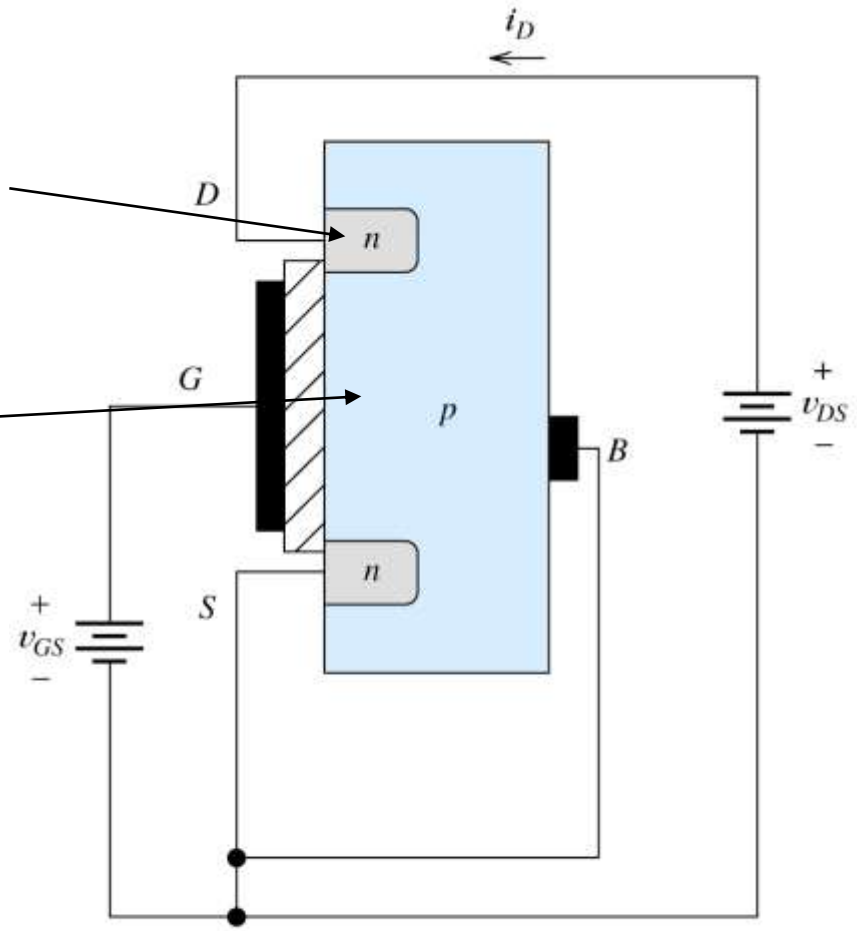
Device characteristics depend on L,W, Thickness, doping levels

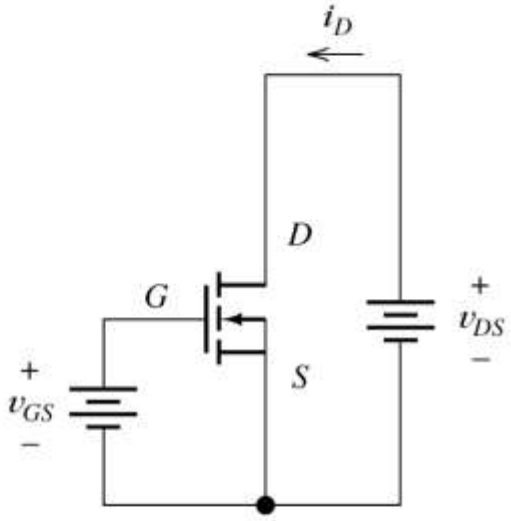
n-channel MOSFET Basic Operation

Operation in the Cutoff region

pn junction:
reverse bias

i_D=0
for v_{GS}<V_{t0}





Schematic

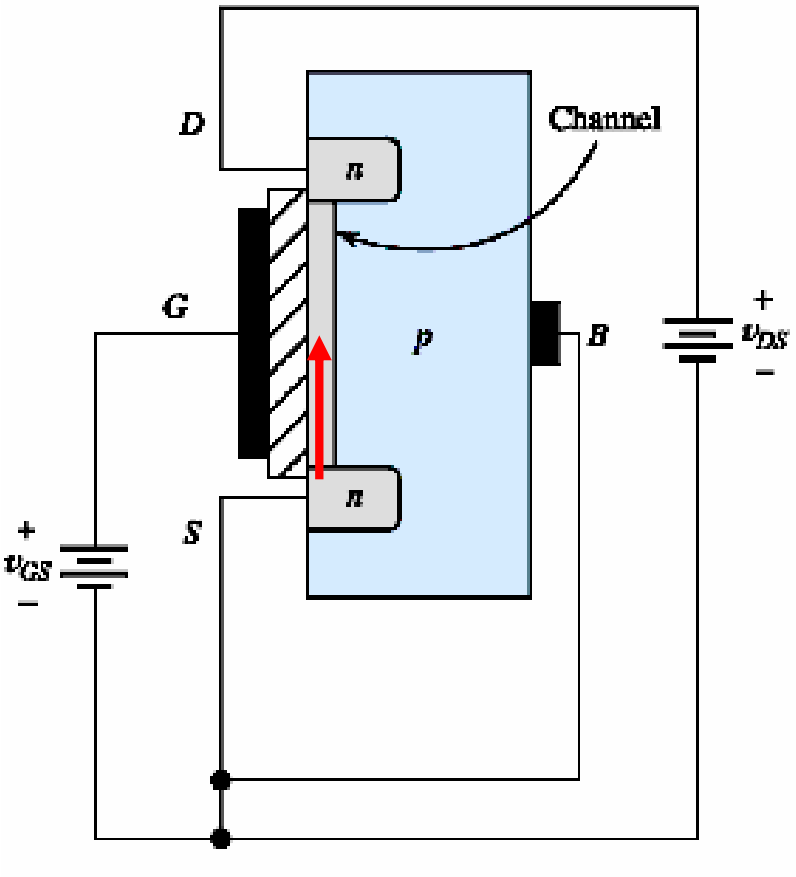
Figure 12.3 For $v_{GS} < V_{to}$, the pn junction between drain and body is reverse biased and $i_D = 0$.

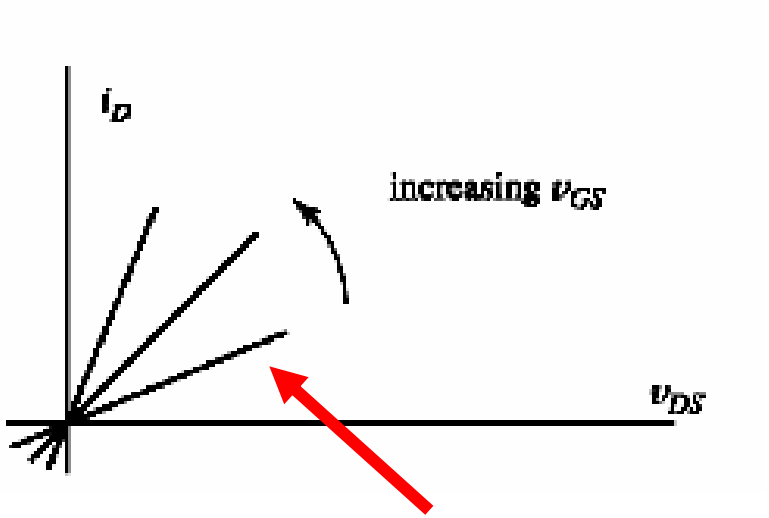
When v_{GS}=0 then i_D=0 until v_{GS}>V_{t0} (V_{t0} -threshold voltage)

n-channel MOSFET Basic Operation

Operation in the Triode Region

For $v_{DS} < v_{GS} - V_{t0}$ and $v_{GS} > V_{t0}$ the NMOS is operating in the triode region



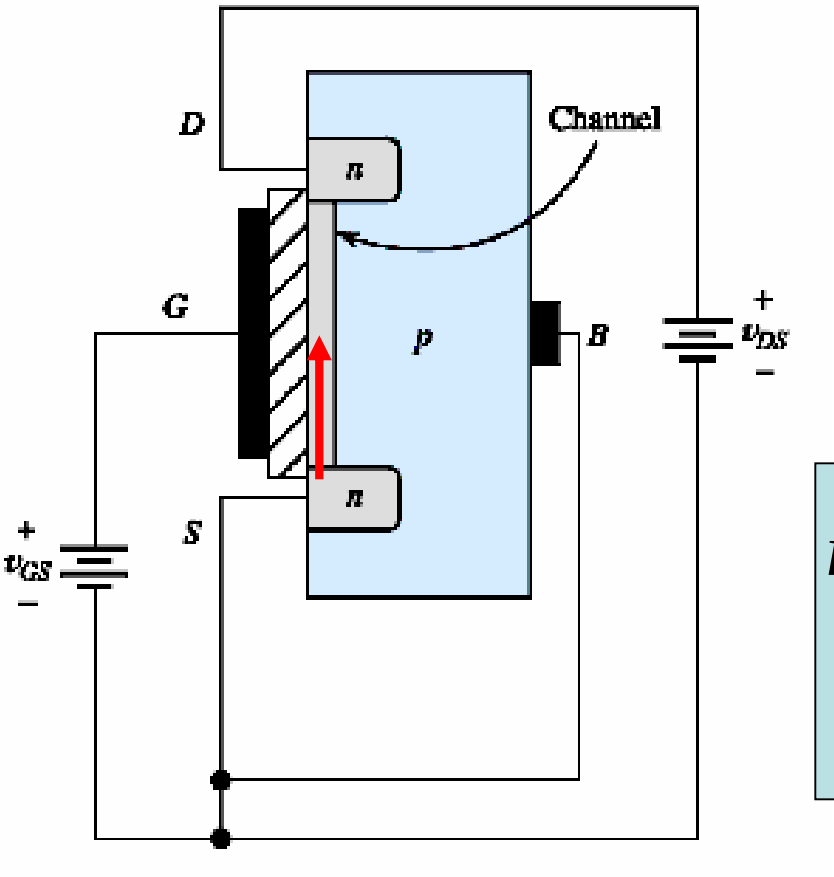


Resistor like characteristic
(R between S & D,
Used as voltage controlled R)

For small v_{DS}, i_D is proportional to the excess voltage $v_{GS} - V_{t0}$

n-channel MOSFET Basic Operation

Operation in the Triode Region



$$i_D = K\left[2\left(v_{GS} - V_{t0}\right)v_{DS} - v_{DS}^2\right]$$

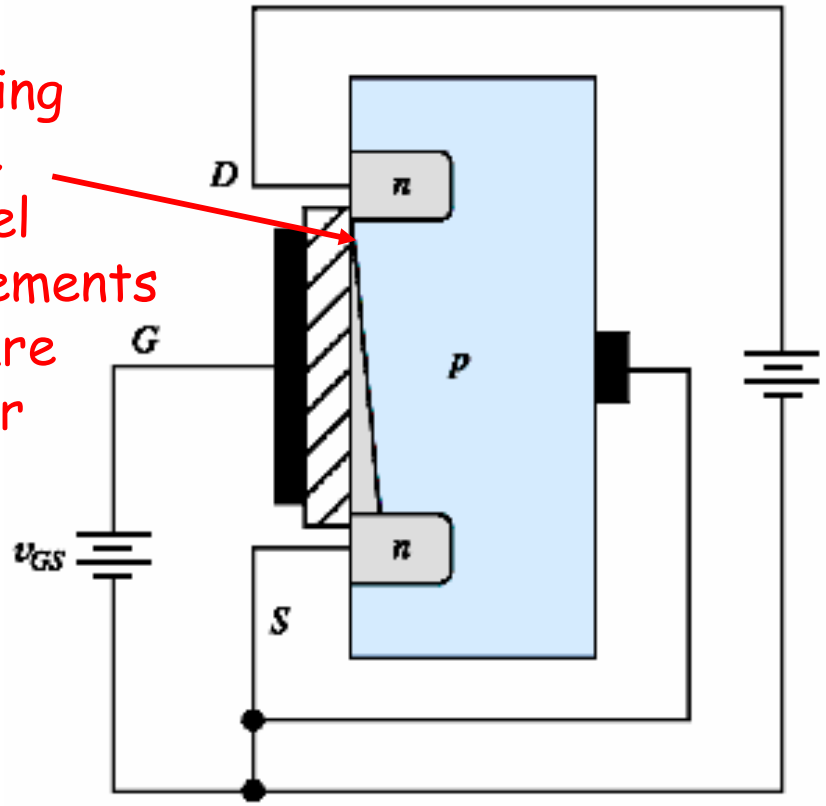
$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

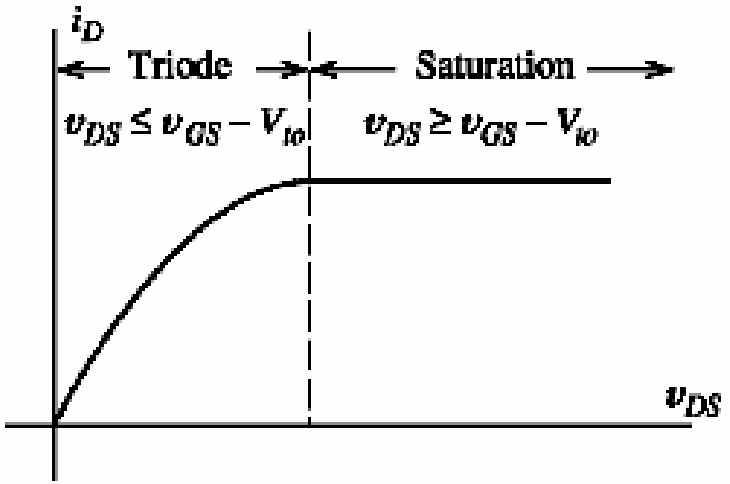
Device parameter KP for NMOSFET is 50 $\mu A/V^2$

n-channel MOSFET Basic Operation

Operation in the Saturation Region (v_{DS} is increased)

Tapering of the channel - increments of i_D are smaller when v_{DS} is larger





When $v_{GD}=V_{t0}$ then the channel thickness is 0 and

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

n-channel MOSFET Basic Operation

Example 12.1

An nMOS has W=160 μm, L=2 μm, KP= 50 μA/V^2 and V_{to}=2 V.

Plot the drain current characteristic vs drain to source voltage for v_{GS}=3 V.

$$i_D = K\left[2\left(v_{GS} - V_{t0}\right)v_{DS} - v_{DS}^2\right]$$

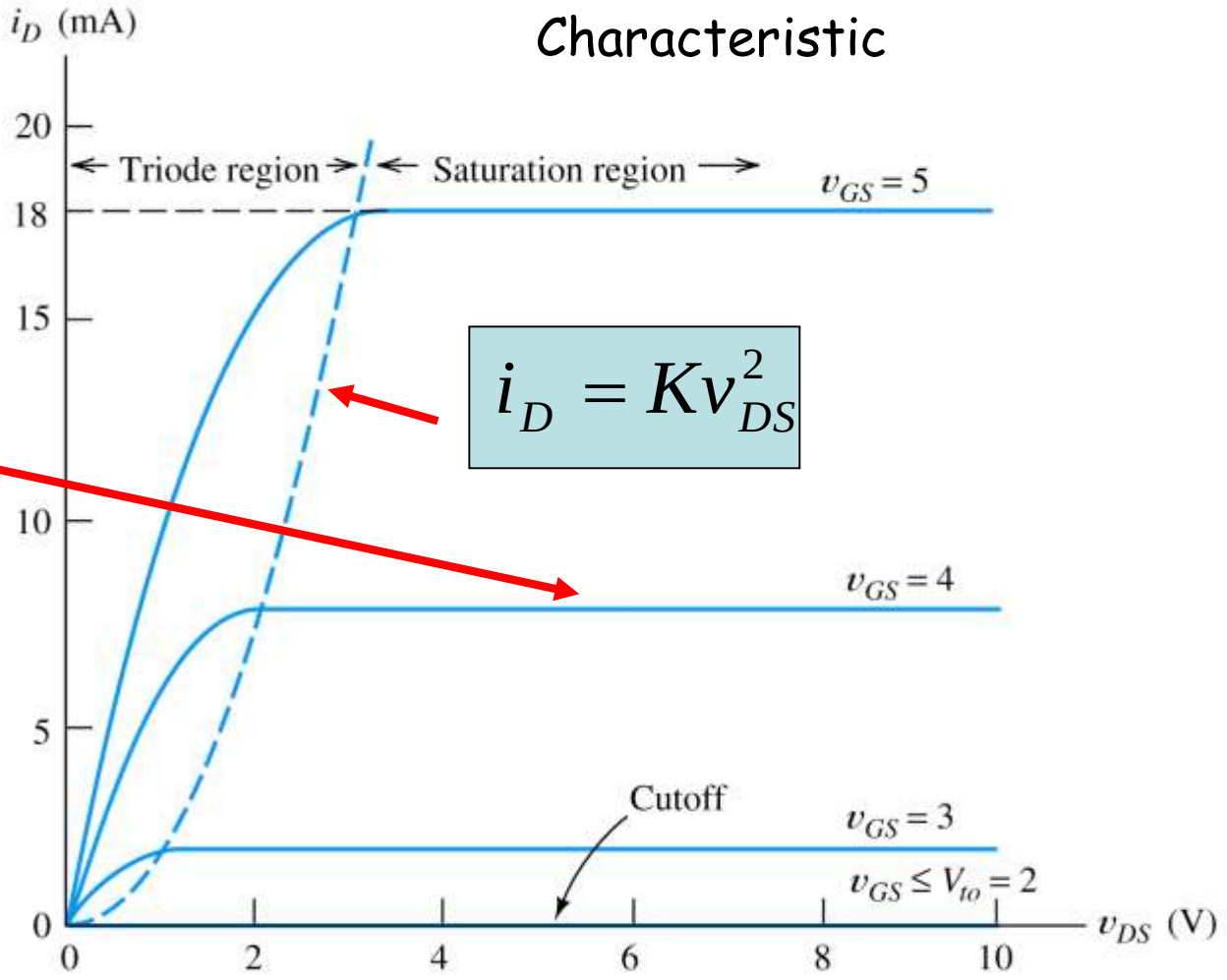
$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

$$K = \left(\frac{W}{L}\right)\frac{KP}{2}$$

n-channel MOSFET Basic Operation

Example 12.1

Characteristic



$$i_D = Kv_{DS}^2$$

Channel length modulation

i_d depends on v_{DS} in saturation region (approx: i_D =const in saturation region)

Figure 12.6 Characteristic curves for an NMOS transistor.

p-channel MOSFET Basic Operation

It is constructed by interchanging the *n* and *p* regions of n-channel MOSFET.

Symbol

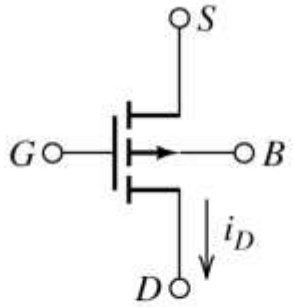


Figure 12.8 Circuit symbol for PMOS transistor.

Characteristic

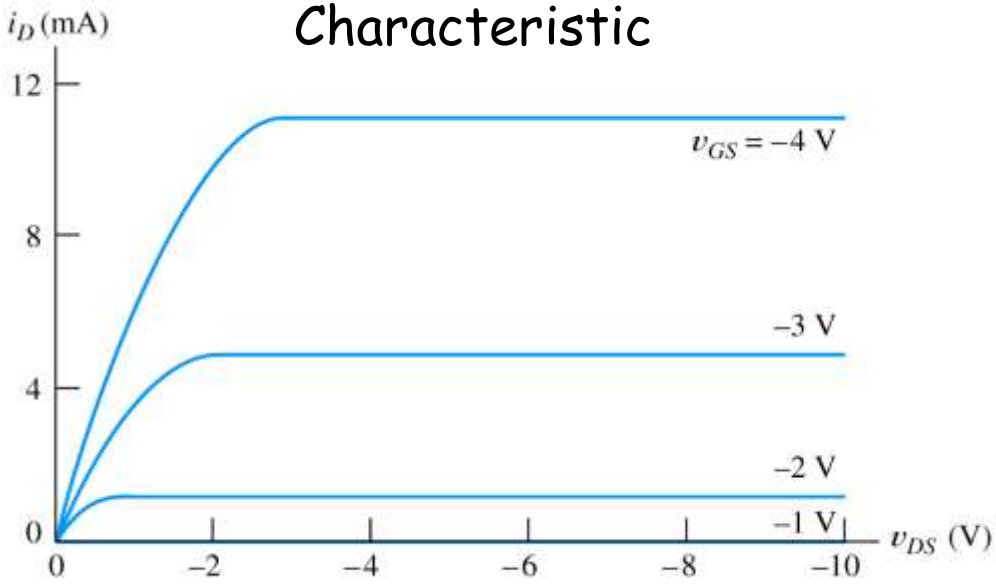
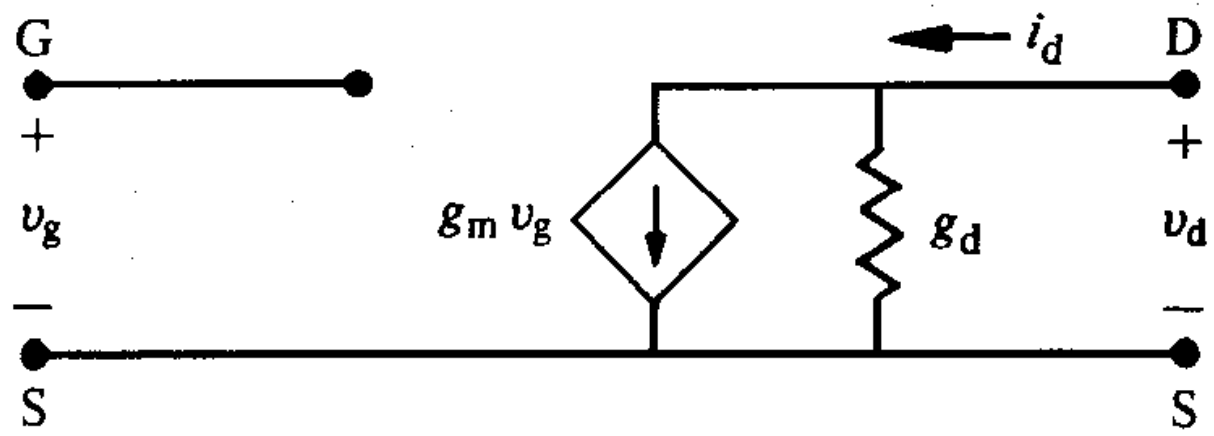


Figure 12.9 Answer for Exercise 12.3.

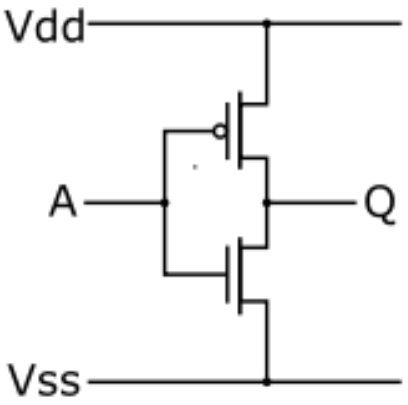
How does p-channel MOSFET operate?
-voltage polarities
-i_D current
-schematic

Equivalentna šema u oblasti zasićenja

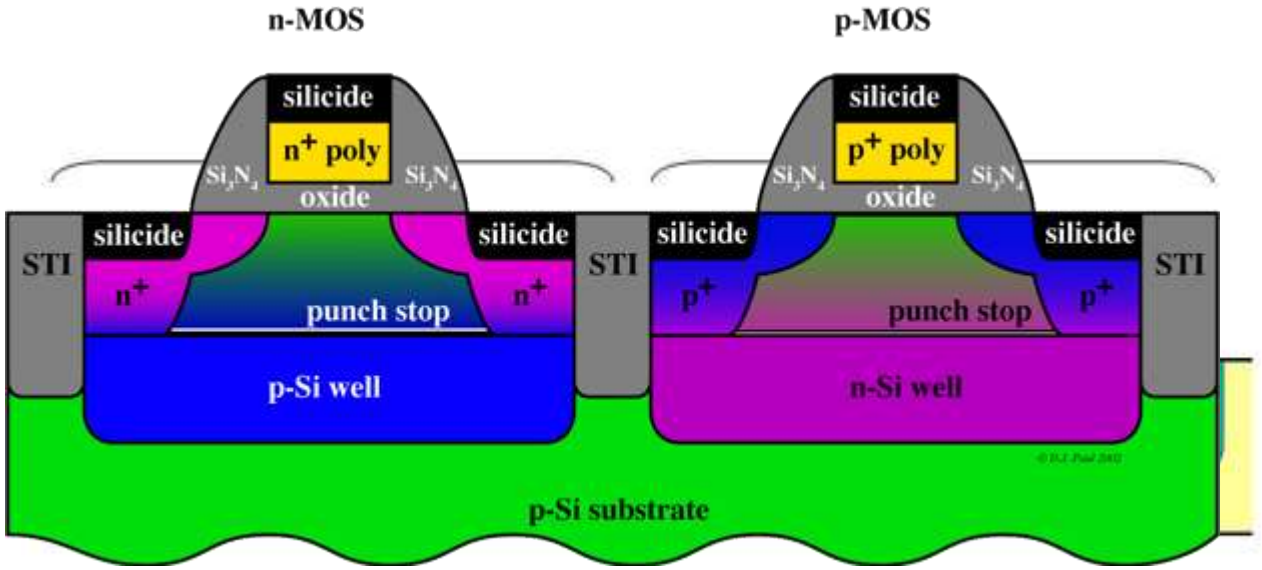


- Gate se ponaša kao otvoreno kolo
- S-D izlazno kolo se ponaša kao strujni izvor

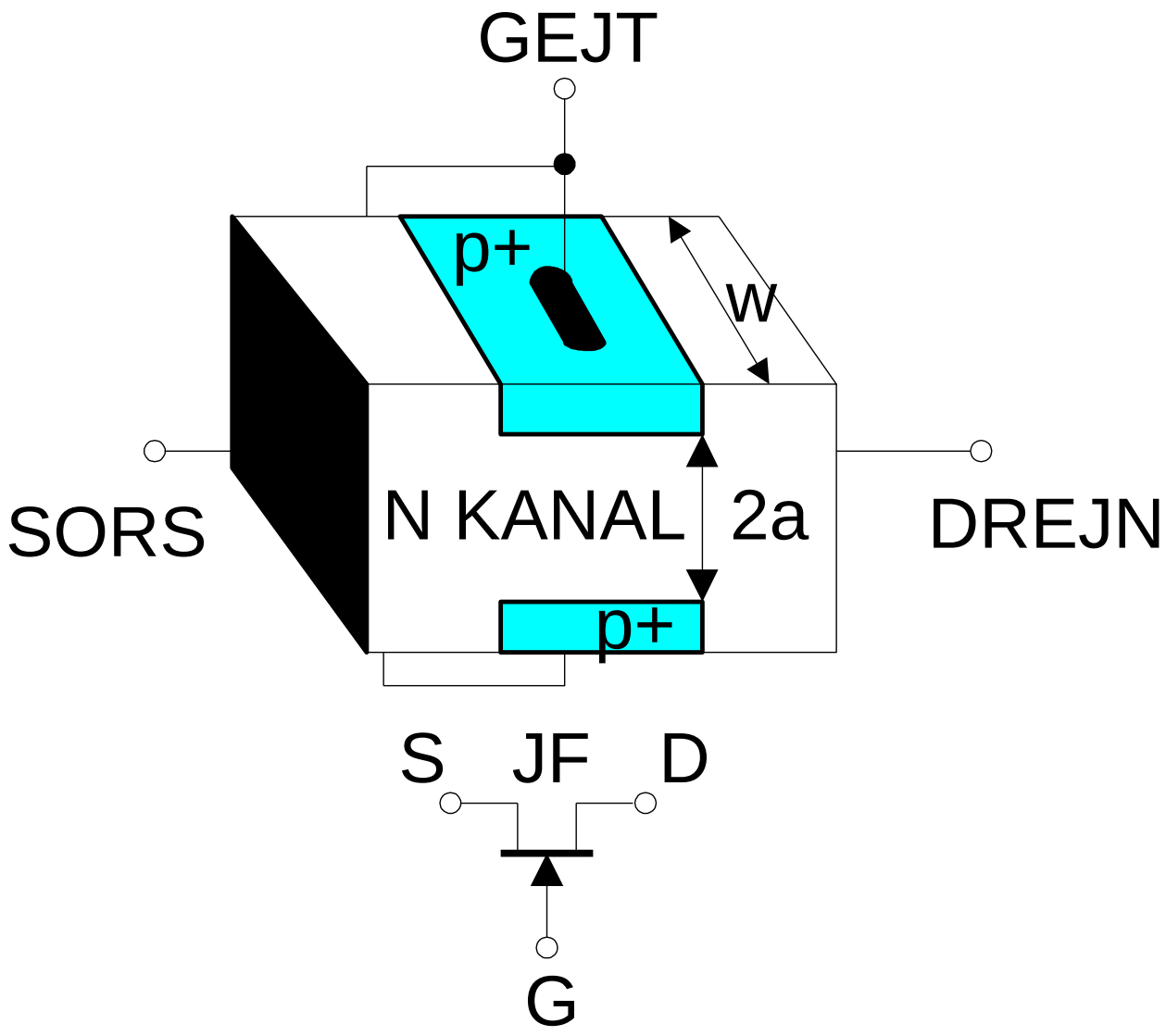
CMOS



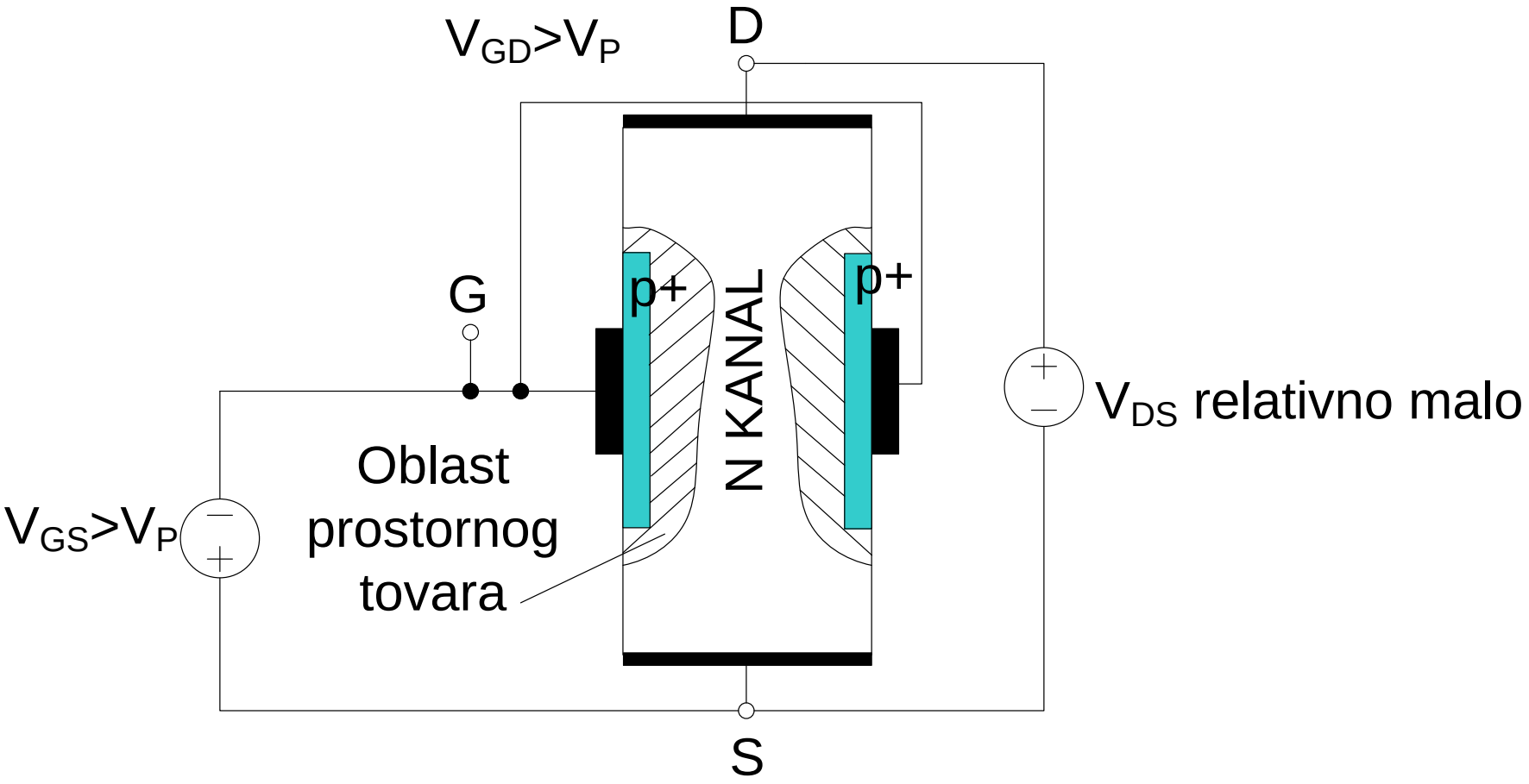
NOT gate (inverter)



Konstrukcija JFET - a



Geometrija provodnog kanala u omskoj oblasti rada JFET –a



Izlazna karakteristika JFET -a

- **Uštinućam kanala, tj. povećanje napona V_{DS} ipak dovodi do smanjenja dužine neuštinutog dela kanala i tako da se izlazne karakteristike u izvesnoj meri iskose**
- **Ova pojava može se modelovati po ugledu na bipolarne tranzistore sa erlijevim naponom V_A, data izrazom**

$$I_D = \left(1 + \frac{V_{DS}}{V_A}\right) I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$