Lab Final - FlipFlops, Displays, and Math!

In this lab, you combine everything you've learned over this semester into one functional design.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Semester Summary

Summarize your learnings from the lab over the whole semester here.
In this lab specifically, we used D-flipflops to create a clock divider, demux, and decode block for seven segment displays with math blocks to create basic calculator logic. Over the semester we have explored how digital logic works and how verilog replicates this in the code editor. We've used different devices such as multiplexers, demultiplexers, encoders, decoders, and state machines to experiment with and manipulate digital logic to make it practical. We've also experimented with implementing synchronous logic circuits with edge-triggered devices to influence different behaviors of a circuit. Overall, we have learned about all of the common devices and logic used in very complex circuits that create the electronics we use everyday today.

Lab Questions

1 - Which state machine design did you use for the scanner, and why?

For our scanner, we created a moore state machine using d flip-flops. This type of state machine allowed us to prioritize predictability and synchronous output. Additionally, it created a simpler implementation which was easier to understand.

2 - What function is the selection logic in the decoder representing? Think functional blocks.

The function that the selection logic in the decoder is representing is which of the segments on the seven segment display light up. For example, to represent 0, the case would be every single segment being lit up besides the middle. This selection logic allows us to correctly display a 4 bit number on a SSD.

3 - What would happen if we did not divide down the clock feeding into the scanner?

A high frequency clock without division would be too fast for the scanner to process data at, likely resulting in missed data or incorrect outputs. The scanner relies on a properly synchronized clock to control the timing of operations.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.