

# Lab 05 - Combinatorial Logic

In this lab, you've learned real world applications of digital logic, as well as how to assemble your own Verilog modules. In addition, you've learned how the constraints file maps your inputs and outputs to real pins on the FPGA.

## Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

## Lab Summary

Summarize your learnings from the lab here.

This lab taught us how to create our own verilog modules and how adders work in the verilog language. We also learned how to map FPGA pins to inputs and outputs using the constraints file. We've learned how to implement full adders in our logic to create a 2 bit adder using switches.

## Lab Questions

### 1 - Explain the role of the Top Level file.

The top level file dictates the behavior of the switch and LEDs, and this specific file creates a staircase design light system. It uses full adders to simulate adding bits with carry ins and carry outs and a wire which completes the logic.

### 2 - Explain the function of the Constraints file.

The constraints file maps the FPGA inputs/outputs ports to specific physical pins on the FPGA board. It defines hardware connections between FPGA logic and external components such as

LEDs and switches. It also ensures the FPGA knows which physical pins correspond to logical signals.

### 3 - How might one add more than two bits together?

Using different full adders such as the ripple carry adder can add more than 2 bits together.

## Code Submission

Upload a .zip of all your code or a public repository on GitHub.