MSP432P4xx Pin Functions

FUNCTION	SIGNAL NAME	Pin	Alt Pin	PIN(PZ)	ALT(PZ)	SIG TYP	DESCRIPTION
ADC	A0	P5.5		69		I	ADC analog input A0
	A1	P5.4		68		I	ADC analog input A1
	A2	P5.3		67		I	ADC analog input A2
	A3	P5.2		66		I	ADC analog input A3
	A4	P5.1		65		I	ADC analog input A4
	A5	P5.0		64		I	ADC analog input A5
	A6	P4.7		63		I	ADC analog input A6
	A7	P4.6		62		I	ADC analog input A7
	A8	P4.5		61		I	ADC analog input A8
	A9	P4.4		60		I	ADC analog input A9
	A10	P4.3		59		I	ADC analog input A10
	A11	P4.2		58		I	ADC analog input A11
	A12	P4.1		57		I	ADC analog input A12
	A13	P4.0		56		I	ADC analog input A13
	A14	P6.1		55		I	ADC analog input A14
	A15	P6.0		54		I	ADC analog input A15
	A16	P9.1		53		I	ADC analog input A16
	A17	P9.0		52		I	ADC analog input A17
	A18	P8.7		51		I	ADC analog input A18
	A19	P8.6		50		I	ADC analog input A19
	A20	P8.5		49		I	ADC analog input A20
	A21	P8.4		48		I	ADC analog input A21
	A22	P8.3		47		I	ADC analog input A22
	A23	P8.2		46		I	ADC analog input A23
Clock	ACLK	P4.2		58		O	ACLK clock output
	DCOR			44			DCO external resistor pin
	HFXIN	PJ.3		86		I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	PJ.2		85		O	Output for high-frequency crystal oscillator HFXT
	HSMCLK	P4.4		60		O	HSMCLK clock output
	LFXIN	PJ.0		41		I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	PJ.1		42		O	Output of low-frequency crystal oscillator LFXT
	MCLK	P4.3		59		O	MCLK clock output
Comparator	C0.0	P8.1		31		I	Comparator_E0 input 0
	C0.1	P8.0		30		I	Comparator_E0 input 1
	C0.2	P7.7		29		I	Comparator_E0 input 2
	C0.3	P7.6		28		I	Comparator_E0 input 3

	C0.4	P7.5		27		I	Comparator_E0 input 4
	C0.5	P7.4		26		I	Comparator_E0 input 5
	C0.6	P10.5		25		I	Comparator_E0 input 6
	C0.7	P10.4		24		I	Comparator_E0 input 7
	C1.0	P6.7		81		I	Comparator_E1 input 0
	C1.1	P6.6		80		I	Comparator_E1 input 1
	C1.2	P6.5		79		I	Comparator_E1 input 2
	C1.3	P6.4		78		I	Comparator_E1 input 3
	C1.4	P6.3		77		I	Comparator_E1 input 4
	C1.5	P6.2		76		I	Comparator_E1 input 5
	C1.6	P5.7		71		I	Comparator_E1 input 6
	C1.7	P5.6		70		I	Comparator_E1 input 7
LCD	L0	P3.7		39		O	LCD drive pin 0 for either segment or common output
	L1	P3.6		38		O	LCD drive pin 1 for either segment or common output
	L2	P3.5		37		O	LCD drive pin 2 for either segment or common output
	L3	P3.4		36		O	LCD drive pin 3 for either segment or common output
	L4	P3.3		35		O	LCD drive pin 4 for either segment or common output
	L5	P3.2		34		O	LCD drive pin 5 for either segment or common output
	L6	P3.1		33		O	LCD drive pin 6 for either segment or common output
	L7	P3.0		32		O	LCD drive pin 7 for either segment or common output
	L8	P2.3		19		O	LCD drive pin 8 for either segment or common output
	L9	P2.2		18		O	LCD drive pin 9 for either segment or common output
	L10	P2.1		17		O	LCD drive pin 10 for either segment or common output
	L11	P2.0		16		O	LCD drive pin 11 for either segment or common output
	L12	P1.7	P4.1	11	57	O	LCD drive pin 12 for either segment or common output
	L13	P1.6	P4.0	10	56	O	LCD drive pin 13 for either segment or common output
	L14	P1.5	P6.1	9	55	O	LCD drive pin 14 for either segment or common output
	L15	P1.4	P6.0	8	54	O	LCD drive pin 15 for either segment or common output
	L16	P1.3	P9.1	7	53	O	LCD drive pin 16 for either segment or common output
	L17	P1.2	P9.0	6	52	O	LCD drive pin 17 for either segment or common output
	L18	P1.1	P8.7	5	51	O	LCD drive pin 18 for either segment or common output
	L19	P1.0	P8.6	4	50	O	LCD drive pin 19 for either segment or common output
	L20	P2.7		23		O	LCD drive pin 20 for either segment or common output
	L21	P2.6		22		O	LCD drive pin 21 for either segment or common output
	L22	P2.5		21		O	LCD drive pin 22 for either segment or common output
	L23	P2.4		20		O	LCD drive pin 23 for either segment or common output

	L24	P6.5		79		O	LCD drive pin 24 for either segment or common output
	L25	P6.4		78		O	LCD drive pin 25 for either segment or common output
	L26	P6.3		77		O	LCD drive pin 26 for either segment or common output
	L27	P6.2		76		O	LCD drive pin 27 for either segment or common output
	L28	P7.7		29		O	LCD drive pin 28 for either segment or common output
	L29	P7.6		28		O	LCD drive pin 29 for either segment or common output
	L30	P7.5		27		O	LCD drive pin 30 for either segment or common output
	L31	P7.4		26		O	LCD drive pin 31 for either segment or common output
	L32	P9.3		75		O	LCD drive pin 32 for either segment or common output
	L33	P9.2		74		O	LCD drive pin 33 for either segment or common output
	L34	P10.5		25		O	LCD drive pin 34 for either segment or common output
	L35	P10.4		24		O	LCD drive pin 35 for either segment or common output
	L36	P10.3		3		O	LCD drive pin 36 for either segment or common output
	L37	P10.2		2		O	LCD drive pin 37 for either segment or common output
	L38	P10.1		1		O	LCD drive pin 38 for either segment or common output
	L39	P10.0		100		O	LCD drive pin 39 for either segment or common output
	L40	P9.7		99		O	LCD drive pin 40 for either segment or common output
	L41	P9.6		98		O	LCD drive pin 41 for either segment or common output
	L42	P9.5		97		O	LCD drive pin 42 for either segment or common output
	L43	P9.4		96		O	LCD drive pin 43 for either segment or common output
	L44	P8.5		49		O	LCD drive pin 44 for either segment or common output
	L45	P8.4		48		O	LCD drive pin 45 for either segment or common output
	L46	P8.3		47		O	LCD drive pin 46 for either segment or common output
	L47	P8.2		46		O	LCD drive pin 47 for either segment or common output
	R03	P7.0		88		I	Input port of fourth most positive analog LCD voltage V4 in external bias mode
	R13	P7.1		89		I	Input port of fourth most positive analog LCD voltage V3 in external bias mode
	R23	P7.2		90		I	Input port of fourth most positive analog LCD voltage V2 in external bias mode
	SWCLKTCK			95		I	Serial wire clock input (SWCLK)/JTAG clock input (TCK)
	SWDIOTMS			94		I/O	Serial wire data input/output (SWDIO)/JTAG test mode select (TMS)
Debug	SWO	PJ.5		93		O	Serial wire trace output
	TDI	PJ.4		92		I	JTAG test data input
	TDO	PJ.5		93		O	JTAG test data output
GPIO	P1.0	P1.0		4		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.1	P1.1		5		I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.2	P1.2		6		I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.3	P1.3		7		I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.4	P1.4		8		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.5	P1.5		9		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.6	P1.6		10		I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.7	P1.7		11		I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P2.0	P2.0		16		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA.
	P2.1	P2.1		17		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA.
	P2.2	P2.2		18		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with a drive capability of up to 20 mA.
	P2.3	P2.3		19		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can

						be configured for high drive operation with a drive capability of up to 20 mA.
P2.4	P2.4		20		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P2.5	P2.5		21		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P2.6	P2.6		22		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P2.7	P2.7		23		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P3.0	P3.0		32		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
P3.1	P3.1		33		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P3.2	P3.2		34		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P3.3	P3.3		35		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P3.4	P3.4		36		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
P3.5	P3.5		37		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
P3.6	P3.6		38		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P3.7	P3.7		39		I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
P4.0	P4.0		56		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.1	P4.1		57		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.2	P4.2		58		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.3	P4.3		59		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.4	P4.4		60		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.5	P4.5		61		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.6	P4.6		62		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P4.7	P4.7		63		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.0	P5.0		64		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.1	P5.1		65		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.2	P5.2		66		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.3	P5.3		67		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.4	P5.4		68		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.5	P5.5		69		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.6	P5.6		70		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P5.7	P5.7		71		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.0	P6.0		54		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.1	P6.1		55		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.2	P6.2		76		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.3	P6.3		77		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.4	P6.4		78		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.5	P6.5		79		I/O	General-purpose digital I/O with port interrupt and wake-up capability
P6.6	P6.6		80		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
P6.7	P6.7		81		I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
P7.0	P7.0		88		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
P7.1	P7.1		89		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
P7.2	P7.2		90		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)

	P7.3	P7.3		91		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.4	P7.4		26		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.5	P7.5		27		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.6	P7.6		28		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.7	P7.7		29		I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P8.0	P8.0		30		I/O	General-purpose digital I/O
	P8.1	P8.1		31		I/O	General-purpose digital I/O
	P8.2	P8.2		46		I/O	General-purpose digital I/O
	P8.3	P8.3		47		I/O	General-purpose digital I/O
	P8.4	P8.4		48		I/O	General-purpose digital I/O
	P8.5	P8.5		49		I/O	General-purpose digital I/O
	P8.6	P8.6		50		I/O	General-purpose digital I/O
	P8.7	P8.7		51		I/O	General-purpose digital I/O
	P9.0	P9.0		52		I/O	General-purpose digital I/O
	P9.1	P9.1		53		I/O	General-purpose digital I/O
	P9.2	P9.2		74		I/O	General-purpose digital I/O
	P9.3	P9.3		75		I/O	General-purpose digital I/O
	P9.4	P9.4		96		I/O	General-purpose digital I/O
	P9.5	P9.5		97		I/O	General-purpose digital I/O
	P9.6	P9.6		98		I/O	General-purpose digital I/O
	P9.7	P9.7		99		I/O	General-purpose digital I/O
	P10.0	P10.0		100		I/O	General-purpose digital I/O
	P10.1	P10.1		1		I/O	General-purpose digital I/O
	P10.2	P10.2		2		I/O	General-purpose digital I/O
	P10.3	P10.3		3		I/O	General-purpose digital I/O
	P10.4	P10.4		24		I/O	General-purpose digital I/O
	P10.5	P10.5		25		I/O	General-purpose digital I/O
	PJ.0	PJ.0		41		I/O	General-purpose digital I/O
	PJ.1	PJ.1		42		I/O	General-purpose digital I/O
	PJ.2	PJ.2		85		I/O	General-purpose digital I/O
	PJ.3	PJ.3		86		I/O	General-purpose digital I/O
	PJ.4	PJ.4		92		I/O	General-purpose digital I/O
	PJ.5	PJ.5		93		I/O	General-purpose digital I/O
I2C	UCB0SCL	P1.7		11		I/O	I2C clock in eUSCI_B0 I2C mode
	UCB0SDA	P1.6		10		I/O	I2C data in eUSCI_B0 I2C mode
	UCB1SCL	P6.5		79		I/O	I2C clock in eUSCI_B1 I2C mode
	UCB1SDA	P6.4		78		I/O	I2C data in eUSCI_B1 I2C mode
	UCB3SCL	P10.3		3		I/O	I2C clock in eUSCI_B3 I2C mode
	UCB3SCL	P6.7		81		I/O	I2C clock in eUSCI_B3 I2C mode
	UCB3SDA	P10.2		2		I/O	I2C data in eUSCI_B3 I2C mode
	UCB3SDA	P6.6		80		I/O	I2C data in eUSCI_B3 I2C mode
Port Mapper	PM_C0OUT	P7.1		89		O	Default mapping: Comparator_E0 output
	PM_C1OUT	P7.2		90		O	Default mapping: Comparator_E1 output
	PM_DMAE0	P7.0		88		I	Default mapping: DMA external trigger input
	PM_SMCLK	P7.0		88		O	Default mapping: SMCLK clock output
	PM_TA0.0	P7.3		91		I/O	Default mapping: TA0 CCR0 capture: CCI0A input, compare: Out0
	PM_TA0.1	P2.4		20		I/O	Default mapping: TA0 CCR1 capture: CCI1A input, compare: Out1
	PM_TA0.2	P2.5		21		I/O	Default mapping: TA0 CCR2 capture: CCI2A input, compare: Out2
	PM_TA0.3	P2.6		22		I/O	Default mapping: TA0 CCR3 capture: CCI3A input, compare: Out3
	PM_TA0.4	P2.7		23		I/O	Default mapping: TA0 CCR4 capture: CCI4A input, compare: Out4
	PM_TA0CLK	P7.1		89		I	Default mapping: TA0 input clock
	PM_TA1.2	P7.6		28		I/O	Default mapping: TA1 CCR2 capture: CCI2A input, compare: Out2
	PM_TA1.3	P7.5		27		I/O	Default mapping: TA1 CCR3 capture: CCI3A input, compare: Out3
	PM_TA1.4	P7.4		26		I/O	Default mapping: TA1 CCR4 capture: CCI4A input, compare: Out4
	PM_TA1CLK	P7.2		90		I	Default mapping: TA1 input clock

	PM_UCA1CLK	P2.1		17		I/O	Default mapping: Clock signal input in eUSCI_A1 SPI slave mode. Clock signal output in eUSCI_A1 SPI master mode
	PM_UCA1RXD	P2.2		18		I	Default mapping: Receive data in eUSCI_A1 UART mode
	PM_UCA1SIMO	P2.3		19		I/O	Default mapping: Slave in, master out for eUSCI_A1 SPI mode
	PM_UCA1SOMI	P2.2		18		I/O	Default mapping: Slave out, master in for eUSCI_A1 SPI mode
	PM_UCA1STE	P2.0		16		I/O	Default mapping: Slave transmit enable for eUSCI_A1 SPI mode
	PM_UCA1TXD	P2.3		19		O	Default mapping: Transmit data for eUSCI_A1 UART mode
	PM_UCA2CLK	P3.1		33		I/O	Default mapping: Clock signal input for eUSCI_A2 SPI slave mode. Clock signal output for eUSCI_A2 SPI master mode
	PM_UCA2RXD	P3.2		34		I	Default mapping: Receive data for eUSCI_A2 UART mode
	PM_UCA2SIMO	P3.3		35		I/O	Default mapping: Slave in, master out for eUSCI_A2 SPI mode
	PM_UCA2SOMI	P3.2		34		I/O	Default mapping: Slave out, master in for eUSCI_A2 SPI mode
	PM_UCA2STE	P3.0		32		I/O	Default mapping: Slave transmit enable for eUSCI_A2 SPI mode
	PM_UCA2TXD	P3.3		35		O	Default mapping: Transmit data for eUSCI_A2 UART mode
	PM_UCB2CLK	P3.5		37		I/O	Default mapping: Clock signal input for eUSCI_B2 SPI slave mode. Clock signal output for eUSCI_B2 SPI master mode
	PM_UCB2SCL	P3.7		39		I	Default mapping: I2C clock for eUSCI_B2 I2C mode
	PM_UCB2SDA	P3.6		38		I/O	Default mapping: I2C data for eUSCI_B2 I2C mode
	PM_UCB2SIMO	P3.6		38		I/O	Default mapping: Slave in, master out for eUSCI_B2 SPI mode
	PM_UCB2SOMI	P3.7		39		I/O	Default mapping: Slave out, master in for eUSCI_B2 SPI mode
	PM_UCB2STE	P3.4		36		I/O	Default mapping: Slave transmit enable for eUSCI_B2 SPI mode
Power	AVCC1			45			Analog power supply
	AVCC2			87			Analog power supply
	AVSS1			43			Analog ground supply
	AVSS2			84			Analog ground supply
	AVSS3			40			Analog ground supply
	DVCC1			13			Digital power supply
	DVCC2			73			Digital power supply
	DVSS1			15			Digital ground supply
	DVSS2			72			Digital ground supply
	DVSS3			82			Must be connected to ground
	VCORE			12			Regulated core power supply (internal use only, no external current loading)
	VSW			14			DC/DC converter switching output
RTC	RTCCLK	P4.3		59		O	RTC_C clock calibration output
Reference	VREF+	P5.6		70		O	Internal shared reference voltage positive terminal
	VREF-	P5.7		71		O	Internal shared reference voltage negative terminal
	VeREF+	P5.6		70		I	Positive terminal of external reference voltage to ADC
	VeREF-	P5.7		71		I	Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground)
SPI	UCA0CLK	P1.1		5		I/O	Clock signal input for eUSCI_A0 SPI slave mode. Clock signal output for eUSCI_A0 SPI master mode
	UCA0SIMO	P1.3		7		I/O	Slave in, master out for eUSCI_A0 SPI mode
	UCA0SOMI	P1.2		6		I/O	Slave out, master in for eUSCI_A0 SPI mode
	UCA0STE	P1.0		4		I/O	Slave transmit enable for eUSCI_A0 SPI mode
	UCA3CLK	P9.5		97		I/O	Clock signal input for eUSCI_A3 SPI slave mode. Clock signal output for eUSCI_A3 SPI master mode
	UCA3SIMO	P9.7		99		I/O	Slave in, master out for eUSCI_A3 SPI mode
	UCA3SOMI	P9.6		98		I/O	Slave out, master in for eUSCI_A3 SPI mode
	UCA3STE	P9.4		96		I/O	Slave transmit enable for eUSCI_A3 SPI mode
	UCB0CLK	P1.5		9		I/O	Clock signal input for eUSCI_B0 SPI slave mode. Clock signal output for eUSCI_B0 SPI master mode
	UCB0SIMO	P1.6		10		I/O	Slave in, master out for eUSCI_B0 SPI mode
	UCB0SOMI	P1.7		11		I/O	Slave out, master in for eUSCI_B0 SPI mode
	UCB0STE	P1.4		8		I/O	Slave transmit enable for eUSCI_B0 SPI mode
	UCB1CLK	P6.3		77		I/O	Clock signal input for eUSCI_B1 SPI slave mode. Clock signal output for eUSCI_B1 SPI master mode
	UCB1SIMO	P6.4		78		I/O	Slave in, master out for eUSCI_B1 SPI mode
	UCB1SOMI	P6.5		79		I/O	Slave out, master in for eUSCI_B1 SPI mode
	UCB1STE	P6.2		76		I/O	Slave transmit enable for eUSCI_B1 SPI mode

	UCB3CLK	P10.1	P8.1	1	31	I/O	Clock signal input for eUSCI_B3 SPI slave mode. Clock signal output for eUSCI_B3 SPI master mode
	UCB3SIMO	P10.2	P6.6	2	80	I/O	Slave in, master out for eUSCI_B3 SPI mode
	UCB3SOMI	P10.3	P6.7	3	81	I/O	Slave out, master in for eUSCI_B3 SPI mode
	UCB3STE	P8.0	P10.0	30	100	I/O	Slave transmit enable for eUSCI_B3 SPI mode
System	NMI			83		I	External nonmaskable interrupt
	RSTn			83		I	External reset (active low)
	SVMHOUT	P4.4		60		O	SVMH output
Thermal	QFN Pad		0	N/A			QFN package exposed thermal pad. TI recommends connection to VSS.
Timer	PM_TA1.1	P7.7		29		I/O	Default mapping: TA1 CCR1 capture: CCI1A input, compare: Out1
	TA1.0	P8.0		30		I/O	TA1 CCR0 capture: CCI0A input, compare: Out0
	TA2.0	P8.1		31		I/O	TA2 CCR0 capture: CCI0A input, compare: Out0
	TA2.1	P5.6		70		I/O	TA2 CCR1 capture: CCI1A input, compare: Out1
	TA2.2	P5.7		71		I/O	TA2 CCR2 capture: CCI2A input, compare: Out2
	TA2.3	P6.6		80		I/O	TA2 CCR3 capture: CCI3A input, compare: Out3
	TA2.4	P6.7		81		I/O	TA2 CCR4 capture: CCI4A input, compare: Out4
	TA2CLK	P4.2		58		I	TA2 input clock
	TA3.0	P10.4		24		I/O	TA3 CCR0 capture: CCI0A input, compare: Out0
	TA3.1	P10.5		25		I/O	TA3 CCR1 capture: CCI1A input, compare: Out1
	TA3.2	P8.2		46		I/O	TA3 CCR2 capture: CCI2A input, compare: Out2
	TA3.3	P9.2		74		I/O	TA3 CCR3 capture: CCI3A input, compare: Out3
	TA3.4	P9.3		75		I/O	TA3 CCR4 capture: CCI4A input, compare: Out4
	TA3CLK	P8.3		47		I	TA3 input clock
UART	UCA0RXD	P1.2		6		I	Receive data for eUSCI_A0 UART mode
	UCA0TXD	P1.3		7		O	Transmit data for eUSCI_A0 UART mode
	UCA3RXD	P9.6		98		I	Receive data for eUSCI_A3 UART mode
	UCA3TXD	P9.7		99		O	Transmit data for eUSCI_A3 UART mode