







Institute for Computing Systems Architecture

A Machine Learning Based Parallelization Assistant

Aleksandr Maramzin, Christos Vasiladiotis, Roberto Castañeda Lozano, Björn Franke, Murray Cole

> The University of Edinburgh **United Kingdom**













Institute for Computing Systems Architecture

A Machine Learning Based Parallelization Assistant

Aleksandr Maramzin, Christos Vasiladiotis, Roberto Castañeda Lozano, Björn Franke, Murrav Cole

"It Looks Like You're Writing a Parallel Loop"





Problem Statement

Parallel Hardware is Ubiqutous

Software is Sequential

Auto Parallelization is Limited

Manual Parallelization is Hard





Problem Statement [1]

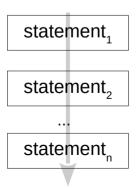
Hardware is parallel

(across the whole range of computing systems)



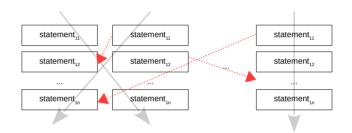
Software is sequential

(a great deal of legacy software is written in a sequential fashion)



Automatic parallelization is limited

(automatic parallelization does not achieve performance levels of manually parallelized code)



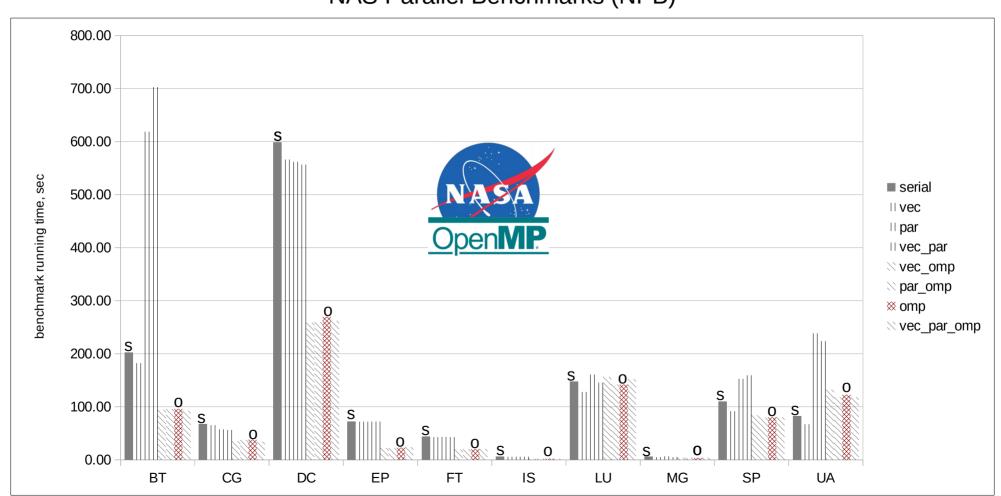
Parallel programming is hard

(requires application domain expertise, familiarity with parallel programming in general and exact frameworks (OpenMP, MPI) in particular, etc.)



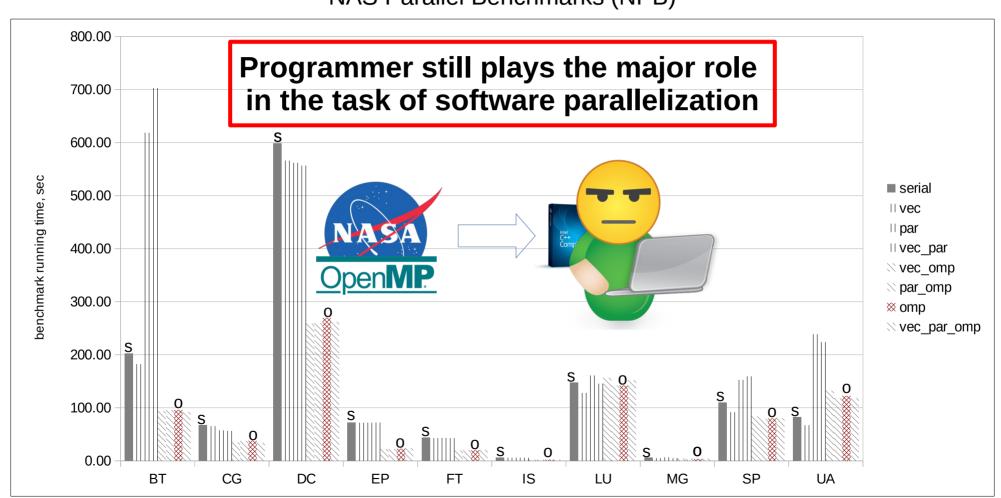
Problem Statement [2]

NAS Parallel Benchmarks (NPB)



Problem Statement [2]

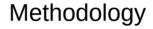
NAS Parallel Benchmarks (NPB)



Proposed Solution

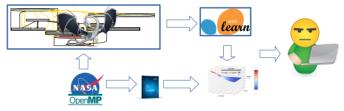
(we propose a novel assistant tool and the methodology to alleviate the process of manual software parallelization)

Tool





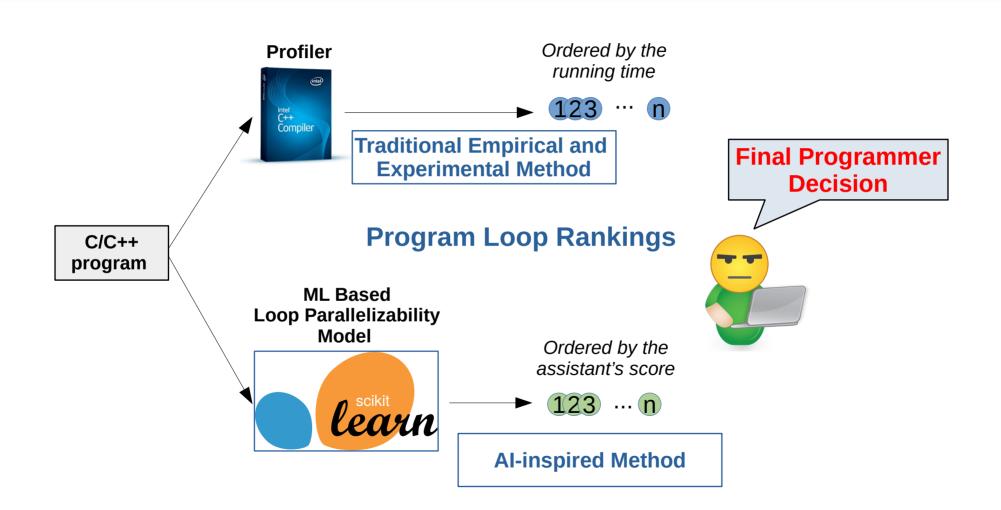
&



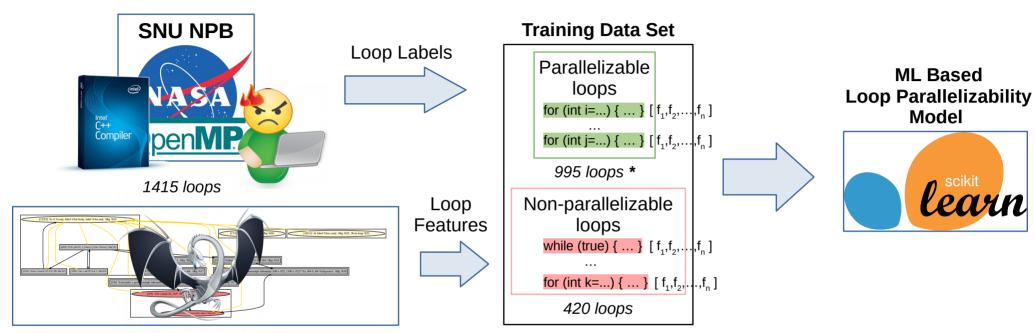




How to use the assistant



Solution Scheme [1]



* Intel Compiler succeeds in parallelizing 812 loops

Loop features are based on static structural properties of loop program dependence graphs (PDGs):

- Absolute size
- Loop Iterator/Payload cohesion
- Number of dependence edges
- Instruction types (calls, loads/stores, etc.)

Loop labels are derived out of OpenMP pragmas present in parallelized SNU NPB versions as well as from the Intel Compiler's parallelization/vectorization reports.

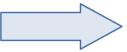
Model

Solution Scheme [2]

Profiler



Potential Contribution to Speedup

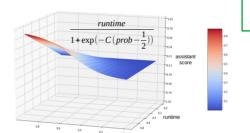


ML Based Loop Parallelizability Model

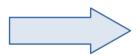


Predicted Probability of Parallelization

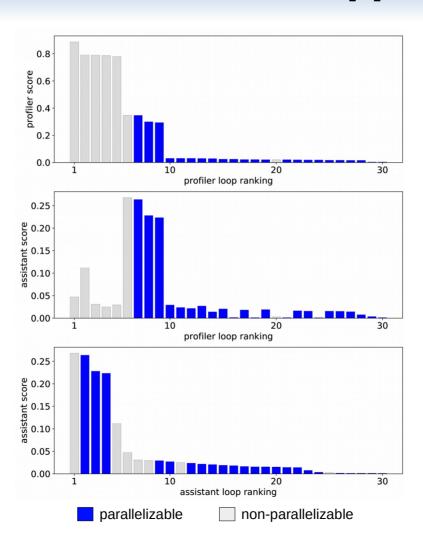




Improved Loop Ranking



Solution Scheme [2]



Results



Predictive performance of our ML based loop parallelizability model

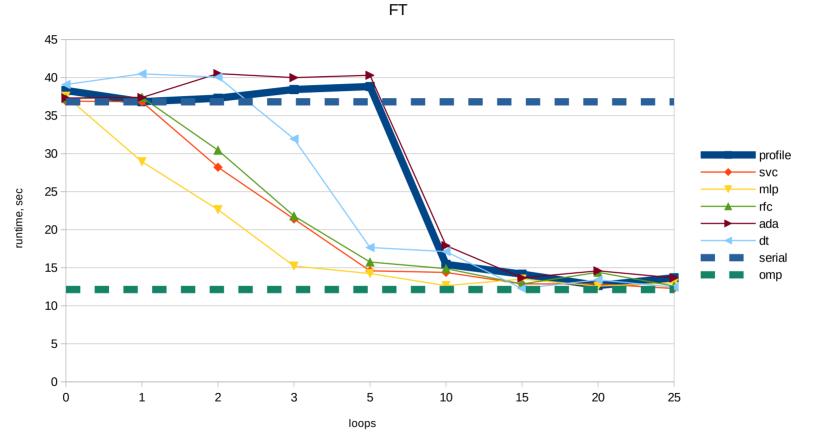


Deployment of our assistant on SNU NPB benchmarks









Manual software parallelization faster

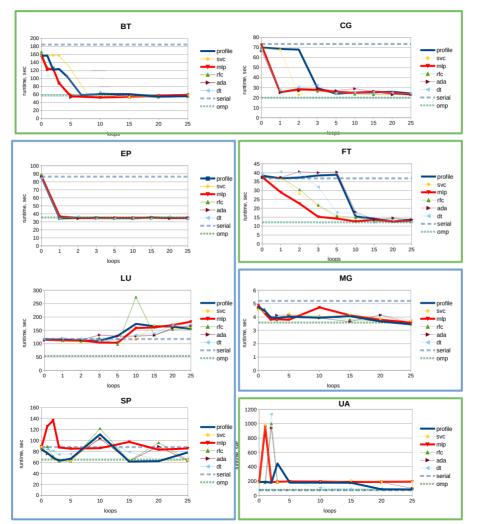
(examine and parallelize 20% fewer Lines Of Code (LOC) to get to the best achievable performance)



Improvement in

4 benchmarks

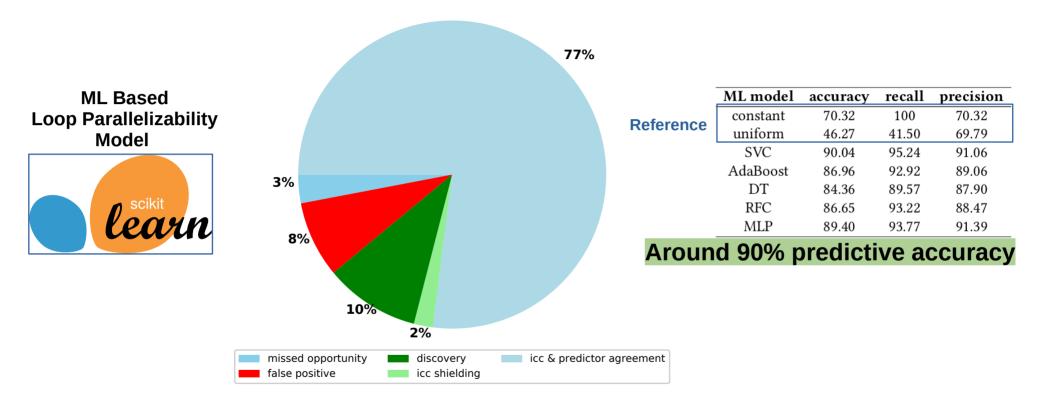
Assistant Deployment



No change in 4 other benchmarks



learn Predictive Performance



Agreement rate of 80%

Discovery rate of 10%

False positive rate of 8% is not critical

Summary & Conclusions

- Despite decades of research into parallelizing compiler technology human experts still play the major role in the task
- Loop parallelizability is learnable property (we created ML model and trained it to work with the accuracy of above 90%)
- ML model of loop parallelizability has been harnessed into an assistant scheme guiding a programmer towards the best achievable performance
- Deployed against SNU NPB benchmarks our assistant showed a faster convergence: 20% Lines Of Code (LOC) reduction

Thank you!







SNU NPB Conjugate Gradient (CG) benchmark

Motivating example

VS.

```
Profiler's Loop
Ranking
```

- 1 cg.c:326
- 2 cg.c:484
- 3 cg.c:509

```
Assistant's Assistant's Parallel Loop
Loop Ranking Probability
```

- 1 cg.c:509
- **2** cg.c:326
- 3 cg.c:484

[**85%**]
[29%]

```
for (j = 0; j < lastrow-firstrow+1; j++) {
   suml = 0.0;
   for (k = rowstr[j]; k < rowstr[j+1]; k++)
      suml = suml + a[k]*p[colidx[k]];
   q[j] = suml;
}</pre>
cg.c:509
```

