







Institute for Computing Systems Architecture

A Machine Learning Based Parallelization Assistant

Aleksandr Maramzin, Christos Vasiladiotis, Roberto Castañeda Lozano, Björn Franke, Murray Cole

> The University of Edinburgh **United Kingdom**













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"It Looks Like You're Writing a Parallel Loop"





Presentation Structure

- Problem statement
- How to use the assistant tool
- Assistant internals
- Parallelization of SNU NPB benchmarks



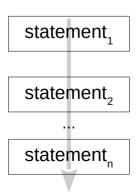


Problem Statement

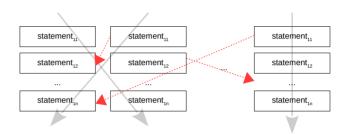
Parallel Hardware is Ubiqutous



Software is Sequential



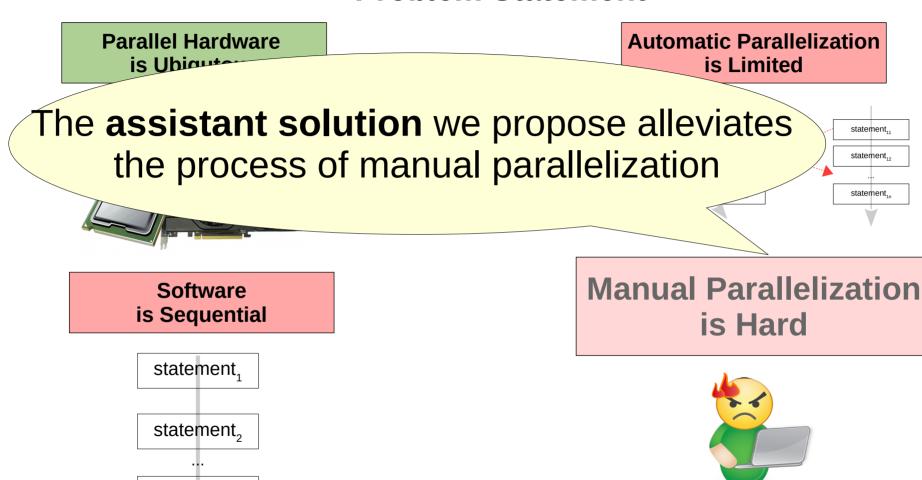
Automatic Parallelization is Limited



Manual Parallelization is Hard



Problem Statement



statement

statement.

statement,,

statement.

Problem Statement

NAS Parallel Benchmarks (NPB)



Parallelization Speedup (Gmean)

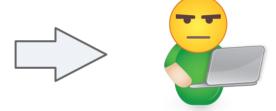
Manual: **1.73**x

Automatic: **0.79x** - **1.10x**



Programmer still plays the major role in the hard task of software parallelization

```
Source Code
  for (int i=0; ... ) {
for (int j=0; j<n;...) {
  L_n:
   for (int m=0;...) {
         for (int k=m; k<n;...) {
```



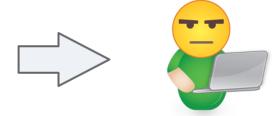
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Program Loop Rankings

Source Order L_0, L_1, \ldots, L_n

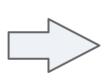


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Program Loop Rankings



Source Order L_0, L_1, \ldots, L_n





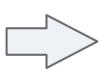
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Program Loop Rankings



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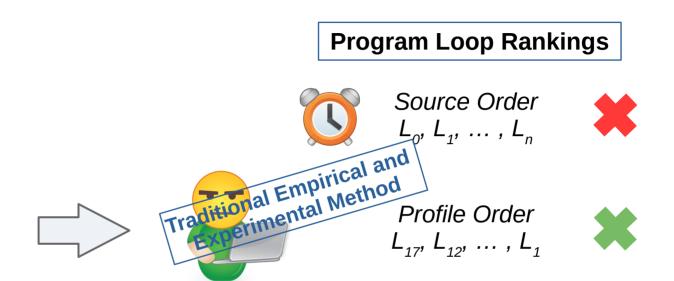


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   for (int m=0;...) {
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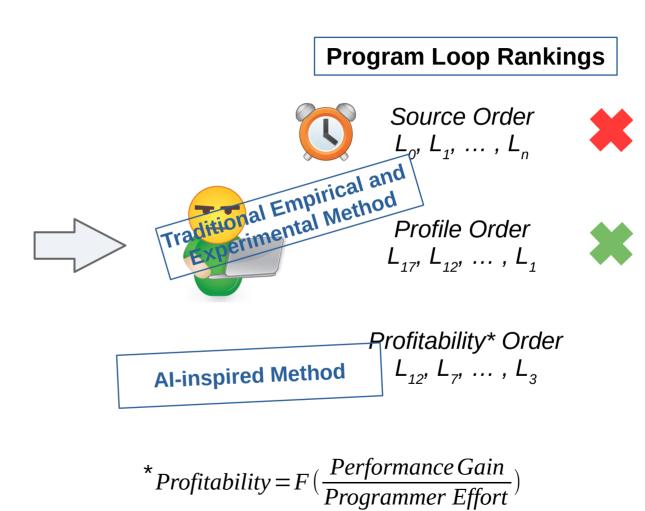
Program Loop Rankings Source Order L₀, L₁, ..., L_n



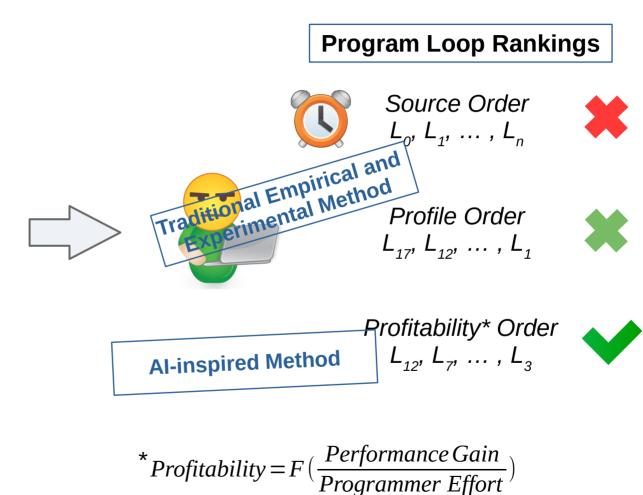
```
Source Code
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for (int j=0; j<n;...) {
   L_n:
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```



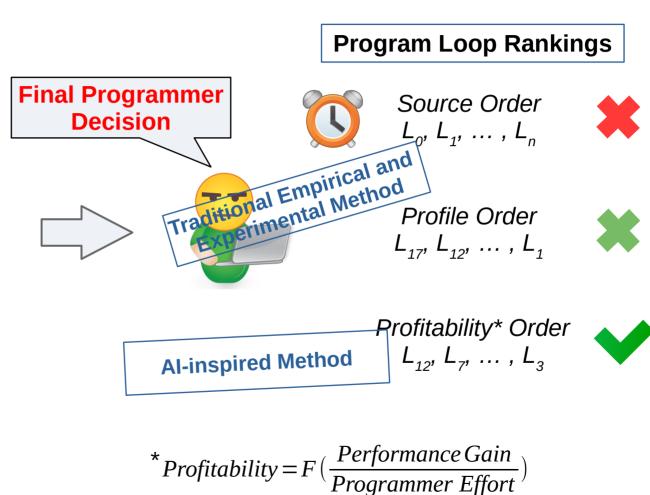
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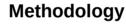
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   for (int m=0;...) {
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```



Proposed Solution

(ML based software parallelization assistant)

Tool

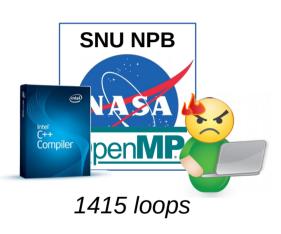




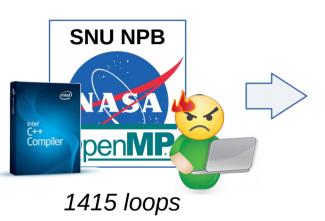


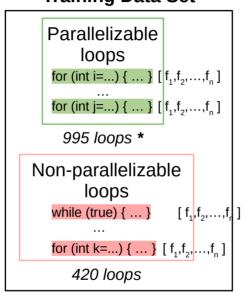




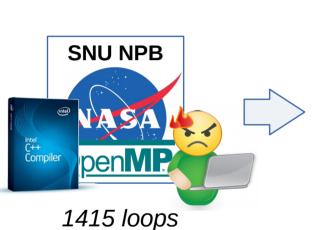


Training Data Set

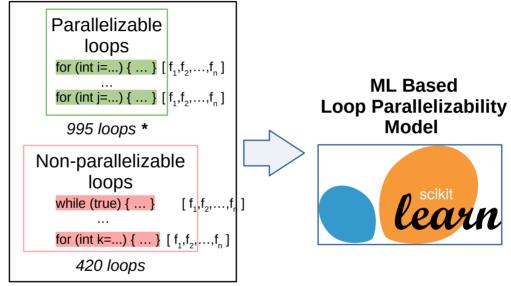




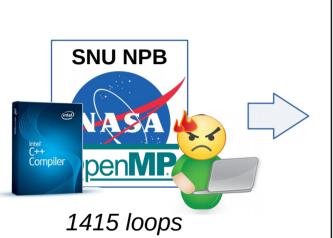
^{*} Intel Compiler succeeds in parallelizing 812 loops



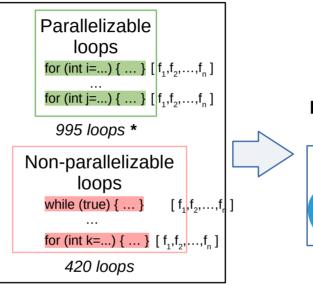




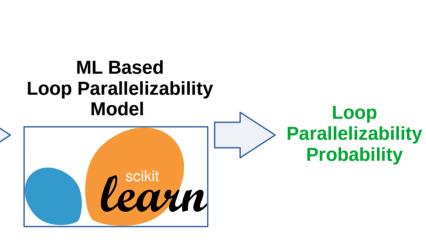
* Intel Compiler succeeds in parallelizing 812 loops



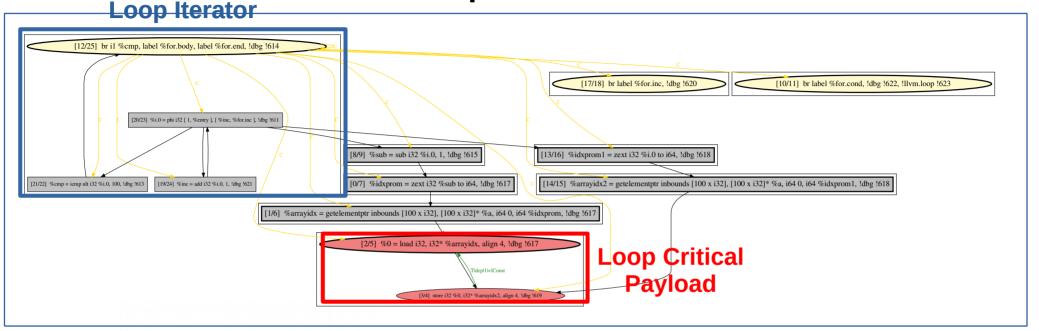
Training Data Set



* Intel Compiler succeeds in parallelizing 812 loops



Loop Features





Loop features are based on static structural properties of loop program dependence graphs (PDGs):

- Absolute size
- Loop Iterator/Payload cohesion
- Number of dependence edges
- Instruction types (calls, loads/stores, etc.)
- etc.

ML Based Loop Parallelizability Model



ML Based Loop Parallelizability Model



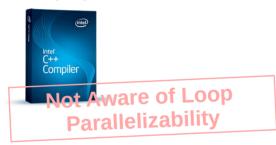
Profiler



ML Based Loop Parallelizability Model

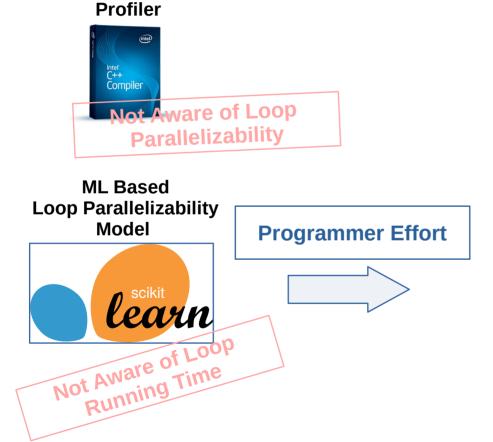


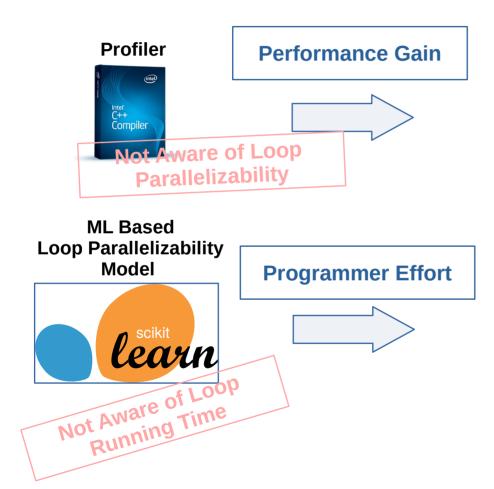
Profiler

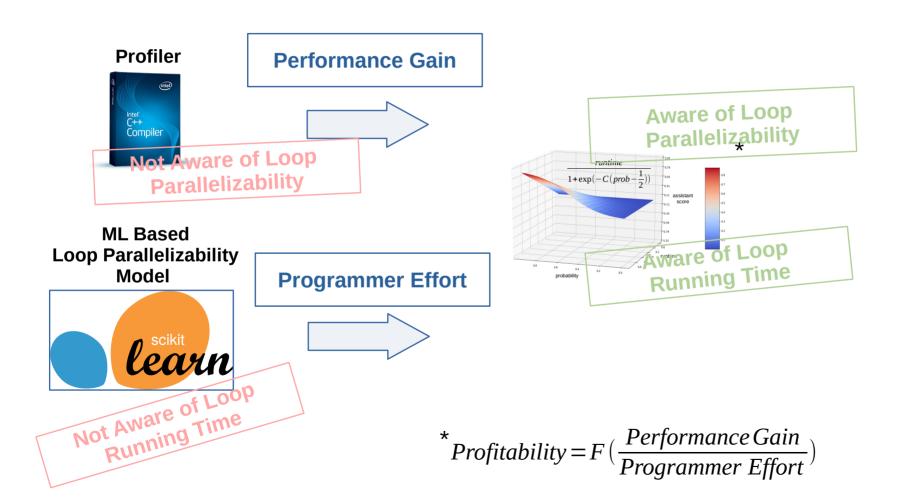


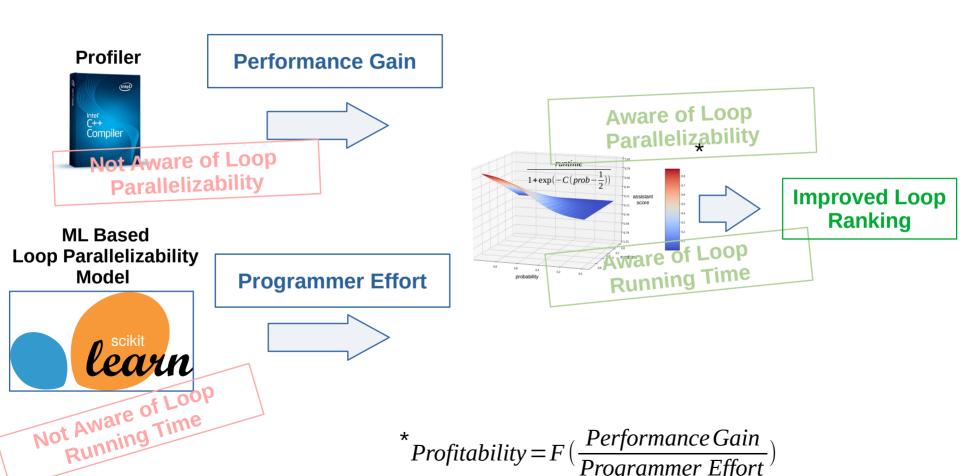
ML Based Loop Parallelizability Model











*Profitability = $F(\frac{Performance Gain}{Programmer Effort})$

Results



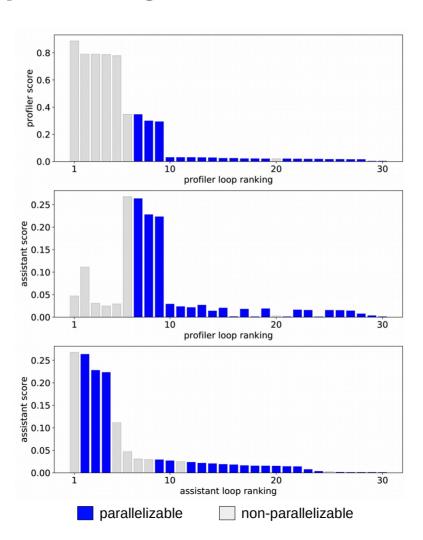
Deployment of our assistant on SNU NPB benchmarks

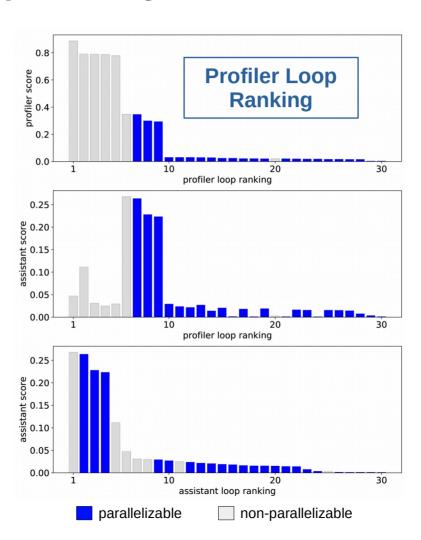


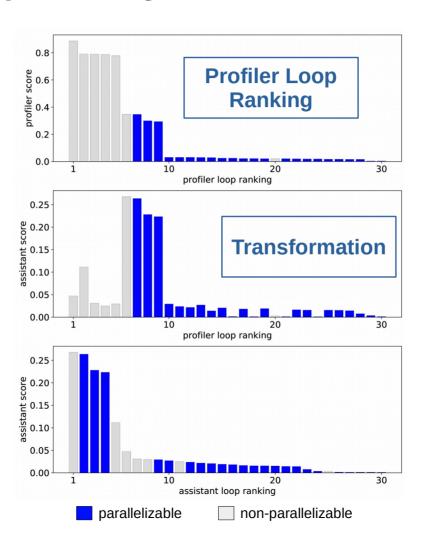
Predictive performance of our ML based loop parallelizability model

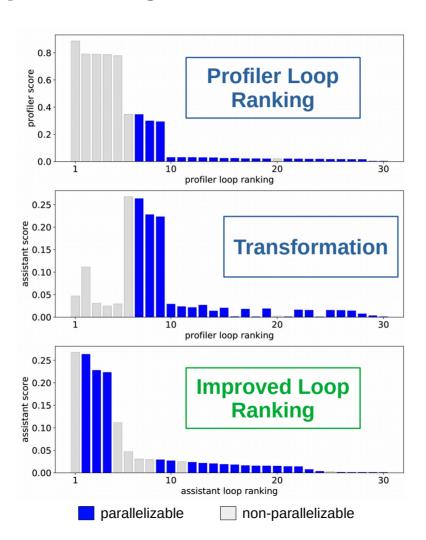




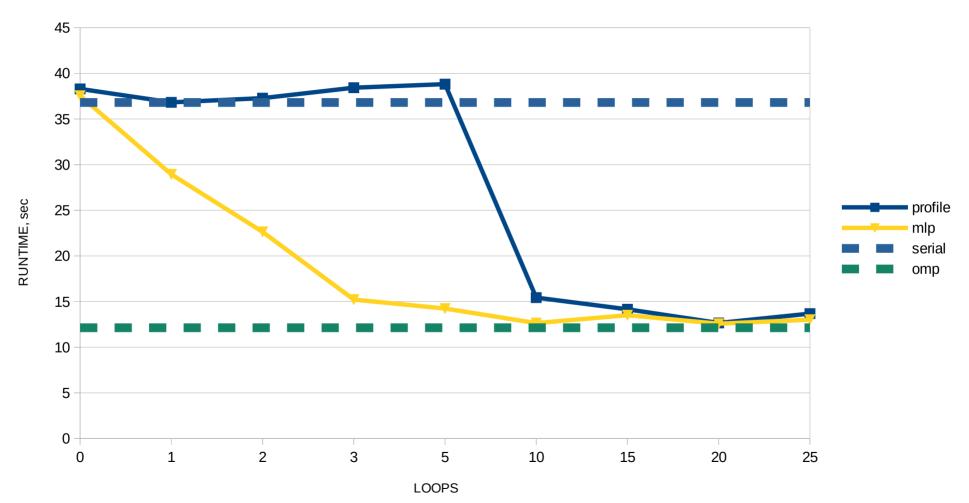


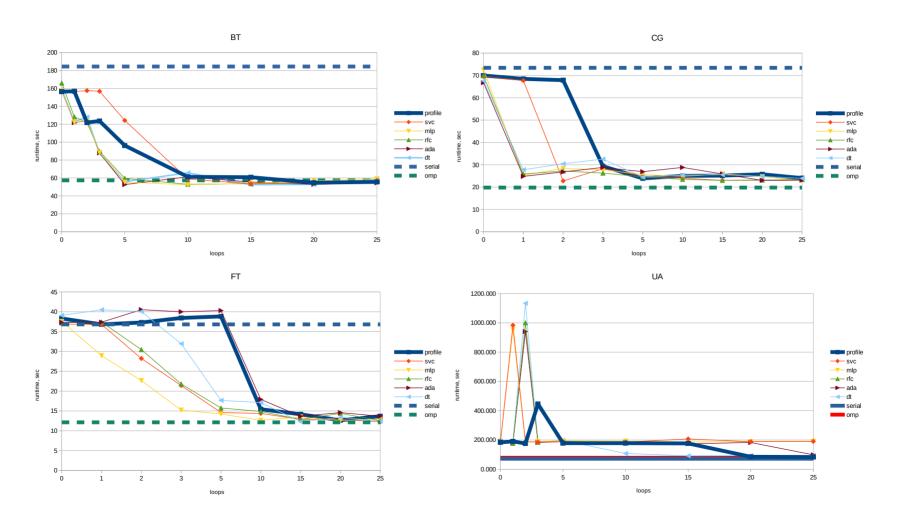


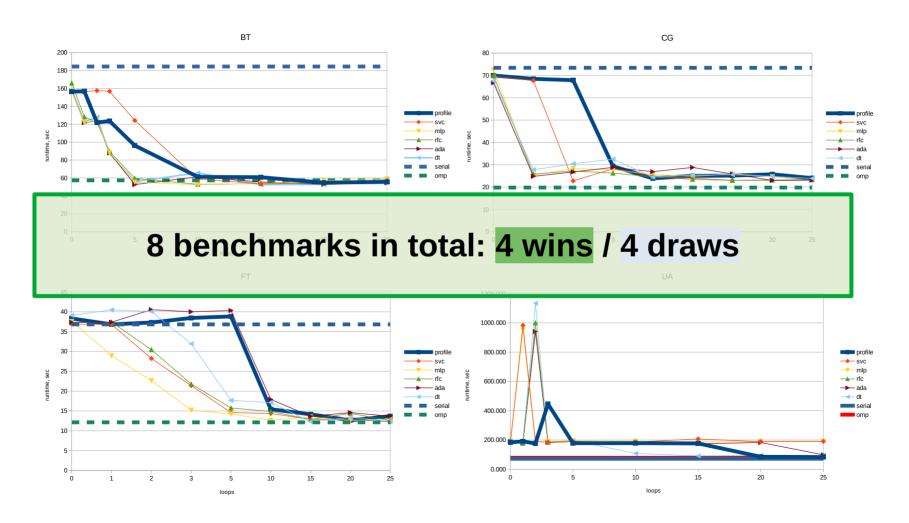


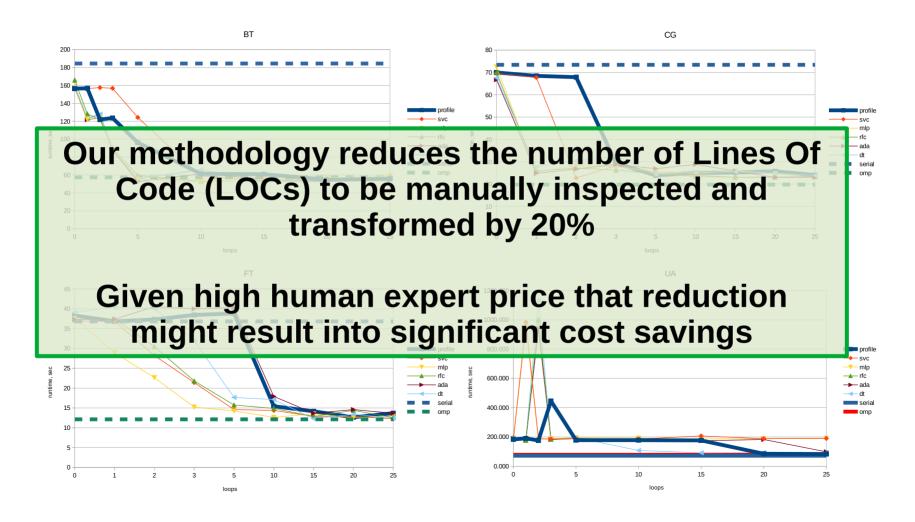


FT









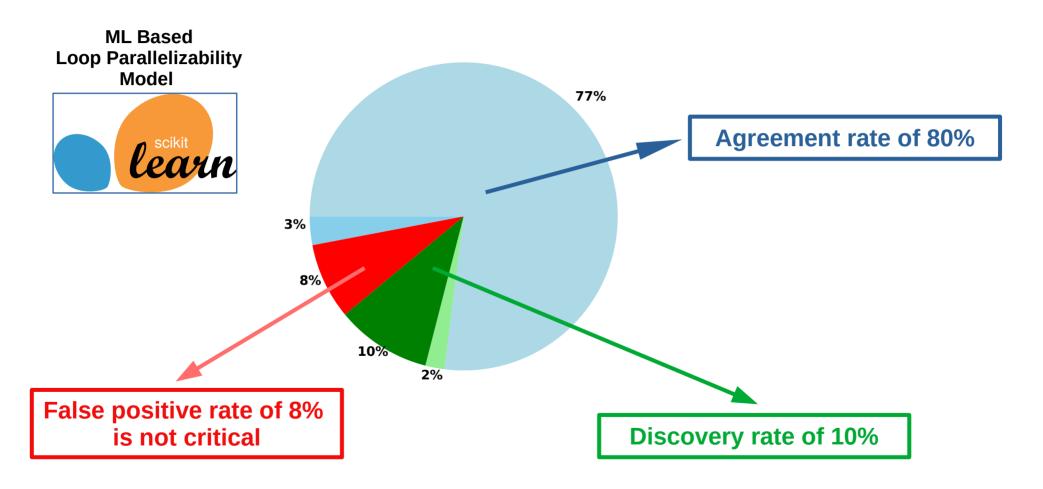
ML Model Predictive Performance

Reference

ML model	accuracy	recall	precision
constant	70.32	100	70.32
uniform	46.27	41.50	69.79
SVC	90.04	95.24	91.06
AdaBoost	86.96	92.92	89.06
DT	84.36	89.57	87.90
RFC	86.65	93.22	88.47
MLP	89.40	93.77	91.39

Around 90% predictive accuracy

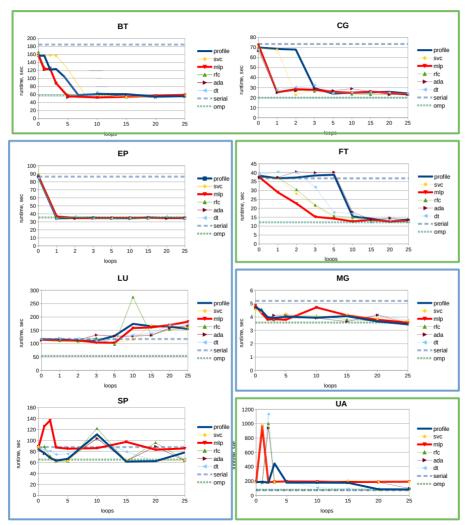
ML Model Predictive Performance



Summary & Conclusions

- Human experts still play the major role in the task of software parallelization
- Loop parallelizability is learnable property (we introduce a ML model and train it to work with the accuracy of above 90%)
- ML model of loop parallelizability has been integrated into parallelization assistant
- Deployed against SNU NPB benchmarks our assistant showed a faster parallelization process: 20% Lines Of Code (LOC) reduction





Motivating example

VS.



SNU NPB Conjugate Gradient (CG) benchmark

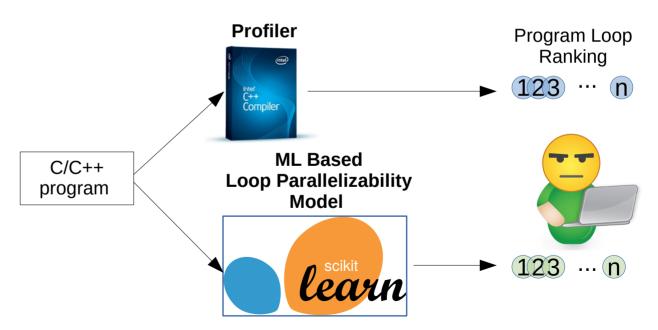
```
Profiler's Loop
Ranking
```

- 1 cg.c:326
- 2 cg.c:484
- 3 cg.c:509

```
Assistant's Assistant's Parallel Loop
Loop Ranking Probability
```

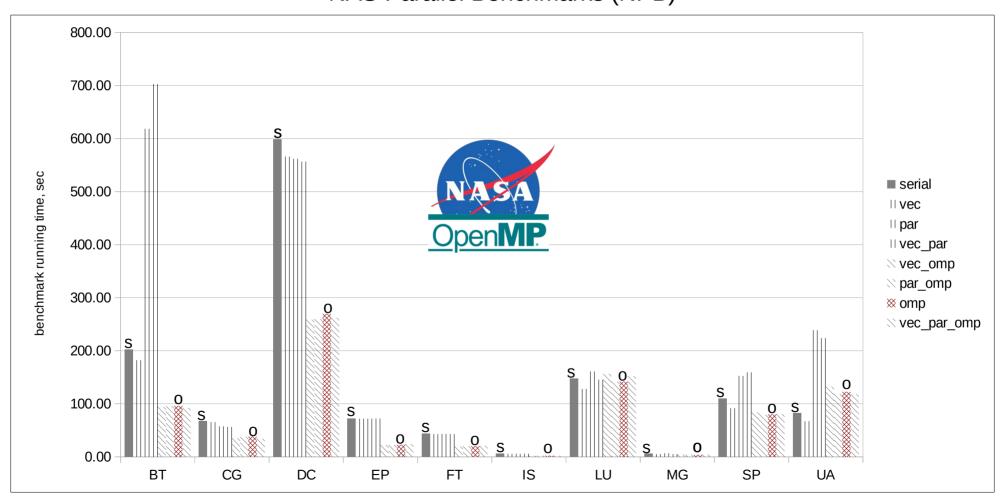
- $(1) cg.c:509 \qquad \qquad [85\%]$
- 2 cg.c:326 [29%]
- 3 cg.c:484 [8%]

```
for (j = 0; j < lastrow-firstrow+1; j++) {
   suml = 0.0;
   for (k = rowstr[j]; k < rowstr[j+1]; k++)
      suml = suml + a[k]*p[colidx[k]];
   q[j] = suml;
}</pre>
cg.c:509
```



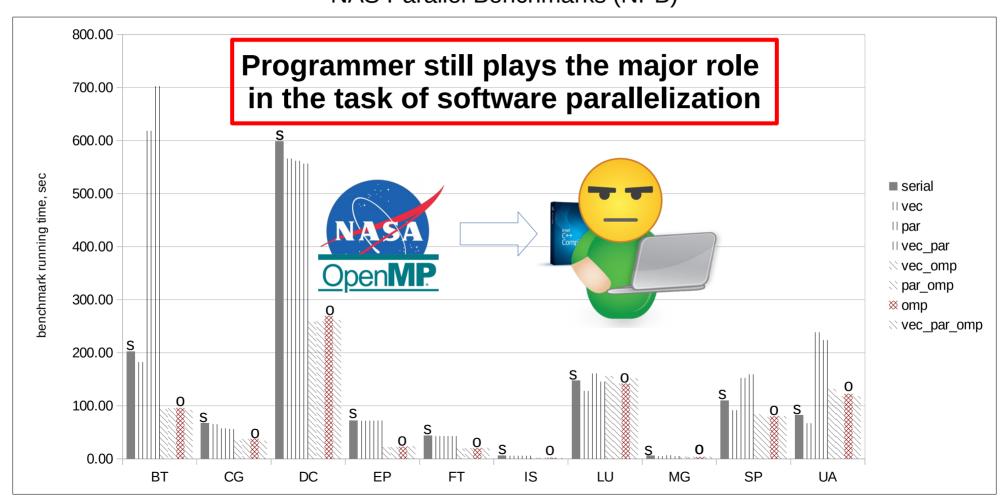
Problem Statement 2/2

NAS Parallel Benchmarks (NPB)



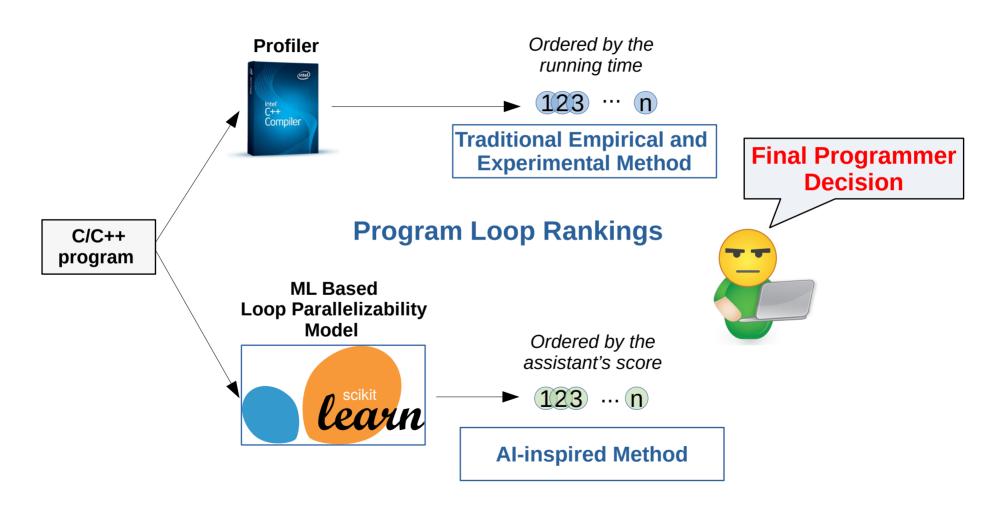
Problem Statement 2/2

NAS Parallel Benchmarks (NPB)

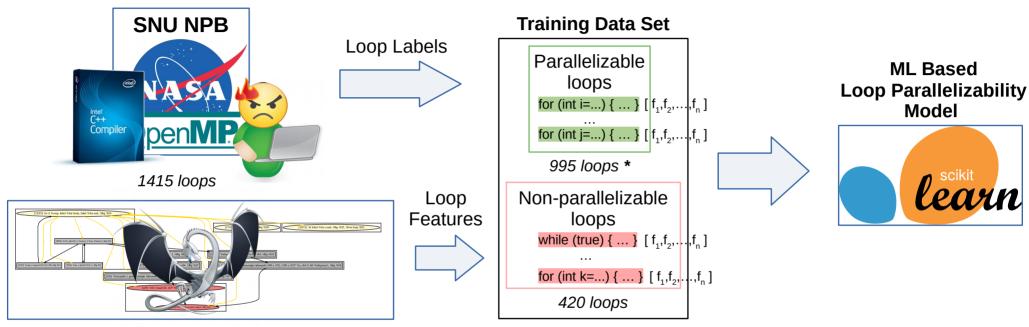


How to use the assistant

(from the programmers perspective)



Solution Scheme [1/2]



Loop features are based on static structural properties of loop program dependence graphs

(PDGs):

Absolute size

Loop Iterator/Payload cohesion

- Number of dependence edges
- Instruction types (calls, loads/stores, etc.)

* Intel Compiler succeeds in parallelizing 812 loops

Loop labels are derived out of OpenMP pragmas present in parallelized SNU NPB versions as well as from the Intel Compiler's parallelization/vectorization reports.



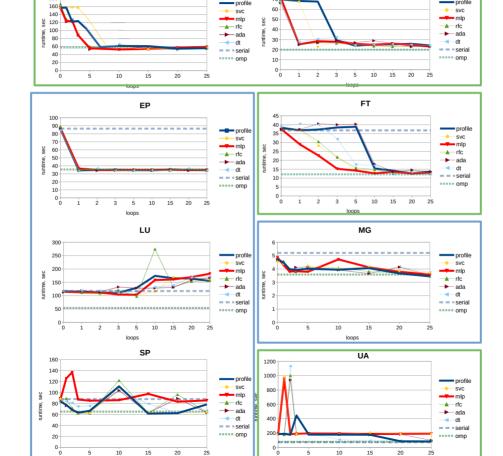
Improvement in

4 benchmarks

вт

How well do we do?

CG



No change in 4 other benchmarks

Problem Statement

NAS Parallel Benchmarks (NPB)

