|  |
| --- |
| AMIT ANIL PATANKAR |

**Email:** av8ramit@berkeley.edu **Phone:** (510) 364-8215 **Address:** 2732 Haste Ave #9, Berkeley, CA 94704

**EDUCATION**

**University of California at Berkeley** *GPA: 3.3 College of Engineering*

*Major*: **B.S. Electrical Engineering and Computer Science**  *Expected date of graduation: May 2015*

**EXPERIENCE**

**NetSpeed Systems *(Engineering Intern)*** *San Jose, CA, Apr 2013 – Sept 2013*

* Designed a cycle approximate model for a network on chip (NoC) that injected and ejected packets from different interfaces, advanced the clock cycle, and created a NoC based upon added hosts and traffic patterns
* Extensively updated SoC interconnect simulator to support parallel packet injection, randomized packet generation, tx/rx rate enforcement, imported traffic profiles, and NoC layer arbitration amongst competing flows ***(Patent Pending)***
* Implemented deterministic algorithm and protocol for random packet generation and NoC/VC arbitration for tx packets
* Improved user control over traffic patterns, message rates, statistics generation, latency display, and tooltips in GUI
* Completely randomized and automated C++ tests for model, simulator, host manipulation, and NoC generation

**Violin Memory *(Engineering and Software Intern)*** *Mountain View, CA, Dec 2011 – Aug 2012*

* Used a linting tool (Atrenta Spyglass) to review the engineers' HDL files and catch for inefficient design errors and other potential design issues in order to prevent problems when chips were synthesized
* Created Python applications that synthesized Verilog code for a state machine using an adjacency matrix and created a directory that contained all possible state machine path combinations. The applications are still used by engineers today
* Programmed an I2C state machine in Verilog that would take an address and command and dependent on the command either read or write 16 bits of data into the specified address used on memory controllers

**PROJECTS**

**LightBike *(Product Designer)***  *Berkeley, CA, Sept 2012 – Nov 2012*

* Programmed an Arduino circuit board to control 8 individual LED lights to display patterns on a rotating bike wheel
* Created a completely self powered and accelerometer based design that produces a position based pattern

**Course Projects**  *Berkeley, CA, Aug 2011 – Present*

* Xilinx Virtex-5 FPGA development using Verilog to build a SRAM arbiter, DoG filter, and DVI controller for VGA
* Complete PCB layout design of an EEG from RLC level that accurately measured brain activity and filtered noise
* Matrix Multiply Optimization from 3 to 75 gigaflops using OpenMP multithreading and Intel SSE Intrinsics
* Created my own Hybrid Data Structure in Java that combined a Hash Table, an Array, and a Graph

**TECHNICAL COURSES TAKEN**

FPGAs & Synchronous Digital Systems

Computer Architecture (Machine Structures)

Data Structures & Advanced Programming Methodology

Structures & Interpretations of Computer Programs

Microelectronic Circuits **(Enrolled)**

Systems and Signals **(Enrolled)**

Computer Networking

Discrete Mathematics & Probability Theory

**TECHNOLOGY SUMMARY**

**Languages**: *PYTHON, C++, C, VERILOG, JAVA, UNIX, MIPS, MATHSCRIPT*

**Platforms**: HSpice, *FPGA Editor, Chipscope, ModelSim, Verdi, Visual Studio, Atrenta Spyglass, NI Labview/Multisim, Arduino*

**Web:** *HTML, CSS, PHP, Wordpress, Joomla, Wix, Bootstrap |* **Visit http://amitpatankar.com/**

**ABOUT ME**

* Member of Theta Tau Professional Engineering Fraternity Epsilon (Berkeley) Chapter in Iota Pledge Class
* Former Technical Consultant for Voyager Consulting Group at UC Berkeley
* Lead Programmer for a Botball Robotics Team. Responsible for main Roomba robot controller functions
* Fluent in four languages: English, Spanish, Hindi, and Marathi
* US Citizen since Birth and Overseas Citizen of India
* Hobbies include basketball, traveling, aviation, TV shows, sports, fantasy leagues, foreign movies, and programming